

Further notes on Circuit Notebook contribution

Thank you for publishing my idea in Circuit Notebook, November 2016 ("Precision switched capacitor DAC needs no precision components") and for improving the clarity of my submission.

I would like to point out to readers that my submission consisted of only the skeleton of the idea, which included Fig.1 and Fig.2 and the descriptions that applied to them. SILICON CHIP staffers have fleshed it out to include Fig.3 and the associated text.

I'm happy that SILICON CHIP has edited and expanded my submission to improve it; the clarity of the description has been improved significantly compared to my submission, and adding extra switches to increase the output range of the circuit to include both 0V and V_{ref} is an inspired idea.

As I was reading the text, it dawned on me that the fourth divider stage of Fig.1 (that was also present in my original submission) is unnecessary. This fourth divider stage has probably also led to some confusion in the text regarding whether Fig.1 represents a 3 or 4-bit DAC: it is in

fact a 3-bit DAC.

Fig.3 does not repeat this error and is therefore a 4.1 bit DAC as stated. However, a small change renders IC8, D1 and D2 unnecessary.

For simplicity, I'll describe the change with reference to Fig.1. All that is required is to take V_{out} from the common terminal of the bottom half of S3. S3 now only needs to be an SPDT switch and the 4th divider stage is no longer needed. With this arrangement, V_{out} will vary from 0V to $7/8 * V_{ref}$ in $V_{ref} / 8$ steps as the digital input is varied from 0 to 7, making it unnecessary to subtract 1 from the digital input.

This rearrangement produces a 3-bit DAC with fewer components than previously required. If it is necessary for the output to range between 0V and V_{ref} (making a 3.1 bit DAC), add a fourth SPDT switch, S0, that switches the output between V_{ref} (when S0 is 1) and the common terminal of S3 (when S0 is 0).

Similar changes can be made to the circuit of Fig.3 to make a 4.1 bit binary DAC with glitch rejection.

**Andrew Partridge,
Toowoomba, Qld.**

DAC circuit should have precision capacitors

Andrew Partridge's interesting article in the Circuit Notebook pages of the November 2016 issue, using a capacitor-based Kelvin-Varley divider in a DAC, does require precision capacitors to work accurately. If the paired capacitors are exactly equal in capacitance then the output voltage is exactly one-half of the input voltage. But if they are not equal when the capacitors are paralleled up and charge flows from the higher charged capacitor to the lower charged capacitor then while the resultant voltage will tend towards one half of the input voltage, it is not exactly one half if the two capacitors don't have equal value.

To demonstrate:

$$C_1 = C_2 \quad V_o/V_i = 0.500$$

$$C_1 = 1.05 C_2 \quad V_o/V_i = 0.498$$

$$C_1 = 1.30 C_2 \quad V_o/V_i = 0.491$$

~~$$C_1 = 2.00 C_2 \quad V_o/V_i = 0.444$$~~

So for a 5% capacitor mismatch ($C_1=1.05$ times C_2), the voltage error is much less at 0.4%. Likewise, if the mismatch is 100% ($C_1=2$ times C_2), the error is 6%.

Ken Moxham,
Urrbrae, SA.