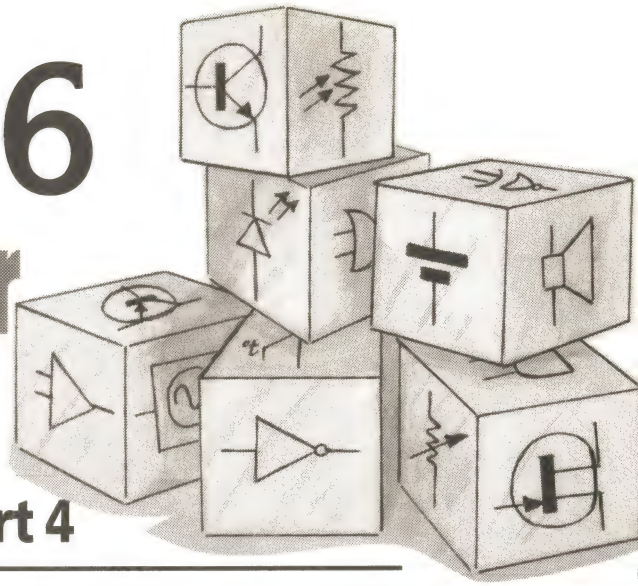
TEACH-IN '96

A Guide to Modular Circuit Design



Max Horsey

Part 4

DURING this series of articles, a range of circuit modules is examined, divided into Input, Processor and Output sections. Where possible a choice of module is offered within each section.

Each of the ten Parts of the Series is accompanied by a constructional article explaining how a complete project may be devised by employing the modules described, together with a p.c.b. design. Each project will be one of many possible ideas that could be implemented and it is hoped that readers will design for themselves a variety of circuits by combining modules provided in the whole series.

The proposed range of modules covered by the Series is detailed in Part 1, Table 1.1. Each module is chosen to link easily with adjacent modules in the same Part, but modules may also be linked with modules in other Parts of the Series.

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HERE in this fourth Part of *Teach-In*, the following Input, Processor and Output modules are examined:

INPUT MODULES: Astables, based on:
- a. logic gates – simple arrangement
- b. voltage controlled variable frequency version
- c. logic gates – improved square wave oscillator
- d. 741 relaxation oscillator
- e. 555 timer

PROCESSOR MODULES: Decade chaser and counter

OUTPUT MODULE: L.E.D., discussing series resistance

The accompanying example project described separately is based around a selection of these modules and is a Vari-Speed Dice indicator. It contains two sets of six l.e.d.s which "chase" when a switch is pressed. When the switch is released the chase speed slows down and finally stops, resulting in a pair of random numbers being highlighted. The effect can be likened to the action of a roulette wheel.

ASTABLE MODULES

Astable circuits based around digital gates generate a continuous stream of "clock pulses", usually square waves. The term *clock pulse* implies a clean change between two voltage levels, often between 0V and close to the positive power rail voltage, generally referred to as *logic 0* and *logic 1*, respectively.

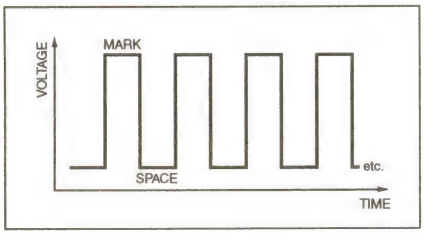


Fig. 4.1. Pulse train with even mark/space ratio.

Some oscilloscopes may have difficulty displaying the vertical aspects of *good quality* pulses (i.e. which rapidly change their logic states), such as those forming the pulse train illustrated in Fig. 4.1, and only the horizontal parts may be seen clearly.

If the time for which the pulse voltage is high equals the time for which it is low, it is said that the pulse *mark/space* ratio is equal, a condition which defines a square wave. If the *mark* (logic 1 level) time is added to the *space* (logic 0 level) time, the total is known as the *period* of the waveform. From this quantity, the frequency of the waveform (i.e. number of waves per second) can be calculated using the formula:

Frequency = 1 / Period

where the frequency is measured in Hertz (Hz), and the period is measured in seconds (s).

Counter circuits increment (add one to) their count value at the instant when the voltage on their clock input changes in a given direction, either positive-going (upwards) or negative-going (downwards). Although most counter circuits require a clock pulse having a clean transition between the two voltage levels, the pulse's mark/space ratio need not be equal.

SIMPLE ASTABLE

If the inputs of a NOR gate or a NAND gate are connected together, the NOR or NAND behaves like a NOT gate or inverter. Since all the following logic-based astable circuits require NOT gates, it follows that NOT gates, NOR gates or NAND gates may be used, and the choice may depend upon the requirements of other parts of the project.

The circuit diagram in Fig. 4.2 shows how a pair of NOR gates can be used to produce a simple astable which generates reasonably good square wave pulses. The frequency is variable by means of potentiometer VR1.

The output frequency signal is normally taken from point Y, as shown, but an inverted output is available from point X if required. Output X is positive when Output Y is at 0V, and vice-versa.

Frequency is determined by the values of capacitor C1, resistor R1 and the resistance set by potentiometer VR1. If the total resistance set by R1 plus VR1 is doubled, or if the value of C1 is doubled, the frequency will be halved.

Select a maximum value for VR1 which provides a frequency slightly lower than that likely to be needed. Resistor R1 should be about one kilohm (1k), and is used to prevent the total resistance approaching zero when VR1 is set for minimum resistance.

Example component values and output frequencies are as follows:

C1	R1 + VR1	Frequency
10nF	56kΩ	1kHz
10nF	560kΩ	100Hz
100nF	560kΩ	10Hz
100nF	56kΩ	100Hz
100nF	5k6Ω	1kHz

Note: 10nF (nanofarads) = 0·01μF (microfarads) and 100nF = 0·1μF.

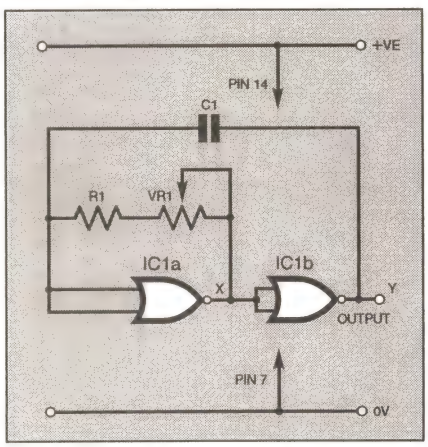


Fig. 4.2. Astable based on two NOR gates.

Be aware that the results shown are approximate and that this type of circuit should only be used if the exact frequency is unimportant.

In practice, select a total resistance (R1 + VR1) of between 4k7 and 1M ohms, and a capacitor in the range 56pF to 100µF. Electrolytic capacitors should have their positive ends connected to the output of IC1b. If capacitor values larger than 100µF (for lower frequencies) are required, use the "improved square wave oscillator" module described later.

If a fixed frequency is required, potentiometer VR1 may be omitted, connecting R1 between the input and output of IC1a.

STARTING AND STOPPING

It is often useful to be able to start and stop an astable circuit without switching off the power supply. The circuits in Fig. 4.3 show how the connections to one gate (IC1a) may be modified so that the gate is forced into one state ensuring that the circuit cannot oscillate.

The gate must be either a NOR or a NAND. Note that the logic levels at the control input and the output when "jammed" in Fig. 4.3a are opposite to those in Fig. 4.3b.

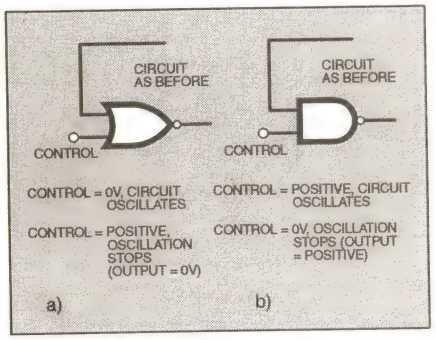


Fig. 4.3. Gated control for astable.

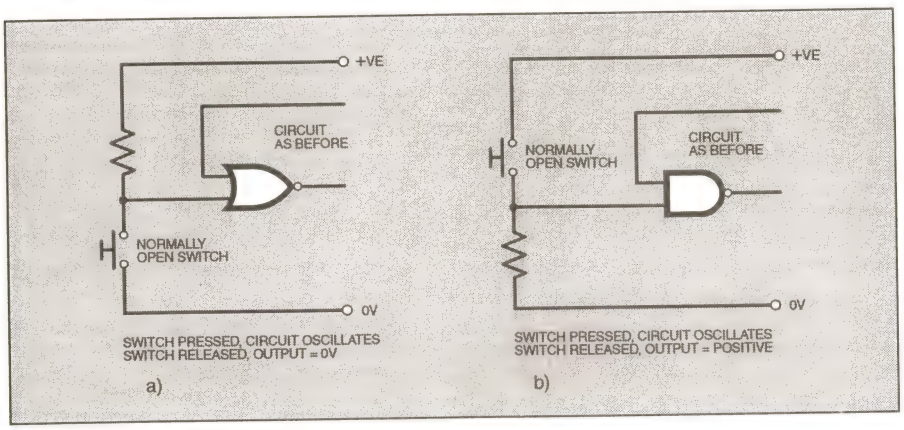


Fig. 4.4. Switched implemention for the circuit in Fig. 4.3.

As explained in Part 1, inputs to CMOS logic gates must *not* be left "open circuit". Consequently, the control input must be connected to a definite logic level, such as the output from another gate in the main circuit. Alternatively, switches may be used to control the logic level of the control input, as shown in Fig. 4.4.

The value of the biasing resistor is not critical and should be somewhere between 10k and 1M ohms.

Either of the two gates in the astable circuit of Fig. 4.2 may be controlled in this way. The choice of which is used will depend on the needs on the following circuit, and on the signal availability from the preceding circuit.

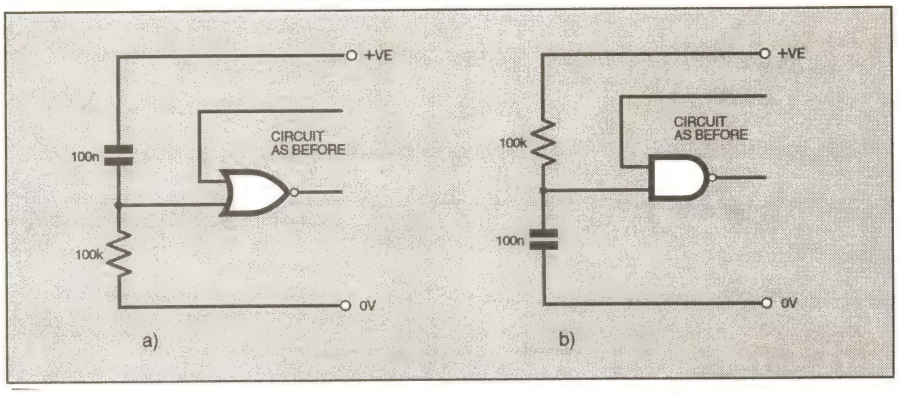


Fig. 4.5. Using a resistor and capacitor to "kick-start" an astable.

Note that the word *output* in Fig. 4.3 and Fig. 4.4 refers to the output of the gate under control, which may or may not be the final output of the astable. For example, if the gate under control is IC1a in Fig. 4.2, the output at IC1b will have the opposite logic level to that shown in Fig. 4.3 and Fig. 4.4.

KICK-STARTING

The circuit shown in Fig. 4.3 may not reliably start to oscillate when power is first switched on and may "jam" into one particular and unpredictable state. Adding one of the switched controls shown in Fig. 4.4 will solve the problem, although manual control is not always convenient.

A useful alternative is to add a resistor and capacitor to "kick-start" the circuit whenever power is applied, as shown in Fig. 4.5.

Referring to the NOR gate circuit in Fig. 4.5a, when power is first applied, the rising voltage at the top end of the capacitor (as seen in the diagram) causes a similar rise on the lower side, (see A.C. Coupling in Part 2). After a very short time, the voltage on the lower side will collapse as the charge leaks to 0V through the resistor. The action is similar to pressing the switch in Fig. 4.4, and the circuit jerks into action.

A similar, though opposite, effect applies to the NAND gate circuit. When first switched on, the voltage on the top side of the capacitor is zero. After a very short time enough current will have passed through the resistor to positively charge the capacitor to a logic 1 level. This is also like pressing the switch in Fig. 4.4.

A practical circuit, based on NOR gates and using the kick start method from Fig. 4.5, is shown in Fig. 4.6.

VOLTAGE CONTROL

It is sometimes useful to control frequency by a varying a voltage, rather than by mechanically setting a variable resistor. The circuit of Fig. 4.2 may be modified to allow simple voltage control as shown in Fig. 4.7.

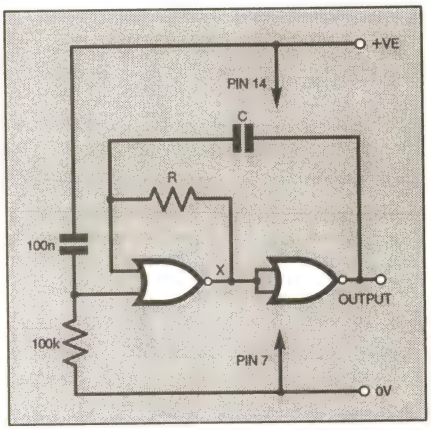


Fig. 4.6. A practical "kick-started" astable.

If the voltage control input is connected to 0V, the circuit will oscillate at its maximum frequency – as determined by the values of the resistors and capacitors. If the voltage control input is raised above 0V the frequency will be reduced, reaching its minimum when the voltage control is at half the supply voltage. If the control voltage is raised further, the frequency will increase again.

This circuit may be also be started and stopped using the control shown in Fig. 4.4 and Fig. 4.5, or kick-started when first switched on by the arrangement shown in Fig. 4.6.

These simple astable circuits sometimes produce "glitches" (unclean switching pulses) which can cause problems in counting circuits.

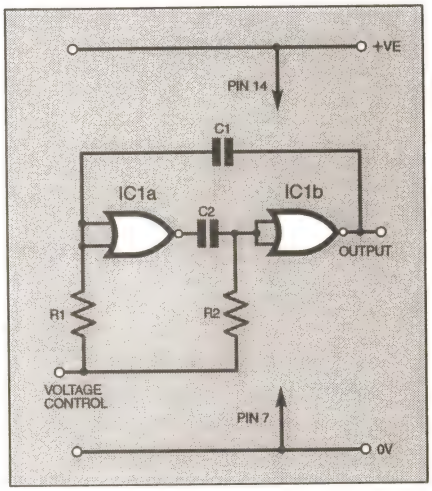


Fig. 4.7. Voltage controlled oscillator.

To sum up the astable circuits in Fig. 4.3 to Fig. 4.7:

ADVANTAGES:

Wide frequency range
Very low current consumption
Easy to interface (connect) to other modules

DISADVANTAGES:

Frequency is approximate, and tends to vary with the supply voltage
Output is quite a good square wave, but not perfect
Glitches may be produced, which could cause problems
Unreliable starting at power-up without additional controls

If a better square wave output without glitches is required, a third gate may be used as shown in Fig. 4.8.

in Part 3, it may be more convenient to measure R in megohms, and C in microfarads. For example:

if R = 330kΩ (= 0·33MΩ) and C = 0·1μF, then

$f = 1 / (8 \times 0{\cdot}33 \times 0{\cdot}1) = 3{\cdot}8Hz$

Note that in this, as in the previous modules, no resistor should have a value of less than 4·7kΩ or too much current will flow via a CMOS 4000 series output.

This type of circuit, with a Schmitt trigger at its heart, is known as a relaxation oscillator.

The circuit of Fig. 4.8 could be simplified by using a single 2-input Schmitt NAND gate, as shown in Fig. 4.9. The CMOS 4093 chip houses four 2-input Schmitt NAND gates, and the CMOS 40106 houses six Schmitt NOT gates (inverters).

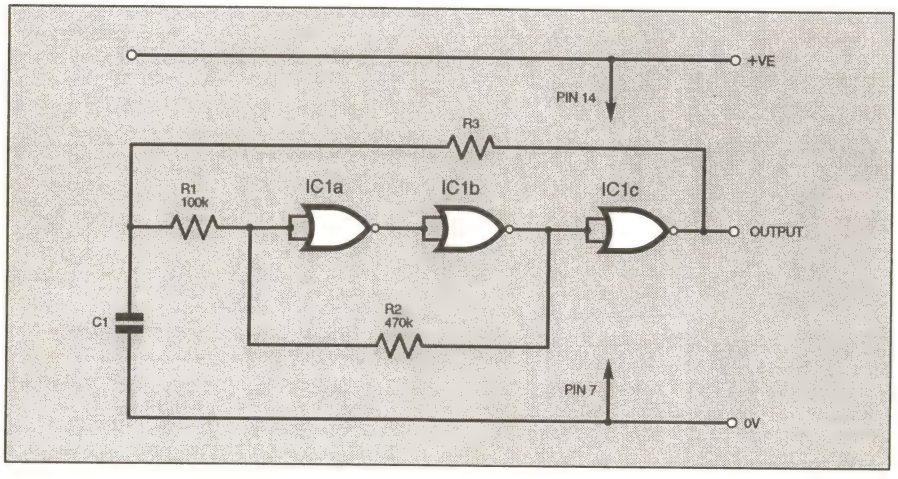


Fig. 4.8. A more reliable square wave oscillator.

IMPROVED SQUARE WAVE OSCILLATOR

An improved square wave oscillator circuit is shown in Fig. 4.8. As can be seen, a third NOR gate is required but the circuit always self-starts at power on, and produces a glitch-free output. Two considerable advantages!

The gates may be NORs as shown, or NANDs or NOTs. Any of the three gates (unless they are NOT gates) may be given the treatment shown in Fig. 4.3 and Fig. 4.4 to enable start/stop control.

The first two gates, IC1a and IC1b, together with resistors R1 and R2, make a non-inverting Schmitt trigger circuit (see Part 1). The third gate, IC1c, inverts the output voltage from IC1b feeding it back to capacitor C1 via R3.

Resistor R3 and capacitor C1 control the frequency of the module. For example, if R3 has a value of 10k and the capacitor a value of 10nF, then the frequency will be about 1.25kHz. If R3 and/or C1 are reduced in value, the frequency will increase proportionally.

Variable control of the frequency may be achieved by inserting a potentiometer, wired as a variable resistor, in series with R3. Note that the ratio of R1 to R2 will also have a small effect on the frequency.

In general terms, and assuming that the values of R1 and R2 are as shown in Fig. 4.8, the frequency will be given by:

$f = 1 / (8 \times R \times C)$

where, f = frequency, R = R3, C = C1

Remember that as in all such formulae, R should be measured in ohms, C in farads and f in hertz, although, as discussed

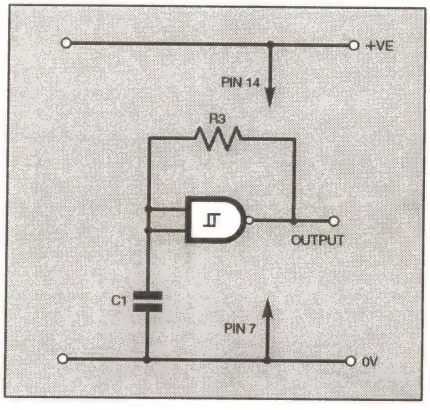


Fig. 4.9. Schmitt trigger oscillator.

To sum up the improved square wave oscillator circuits of Fig. 4.8 and Fig. 4.9:

ADVANTAGES:

All the advantages of the previous circuits (Fig. 4.2, Fig. 4.7)
Output is free of glitches
Single Schmitt gate can be used for Fig. 4.9

DISADVANTAGES:

An extra gate is required for Fig. 4.8
Frequency is slightly dependent on the supply voltage

OP.AMP OSCILLATOR

Like the last two modules, Fig. 4.8 and Fig. 4.9, the op.amp relaxation oscillator circuit shown in Fig. 4.10 is always self-starting at power on and provides an output free of glitches.

The frequency of the output depends upon the values of resistor R1 and

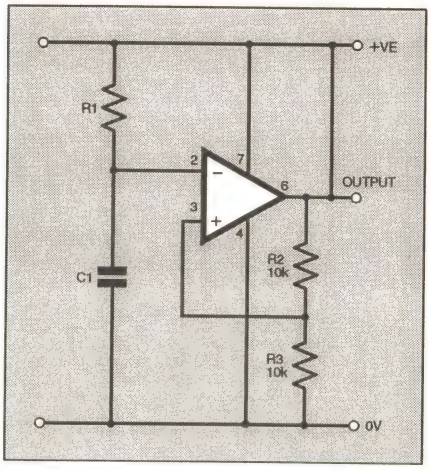


Fig. 4.10. Op.amp relaxation oscillator.

capacitor C1, and is given by the formula:

$f = 1 / (2{\cdot}2 \times R1 \times C1)$

where f is measured in hertz, R1 in ohms and C1 in farads.

As before, a more manageable combination of units is: R in MΩ, C in μF; f will still be in hertz. As an example:

if R1 = 470kΩ (= 0·47MΩ) and C1 = 0·22μF, then

$f = 1 / (2{\cdot}2 \times 0{\cdot}47 \times 0{\cdot}22) = 4{\cdot}4Hz$

The formula may be changed round if a particular frequency is required. For example, suppose a frequency of 2kHz (i.e. 2000Hz) is needed. Since the range of values of capacitors is limited, choose a capacitor value and then calculate the required resistor.

Selecting a capacitor with a value of 100pF (= 0·0001μF) and changing the formula round:

$R = 1 / (2{\cdot}2 \times f \times C)$

therefore, $R = 1 / (2{\cdot}2 \times 2000 \times 0{\cdot}0001) = 2{\cdot}27k\Omega$

In practice, select a 2·2kΩ (2k2) resistor, or use a 4·7kΩ (4k7) preset and adjust it for the correct frequency.

For many simple applications below about 20kHz, a type 741 op.amp may be used in the above circuit. For higher frequencies, other op.amps, such as the 748 or TL071, will provide good results. Low current CMOS versions of op.amps may also be substituted.

To sum up the op.amp relaxation oscillator in Fig. 4.10:

ADVANTAGES:

Uses a simple op.amp
Produces a stable, glitch-free output

DISADVANTAGE:

Output may not swing fully between power line levels
Uses more current than a logic gate i.c.

555 ASTABLE

The timer i.c. type 555 is specifically designed for monostable and astable circuits. When used as an astable, as shown in Fig. 4.11, it is another example of a relaxation oscillator.

Referring to the graph in Fig. 4.11, where T1 is the "mark" time in seconds, T2 is the "space" time and "Total T" is the whole period, then:

$T1 = 0{\cdot}7 (R1 + R2) \times C$
$T2 = 0{\cdot}7 \times R2 \times C$

and Total $T = 0{\cdot}7 \times (R1 + 2R2) \times C$

thus, $f = 1 / (0{\cdot}7 \times (R1 + 2R2) \times C)$

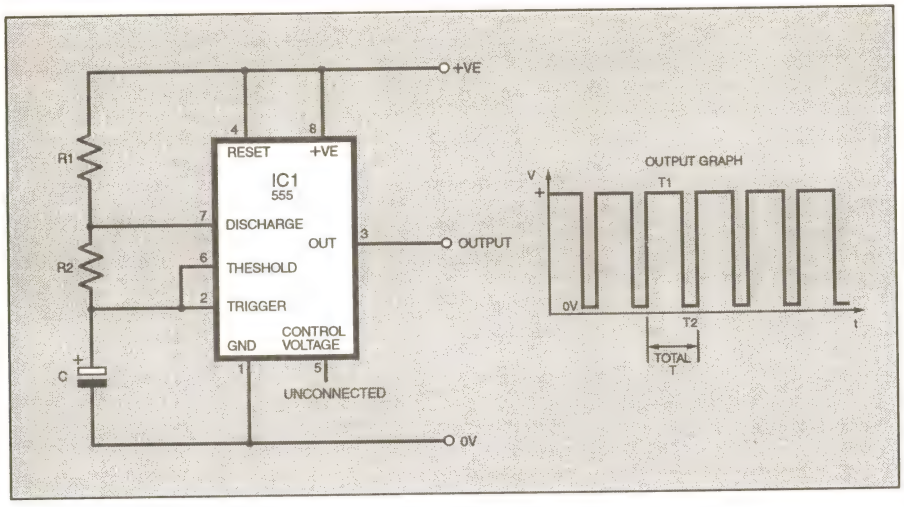


Fig. 4.11. A 555 astable and example output graph.

however, if R2 is much larger than R1 (e.g. R2 = 100kΩ, R1 = 4·7kΩ)

then, $f = 1 / (1{\cdot}4 \times R2 \times C)$

For example, suppose a value of 680kΩ is selected for R2, but R1 remains at 4·7kΩ. This would be a sensible choice since it results in the output having a nearly equal mark/space ratio, and the simple formula which ignores R1 can be used.

Using a capacitor of, say, 10nF and changing the units: 680kΩ = 0·68M and 10nF = 0·01μF

then, $f = 1 / (1{\cdot}4 \times 0{\cdot}68 \times 0{\cdot}01) = 105Hz$

Note that in Fig. 4.11 an electrolytic capacitor is shown, which is more suited to low frequencies. For higher frequencies, a non-polarised capacitor would normally be used.

The formulae above can be used to calculate:

Time period (T1) for which the output is positive
Time period (T2) for which the output is at 0V
Total time period (T1 + T2)
Frequency for all values of R1 and R2
Frequency formula simplified, if R2 is much larger than R1

Remember that if R2 is much larger than R1, the output wave has a nearly equal mark/space ratio (i.e. T1 = T2).

Some further example values and results are as follows (the answers are approximate):

R1	R2	C	f
4·7kΩ	100kΩ	0·001μF (1nF)	7kHz
4·7kΩ	100kΩ	0·01μF (10nF)	700Hz
4·7kΩ	1MΩ	0·01μF (10nF)	70Hz
4·7kΩ	1MΩ	0·1μF (100nF)	7Hz

If a variable frequency is required, replace R2 with a potentiometer wired as a variable resistor.

To sum up the 555 astable circuit of Fig. 4.11:

ADVANTAGES:

Easy to handle and use (standard version is not static sensitive)
Provides a stable frequency
Output can supply at least 100mA, and can drive small loudspeakers directly

DISADVANTAGES:

Standard version consumes more current than CMOS logic gates
Standard version can cause interference to other chips, e.g. counters
CMOS version is static sensitive

DECADE COUNTER AND CHASER

The Processor/Output module shown in Fig. 4.12 is based on the CMOS decade counter i.c. type 4017. Whenever its "clock input" (pin 14) is switched from 0V to positive, the i.c. counts up by one.

When the counter is in its reset condition, output Q0 (pin 3) is positive (high) and all the other outputs (Q1 to Q9) are at 0V. At each count, the currently high output pin returns to 0V and the next output pin in sequence switches high, in numerical Q order. When Q9 is high, the next clock pulse sets it low, and Q0 again goes high.

Note that the clock input must not be left "floating". It must either be connected to the output of another circuit, or be connected to 0V via a resistor of, say, 100k. Output pin 12, the CO (carryout) pin, is not used in this circuit and must not be connected to either power line.

In Fig. 4.12, outputs Q0 to Q9 are connected to l.e.d.s. Since only one l.e.d. is ever on at any time, a single series resistor is used to control their current.

Using the standard 4017, the l.e.d.s will not be very bright (although low current, high brilliance types could be used), since the outputs are not really designed for driving them, being capable of delivering very little current (see Part 1).

Alternatively, the 74HC4017 version could perhaps be substituted, which can deliver about 25mA per output pin. The l.e.d.s will be brighter, but this version of the counter *must* be used on a lower supply voltage. A *maximum* of 6V is permitted, although in practice it is safer to use a 4·5V battery, or a 5V regulated supply.

In reality, more current can probably be drawn from the pins of the standard 4017 than nominally allowed, although the output voltage level will fall accordingly. The subject of l.e.d. series resistors is discussed later, but assume now that a value of 220Ω for the resistor in Fig. 4.12 will probably be satisfactory when the circuit is powered at 12V.

Although the counter outputs are shown driving l.e.d.s, they may be used to drive other devices, such as transistors, if a larger output current is required. (See the section on *npn* drivers and Darlington drivers in Part 1.)

COUNTER RESETTING

Although the counter automatically resets back to zero on the tenth pulse, it is often desirable for it to be reset at an earlier point in the cycle. This may be achieved by using the counter's reset (RST) input pin 15. When pin 15 is connected to 0V the i.c. does not reset until each tenth pulse is received, but if pin 15 is made positive at any time, the counter will reset immediately (i.e. output Q0, pin 3, will switch high again).

There are several ways in which the counter can be reset. A manual reset control can be provided by a pushswitch, as shown in Fig. 4.13a. Normally, pin 15 is held at 0V via the resistor but when the pushswitch is pressed, pin 15 goes high, so resetting the counter.

In another situation, it may be required that the counter should be reset on a count

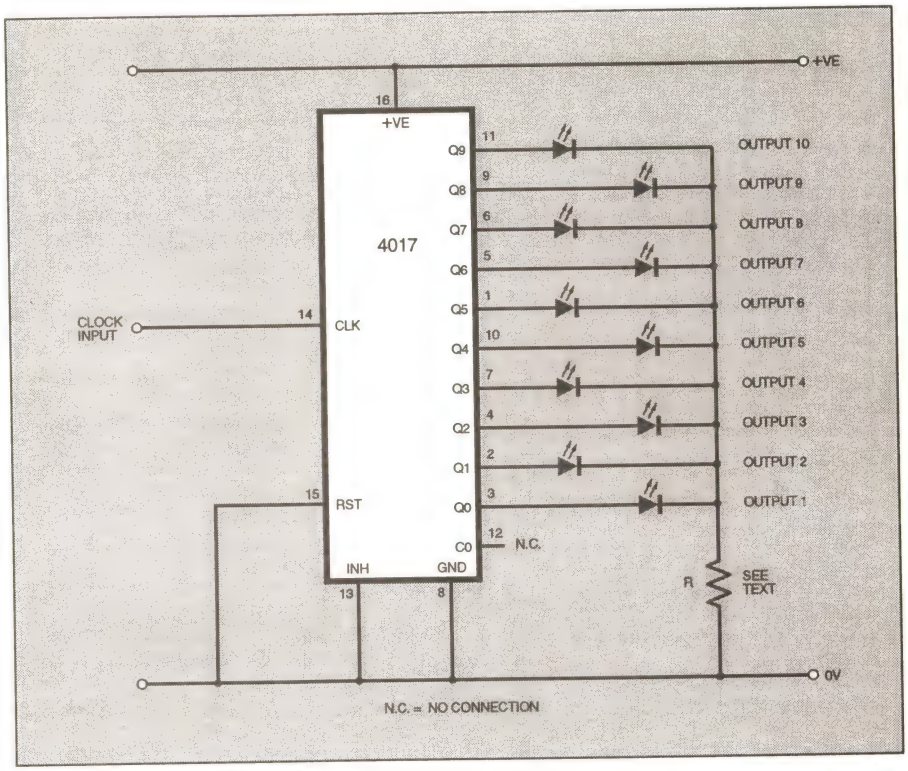


Fig. 4.12. Decade counter and chaser circuit.

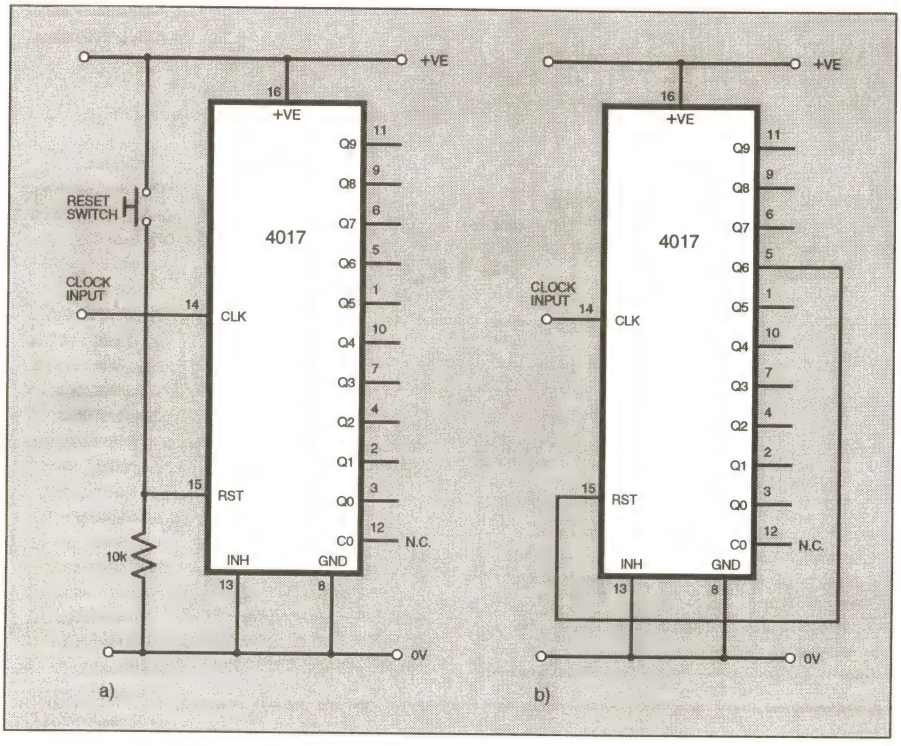


Fig. 4.13. Two methods by which the 4017 can be reset.

of six (for use as a dice indicator, for example). How this is done is shown in Fig. 13b.

The reset pin 15 is connected to the seventh output (Q6), which is normally at 0V. Starting from output Q0, the count proceeds upwards to output Q5, each output remaining high until the next clock pulse is received.

On the sixth clock pulse, though, output Q6 goes high, automatically resetting the counter back to zero via pin 15, and setting output Q0 high again. Consequently, output Q6 is only momentarily held high, a pulse period which is so short that it would be difficult to see it even on an oscilloscope.

CASCADING AND INHIBIT

A "carryout" function is provided via pin 12 (CO). It may be used to drive the clock input of a second counter if it is necessary to count up beyond nine. The use of this principle is illustrated in the *Vari-Speed Dice* project (see other pages).

An "inhibit" function is also provided on this type of counter, via pin 13 (INH). If this pin is taken high, the counter will cease to respond to clock pulses on its input pin 14, with the last-triggered output remaining high.

As soon as pin 13 is returned to 0V, the counter again responds to clock pulses as normal, continuing from the last output triggered. The inhibit function can be controlled by a switch in same way as shown in Fig. 4.13a.

L.E.D. SERIES RESISTORS

So far in this series, values for various l.e.d. series resistors have been suggested. These values were first calculated, and then the result was sometimes modified according to experience with a particular circuit.

For example, the 220Ω value for the resistor in Fig. 4.12 is actually much lower than calculation would suggest, due to the output resistance within the i.c. Even so, the method by which values are calculated is fairly straightforward and provides a good starting point in selecting a resistor value. First, though, consider why a series resistor is actually needed.

When a *bulb* is connected to a power supply, as in Fig. 4.14a (in this case a 12V bulb and a 12V battery), the circuit will function satisfactorily. However, if an *l.e.d.* is substituted for the lamp, as in Fig. 4.14b, the l.e.d. will glow briefly and then die. Before it dies, though, it passes so much current that a small battery could quickly run down.

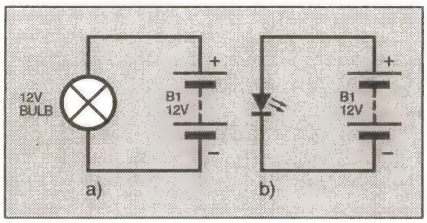


Fig. 4.14. The bulb circuit (a) will work happily but the l.e.d. in the other circuit (b) will die rapidly.

The reason is that a bulb has resistance and will pass an amount of current according to Ohm's Law:

$$I = V / R$$

The formula shows that the amount of current (I) depends up on the resistance (R) of the bulb and the voltage (V) across it. Once the bulb filament has reached its working temperature, its resistance is fairly constant and the current flowing depends only upon the voltage.

An l.e.d. is quite different. It is a diode which, in the direction that current can flow through it, has little appreciable resistance.

As stated in Ohm's Law, when resistance (R) is very small, the current (I) flow through it is very large. Consequently, the 12V battery in Fig. 4.14b causes a great deal of current to flow through the l.e.d., although the current will also be slightly limited by the additional resistance of the wires linking the l.e.d. to the battery, plus the internal resistance of the battery itself.

FORWARD VOLTAGE

There is a complication which arises regarding the calculation of current flow through an l.e.d. Although l.e.d.s can be said to have no appreciable resistance to current flow, a voltage difference, known as the *forward voltage drop*, exists across the l.e.d. when current flows through it.

The forward voltage drop varies slightly with different types of l.e.d., but is typically about 2V. In one sense, then, an l.e.d. *does have* significant resistance, but only to the first 2V or so of its supply voltage. It is therefore difficult to make a simple statement about its resistance and to apply this conventionally to Ohm's Law.

However, if an l.e.d. has a forward voltage drop of 2V, then the 12V battery in Fig. 4.14b can be likened to a 10V battery connected to a short-circuit. Both components will be very unhappy!

A good catalogue will state the forward voltage drop (V_f) of the l.e.d. being selected. Typically, the V_f for standard red l.e.d.s ranges from about 1·8V to 2V; other colours may range from 2V to 2·2V. However, if a forward voltage of 2V is assumed, calculation results will be accurate enough.

RESISTOR CALCULATION

Since an l.e.d. does not have resistance in the normal sense, a resistor has to be connected in series between it and the power supply to limit the current flow to a safe level, as shown in Fig. 4.15.

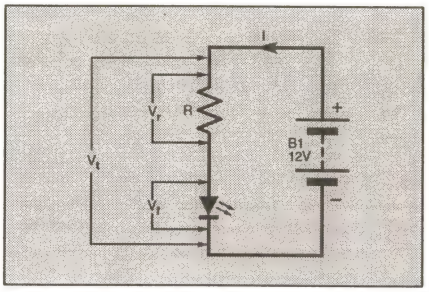


Fig. 4.15. Using a current-limiting resistor in series with an l.e.d.

To calculate the value of the resistor (R) the following information is required:

Total voltage applied (V_t)
Forward voltage drop (V_f) across the l.e.d.
Current required through the l.e.d. (I)

In the example shown in Fig. 4.15, V_t is 12V and V_f is 2V. A catalogue will state the maximum current which can be permitted to flow through an l.e.d. Standard types require around 10mA to 20mA, although low current types are available which typically require 2mA, but these are more expensive. Currents less than the maximum can be used, although the brilliance of the l.e.d. will diminish accordingly. For this example, a current of about 15mA is desired.

Because the resistor in Fig. 4.15 is in series with the l.e.d., the current flow through the l.e.d. will be equal to the current flow through the resistor, in this case, about 15mA.

The forward voltage drop across the l.e.d. (V_f) is taken as 2V, and the voltage across the resistor (V_r) is the total voltage (V_t) less V_f.

thus, $V_r = V_t - V_f$

therefore, $V_r = 12 - 2 = 10V$

So, in the example, the voltage across the resistor is 10V. If the voltage across a resistor and the current flowing through it

are known, the required resistance value can be calculated using Ohm's Law:

$R = V / I$

Note that V must be in volts, I in amps, and R in ohms. The current of 15mA should be re-written as 0·015A, therefore:

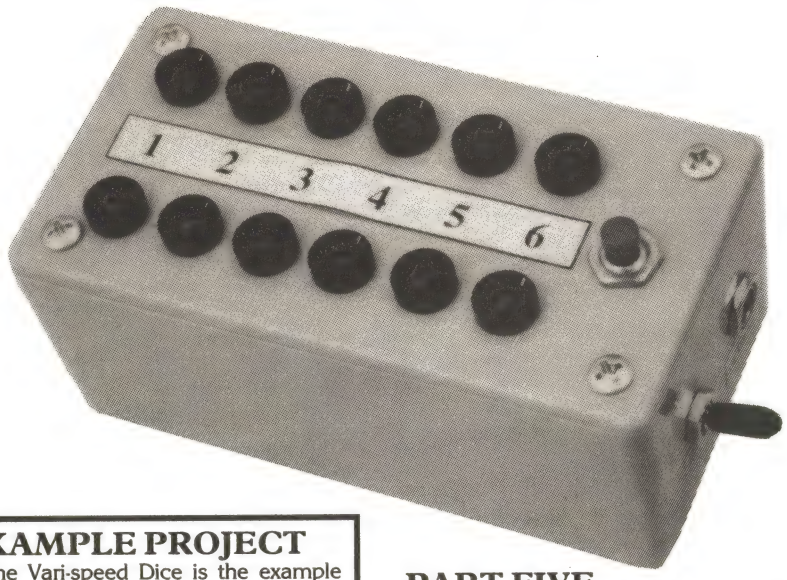
$R = 10 / 0{\cdot}015 = 667\Omega$

The standard resistor value nearest to 667Ω is 680Ω. This represents a good choice since the l.e.d. will be quite bright on a total voltage of 12V. Remember, though, that increased brilliance requires more current and results in a shorter battery life.

NON-STANDARD L.E.D.S

The calculations above apply to ordinary cheap l.e.d.s. It is possible to buy l.e.d.s which have a built-in resistor (although they cost more), in which case either a 5V type or 12V type must be selected, as appropriate.

Flashing l.e.d.s have an integral i.c. and are designed for a particular voltage range. Providing the voltage is within that range, the i.c. regulates the current supplied to the l.e.d. without the need for a series resistor.



EXAMPLE PROJECT

The Vari-speed Dice is the example project (elsewhere in these pages) which shows how the modules in *Teach-In* Part 4 can be combined in a practical application.

PART FIVE

The modules to be examined in *Teach-In* Part 5 are an I.R. receiver, encoder/decoder, bistables and a pulsed Darlington output. The example project is an Infra-Zapper.

Ohm Sweet Ohm

Max Fidling

Snowbound

I'm often amazed how the United Kingdom grinds to a complete halt when the first seasonal snowflakes land on our island. An inch is enough to close motorways and cause all sorts of national catastrophes and disasters – all of which, though, pale into insignificance compared with the time the Fidling household experienced a sudden shortage of tinned cat food for you-know-who!

Having received my marching orders from the Boss, I'd ventured out on a treacherous snowy pavement to the nearby corner shop, to purchase some tinned grub for my mange-tout moggie. What I would do for one of those snow scooters I'd seen on the telly! (A funny place to keep a snow scooter, I know.)

The biting wind did nothing to cheer my soul on this wintry day, as I shuffled home carrying a plastic bag of clattering tins of cat food, plus a packet of chocolate biscuits with which I'd decided to treat myself.

Hence, today saw me stuck in the workshop, which had donned a wig of freshly fallen snow. Inside the 'shop, though, the electric fan heater was blasting out three kilowatts of glorious heat, with myself and Piddles (my pesky puss) toasting nicely.

I was slowly thawing out after my expedition while Piddles was scoffing merrily away, clattering his plastic bowl on the floor of the shack oblivious to the fact that I'd nearly succumbed to terminal frostbite purely for his benefit (or so it felt like).

Thermal Contact

Upon my return I had been duly honoured with a mug of tea which I slurped appreciatively, whilst pondering whether there was any similarity between the name of my companion and the flavour of the tea ... Dunking a biscuit in my cuppa, (one of my uncouth habits, I'm afraid), half of the soggy bikky suddenly fell into the tea with a "ploop". I polished off the cheering brew with a gulp.

As you'd expect, the electric fan heater had not escaped the attention of my electronic meanderings. I'd recently completed an electronic thermostat project which I'd seen published in the magazine; my new temperature-sensitive gizmo sat there on the bench, with a thermistor probe stuck unceremoniously to the wall with Blu-Tak and the fan heater plugged into a mains socket mounted on top of the housing.

The heater whirred away, providing a handsome level of heat, and an l.e.d. on the panel glowed benignly as a confirmation that all was well with this negative tempco contraption ... Or so I hoped!

The trouble with dinner time is that I have to make it back to the house, leaving the cushy comfort of the snug 'shop, rather an inconvenience but you can't have everything these days, I sighed. At least we had an intercom between the workshop and the kitchen, another project I'd made recently and installed using a part drum of surplus 15A three-core cable. You could probably route a city's entire telephone exchange down the cable but never mind!

The intercom performed magnificently as the Boss summoned me to chow time. I reckoned Piddles would be safe enough in the shack, and I left the heater blazing merrily away so that all would be cosy upon my return.

Taking the Biscuit

About an hour later, and feeling suitably full of scrummy Yorkshire Pudding with gravy, I sneeked out and slithered back to my bolt-hole in the back garden. The menacing moggie had sprung onto the bench and was peering out at me through the window, tail swishing, having spotted some birds pecking away at the bird nut feeder I'd nailed up outside.

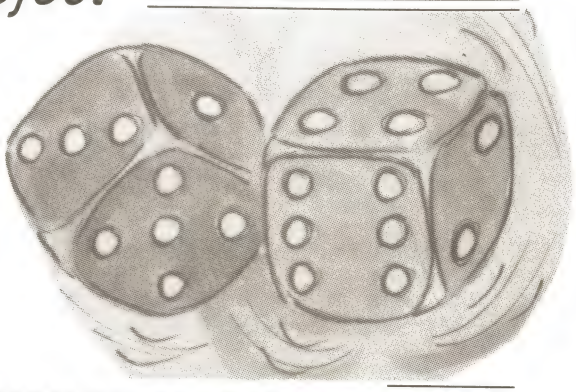
Not wanting to see my feathered friends dashed to ribbons at the paws of my marauding moggie, I quickly nipped through the door which I bolted firmly shut behind me! A certain fragrance greeted my nostrils ... a sort of biscuity, chocolatey kind of odour (I always thought I'd make a good wine buff) which I wanted to eat, it smelled so good!

Looking down at the floor, I could see the remains of several of my favourite chocolate biscuits which that dang-nabbing cat had snaffled! Piddles looked at me innocently, with his "Who, Me?" kind of expression: I glared back with my "Yes! You!" evil stare.

Worse still, the cocoa-flavour pong was traced to the pack of biscuits which he'd knocked over in front of the fan heater, where the blow-torch breath of the heater had melted the biscuits together into a chocolate digestive brick!

Undeterred, and not wanting to waste good food, I grabbed the freezer aerosol from the shelf above and I sprayed the outermost packet liberally. Whether it was entirely foodsafe I wasn't sure, but a deft application of a one-inch woodworking chisel separated the amalgamated sweetmeats inside into pieces which Piddles and I started to scoff between us, whilst peering out of the window wondering what we'll do next for entertainment.

VARI-SPEED DICE



MAX HORSEY

PCB DESIGN BY ALEX SIMM

When the chips are down, let them shake, rattle and roll out your fate. Illustrates how Teach-In Part Four might be applied.

THIS project is based on the information provided in *Teach-In* Part 4 and shows how modules may be selected and combined to produce a working project.

The Vari-Speed Dice includes a simple l.e.d. display, formed around two rows of six l.e.d.s which "chase" before stopping at "random". A novel feature of the circuit is that instead of the display stopping abruptly it gently slows to a halt, rather like a roulette wheel, thereby adding to the excitement if a particular number is required.

Making electronic circuits "random" is very difficult since any monostable or timer module will use a fixed time sequence. The project therefore relies upon a simple timer, plus the time for which the Start button is held down. The human factor adds the required degree of randomness!

BLOCK DIAGRAM

A block diagram of the modules required to make up the circuit is shown in Fig. 1. When the start button is pressed and held down, the timer causes the astable to start at full speed. The square wave from the astable drives the first counter/l.e.d. driver module, which causes six l.e.d.s to flash in sequence.

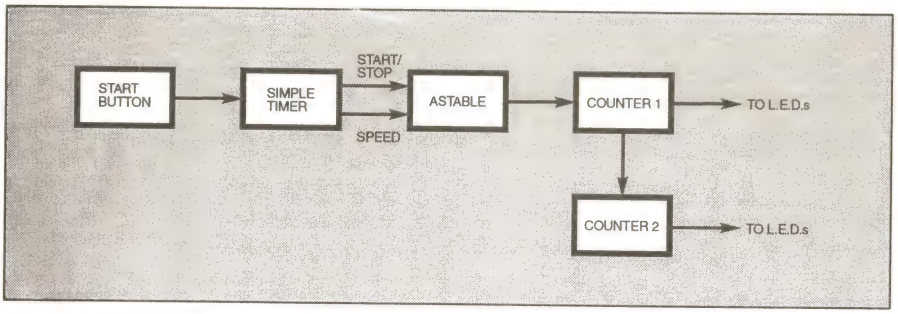


Fig. 1. Block diagram for the Vari-Speed Dice.

The same output from the astable could be used to drive the second counter, but this would make the l.e.d.s always stop at the same pairs. A second astable, set at a different speed would solve the problem, but this would necessitate the use of another i.c.

A more obvious way of driving the second counter is from the "carry" output of the first counter. In other words the second counter moves one step for every six steps of the first. The result is just as random as using two astable modules.

CHOOSING THE MODULES

The complete circuit diagram for the Vari-Speed Dice is shown in Fig. 2.

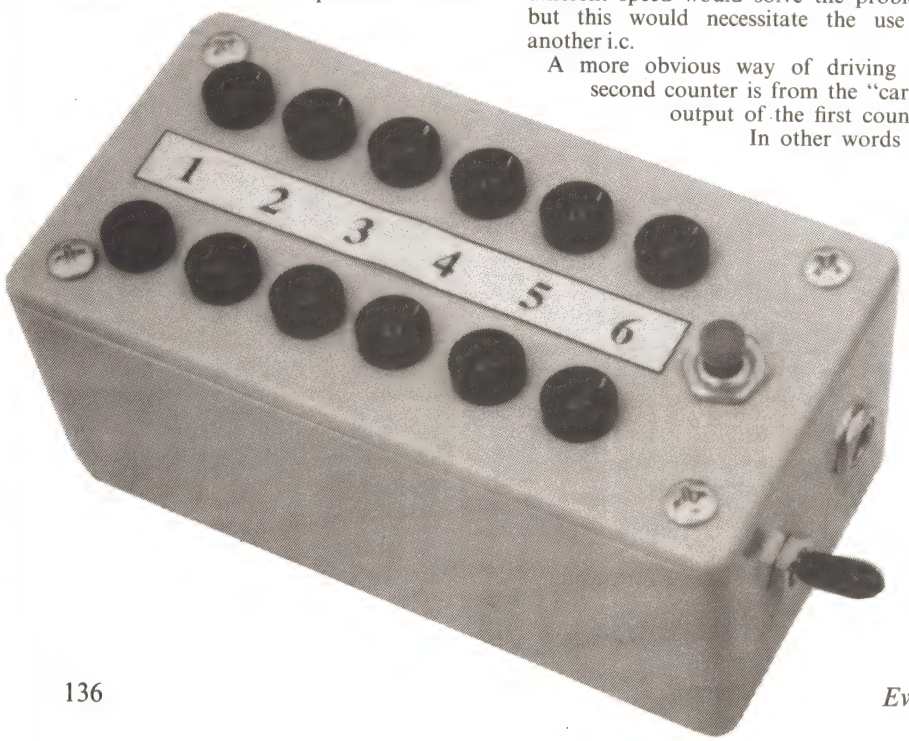
The Timer is based on the Simple Capacitive Delay module described in *Teach-In* Part 2 (Fig. 2.3). When the Start switch S1 is pressed, capacitor C1 is discharged. When S1 is released, C1 charges up slowly via resistor R1. The values of R1 and C1 determine the speed with which the voltage across C1 rises – higher values equals longer time.

A slowly changing voltage is often a nuisance in logic circuits, many of which require a sudden change from logic 0 to logic 1. However, in this design the slowly rising voltage is put to good use in controlling the speed of the astable.

VOLTAGE CONTROLLED ASTABLE

A number of astable modules are outlined in *Teach-In* Part 4. The one chosen for use here is the Voltage Controlled Frequency module of Fig. 4.7, which has its frequency (speed) varied by changing the voltage on the two input resistors, R2 and R3 in Fig. 2. This circuit does not provided a "glitch- free" output, but this is of no consequence since any glitches which cause the counter to move one step more than expected will add to the randomness.

In Fig. 2, the astable is formed around two NOR gates, IC1c and IC1d. Its basic frequency is determined by the values of resistors R2 and R3, and capacitors C2 and C3 (larger values = lower frequency). Their values have been chosen to set the



oscillator speed to make it impossible to predict the outcome of the count. (If the value of C2 were to be increased to 100nF the speed would be just slow enough to allow a sharp contestant to fix the result by releasing the button at a particular moment.)

A method of switching an astable on and off by controlling the voltage at one of the pins was also discussed in Part 4 (Fig. 4.3). The technique is used here in the circuit of Fig. 2, IC1c pin 9 being the on/off input, which is controlled by the output from IC1b pin 4. When IC1c pin 9 is held high (made positive) the astable stops oscillating.

Referring to IC1a and IC1b, when the voltage at the junction of R1 and C1 is low, pins 1 and 2 will be low, consequently pins 3, 5 and 6 will be high and pin 4 low. In other words, output pin 4 merely copies the logic on input pins 1 and 2. Using a pair of gates in this way provides a cleaner voltage change at IC1c pin 9 than would be the case if the pin was connected directly to C1.

When switch S1 is pressed, the voltage at the positive side of capacitor C1 falls to zero and, as a result, IC1c pin 9 also goes low. Since the lower ends of resistors R2 and R3 are also connected to C1, and thus also at 0V, the astable oscillates at its maximum speed (as discussed in Part 4).

As C1 charges, the voltage at its junction with R2 and R3 rises, causing the astable to slow down. When the voltage across C1 reaches half the supply voltage, the astable is at its minimum speed. Then, as this voltage crosses the half way level, the logic at IC1b pin 4 changes from low to high, causing the astable to stop oscillating.

COUNTER/ CHASER

The l.e.d. counter/chaser circuits are based on those discussed in Part 4, Fig. 4.12 and Fig. 4.13, using a CMOS 4017B decade counter. Essentially, both counters are identical and are formed around IC2 and IC3. Each is connected so that it counts from one to six, then resets to one again at the next clock pulse.

Counter IC2 is "Clocked" on its input pin 14 by the output pulses from IC1d pin 11 of the astable. Pulses from the "Carry Out" pin 12 of IC2 provide the clock pulses for counter IC3.

On both IC2 and IC3, Reset pin 15 is connected to output pin 5, which is the seventh output (Q6). Consequently, each i.c. counts from the first output (Q0), through outputs Q1 to Q5, then resetting back to Q0 immediately the count reaches output Q6.

Each output is connected to an l.e.d. Since only one l.e.d. can be on at any one time, a single series resistor, R4 for IC2 and R5 for IC3, is used to control the current. The current available from each output

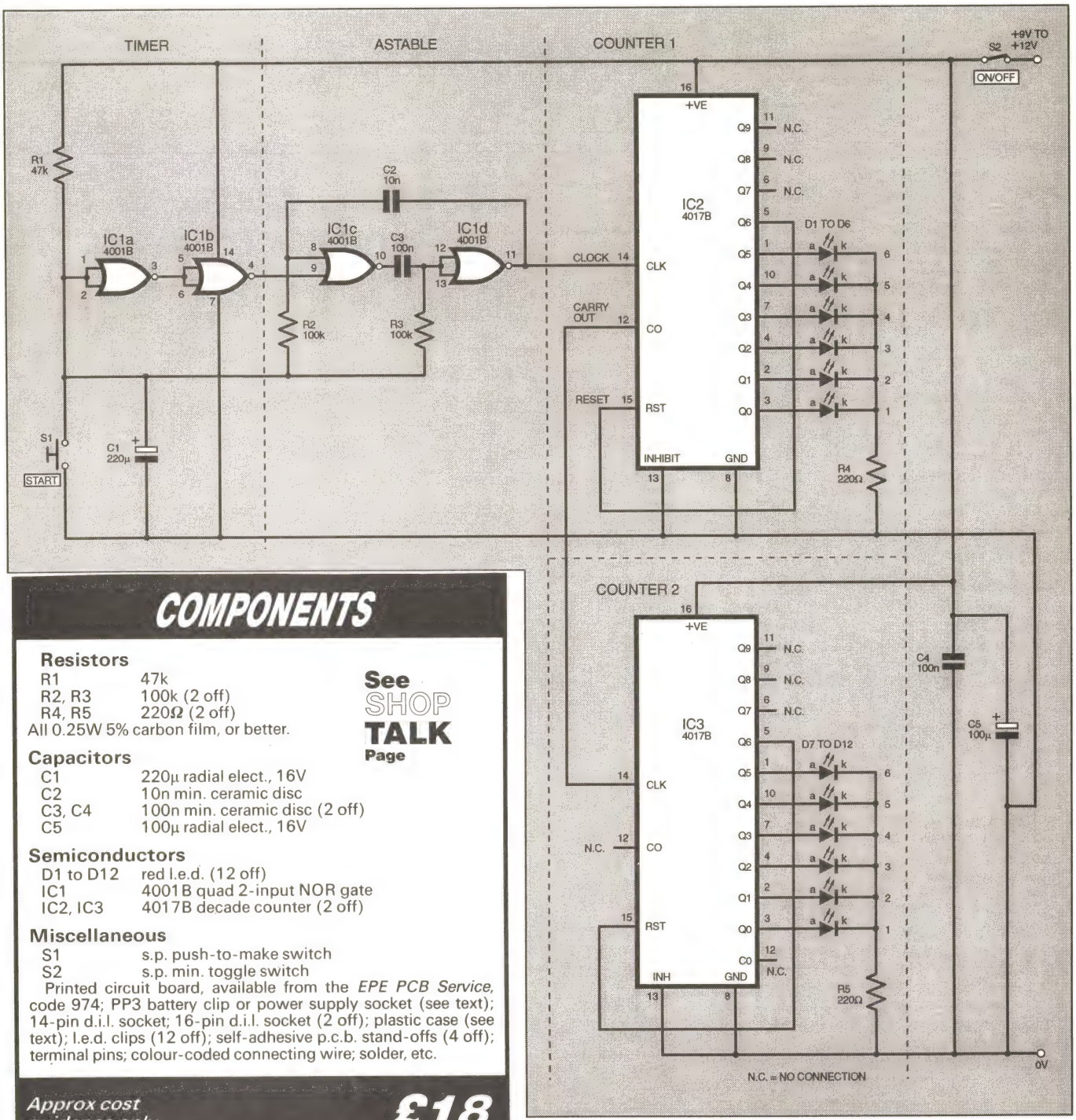


Fig. 2. Full circuit diagram for the Vari-Speed Dice.

COMPONENTS

See SHOP TALK Page

Resistors

R1	47k
R2, R3	100k (2 off)
R4, R5	220Ω (2 off)

All 0.25W 5% carbon film, or better.

Capacitors

C1	220µ radial elect., 16V
C2	10n min. ceramic disc
C3, C4	100n min. ceramic disc (2 off)
C5	100µ radial elect., 16V

Semiconductors

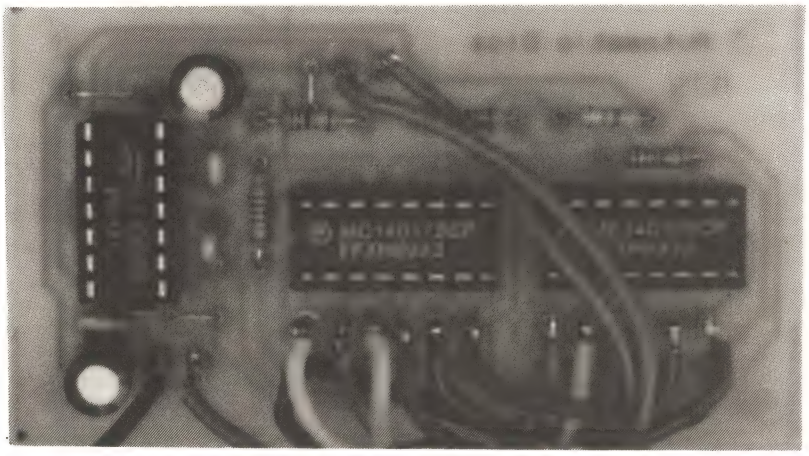
D1 to D12	red l.e.d. (12 off)
IC1	4001B quad 2-input NOR gate
IC2, IC3	4017B decade counter (2 off)

Miscellaneous

S1	s.p. push-to-make switch
S2	s.p. min. toggle switch

Printed circuit board, available from the *EPE PCB Service*, code 974; PP3 battery clip or power supply socket (see text); 14-pin d.i.l. socket; 16-pin d.i.l. socket (2 off); plastic case (see text); l.e.d. clips (12 off); self-adhesive p.c.b. stand-offs (4 off); terminal pins; colour-coded connecting wire; solder, etc.

Approx cost guidance only **£18**



Completed printed circuit board.

is rather small, and the i.c. is not really designed for driving l.e.d.s directly. However, with a supply of 9V or 12V (from, say, a mains adaptor) the l.e.d.s are more than adequately lit.

If extra brightness is required, special low-current l.e.d.s are available. Alternatively the CMOS 4017B could be replaced by the 74HC4017 which has a much higher output current, but *MUST NOT* be used on a supply of *MORE* than 6V. The subject of CMOS output currents and l.e.d. series resistors is referred to in Part 4.

Capacitors C4 and C5 provide the required power line decoupling, as discussed in Part 1. Switch S2 is a power supply On/Off switch, particularly important if a battery is used to power the circuit.

CONSTRUCTION

Details of the printed circuit board (p.c.b.) and its connections for the Vari-Speed Dice are shown in Fig. 3. This board is available from the *EPE PCB Service*, code 974.

Fit the two short wire links (not the connecting wires), followed by the i.c. sockets and resistors. Now fit the small ceramic disc capacitors. The labelling of these can sometimes be confusing. Note that if the legend "103" is printed on the capacitor body it means the capacitance value is 10nF (0·01μF) and that "104" means 100nF (0·1μF).

To some readers, this may seem quite illogical. However, "103" actually translates like a resistor colour code, namely, "one", "zero" plus "three" more zeros, i.e. 10,000, measured in picofarads (pF). Clarifying further:

$1F = 10^6\mu F = 10^9 nF = 10^{12} pF$

Capacitors C1 and C5 are electrolytic and must be fitted the correct way round. The negative end is normally printed on the body; the positive end is indicated by a longer lead.

Solder terminal pins into the p.c.b. for all the external connections.

The p.c.b. allows the l.e.d.s to be mounted directly to it, if preferred. However, in the prototype, the l.e.d.s were mounted on the case lid and linked to the p.c.b. with wires. It is *much* easier to mount the l.e.d.s in the case *before* connecting them to the circuit.

If this is the chosen method, note from Fig. 3 that the l.e.d. anodes (a) have separate wires connecting back to the board. The l.e.d. cathodes (k), however, are soldered to each other in two groups, each group is then connected to the board via a single wire.

HOUSING THE DICE

The prototype was used with a 12V battery eliminator (mains adaptor) and was housed in a plastic case measuring 104mm × 53mm × 44mm. Although the circuit can be powered by a 9V battery, note that a PP3 battery will not easily fit into this size of box.

As seen in the photographs, l.e.d.s were mounted in two straight lines. Alternatively, two circular arrangements could be used. When marking out the positions of the l.e.d.s, allow room for their mounting clips. Although the l.e.d.s could be inserted directly into the case, the use of clips makes the mounting task easier and provides a much neater finish.

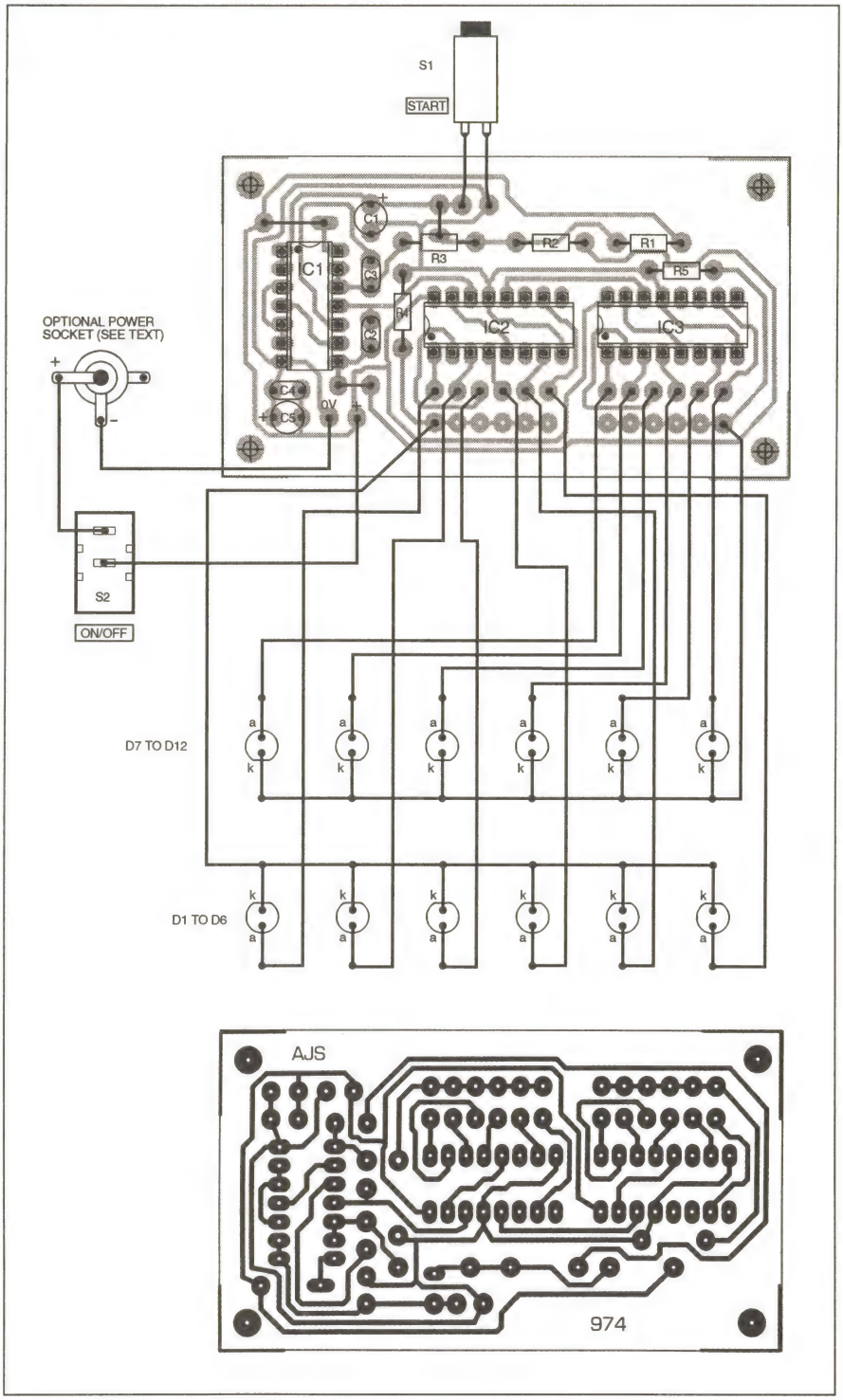


Fig. 3. Printed circuit board component layout, interwiring and full size underside copper foil master pattern. The spare copper pads, below IC2/IC3, can be used for direct *board mounting of the l.e.d.s.*

Mark the positions of the Start pushbutton switch, On/Off switch and Power Input socket, if required. Drill the holes, taking particular care to get the l.e.d. holes in line – even if just one l.e.d. is not exactly in line the appearance is spoilt. It helps if a very small drill is used first.

Position the l.e.d.s into their clips ensuring that the cathode (k) leads are all facing the same way as shown in Fig. 3. This makes the common cathode (k) connections much simpler to arrange. The cathode side of an l.e.d. is usually the shorter lead. If the leads have been cut, note that the cathode of a round l.e.d. is likely to be denoted by a tiny flat mark at the base of the body.

Now connect and solder the l.e.d. cathodes using a length of *bare* wire. This common junction is connected to the p.c.b. using a length of *insulated* wire.

Use colour coded insulated wire to link the l.e.d.s to the terminal pins. In other words, use a black lead for the common cathode connection, a brown lead for l.e.d. D1, red for D2, orange for D3, etc. Using coloured leads in resistor colour code order greatly eases assembly, particularly if fault finding is necessary.

The l.e.d. leads should be shortened before soldering and bent neatly against the plastic body of the case after soldering.

Complete the external wiring. Discharge static electricity from your body before handling the i.c.s, by touching a grounded item first. Then insert the i.c.s into their sockets ensuring that their orientation notches line up as shown.

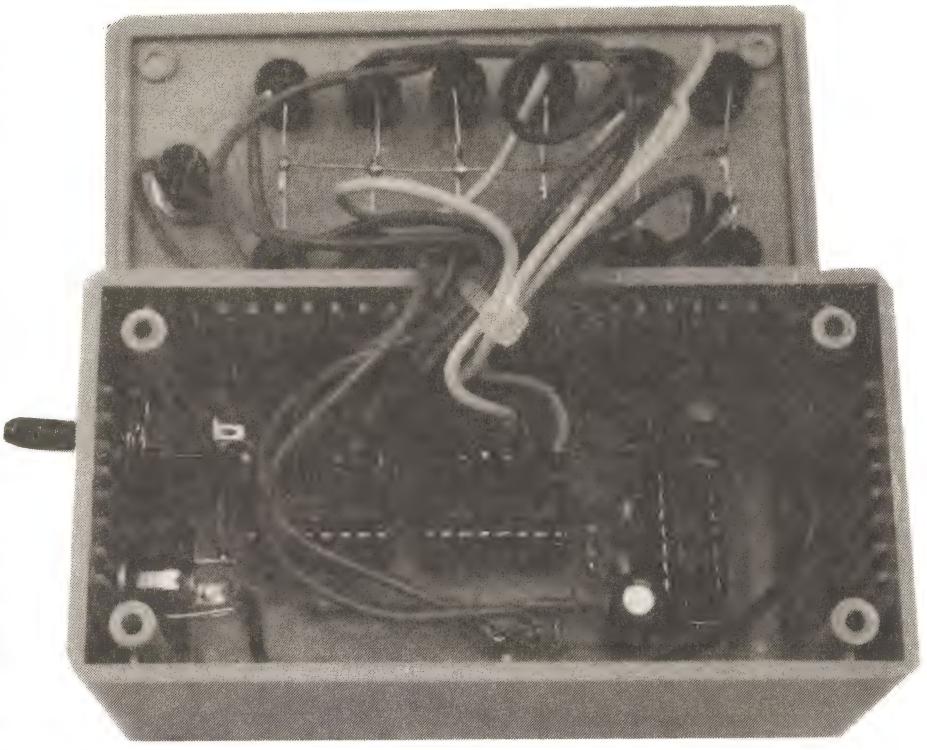
Now thoroughly check the board with a magnifying glass, ensuring that components are correctly positioned and that all solder joints are correctly made.

TESTING

A regulated 9V or 12V supply which can be limited to a maximum output current of 100mA is ideal for testing, and will be unlikely to harm the circuit even if major mistakes have been made.

Connect the supply, switch on S2, and check that one l.e.d. of each set lights up. If this does not happen, switch off and recheck for mistakes.

If all is well, press switch S1. The l.e.d.s should chase, with one set chasing six times faster than the other. Release S1. After a brief pause, the chase should slow down and finally stop. The pause length may be shortened by reducing the value of either resistor R1 or capacitor C1.



The p.c.b. is positioned on the base of the box with self-adhesive stand-offs. Take care that the lid mounted components do not short on the p.c.b.

FAULT FINDING

If the circuit does not behave as expected, decide first if the fault affects the whole circuit, or just one module and if so, which one. For example, measure the voltage across pins 7 and 14 of IC1, and across pins 8 and 16 of IC2 and IC3. If a voltage reading equal to that of the power supply is present, and with the correct polarity, check each module as described below. If not, check that the power socket has been connected correctly and that there is a voltage across it.

Read the fault finding guide in Part 1 of the series for general help, and using a voltmeter with its negative side connected to 0V in the circuit try the following tests:

When S1 is pressed, the voltage at IC1 pins 1 and 2 should be 0V. When S1 is released this voltage should rise to the maximum power supply level. The voltage at IC1 pins 3, 5 and 6 should be equal to the positive supply when S1 is pressed, switching to about 0V a few seconds after S1 is released. IC1 pin 4 should do the opposite of pin 3. Check that the voltage on IC1 pin 9 copies that on IC1 pin 4.

Correct operation of the astable can only be checked with the aid of an oscilloscope: a square wave should be seen at IC1 pin 11 and IC2 pin 14.

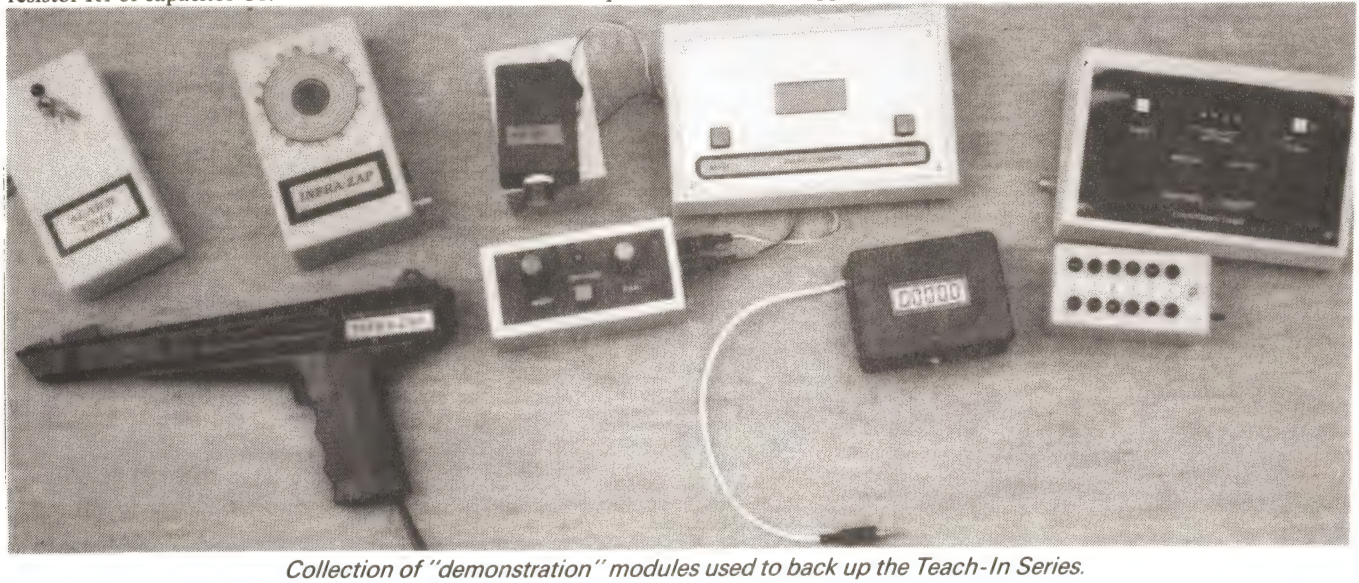
Failure of all the l.e.d.s is likely to imply that they are connected the wrong way round or the common connection between their cathodes and the p.c.b. has been forgotten.

INSTALLATION

The p.c.b. may be fastened to the base of the case using self-adhesive p.c.b. supports. Check that when the lid is positioned, a short circuit cannot occur between exposed parts on the p.c.b. and the bare l.e.d. wires. Screw the lid into position, and give the project a final test. □

PART FIVE

Next month an Infra-Red Zapper construction project will be the subject of *Teach-In* Part Five.



Collection of "demonstration" modules used to back up the Teach-In Series.