PRECISION JFET OP-AMPS IN PLASTIC

Dallas TX.

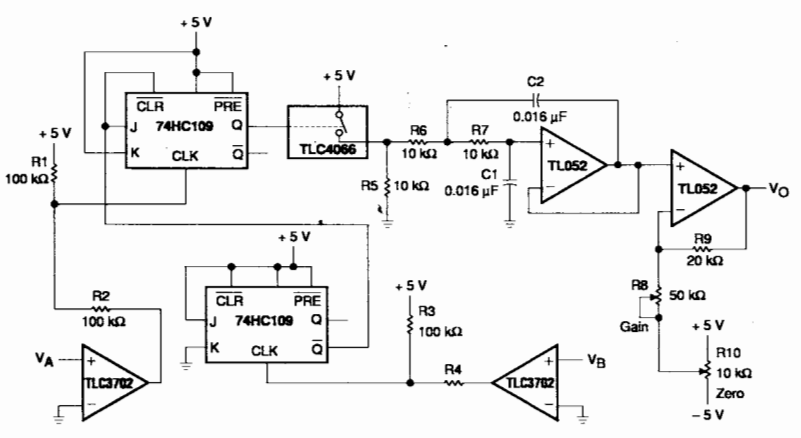
A complete family of Enhanced-JFET precision op amps with a very low input-offset-voltage specification that remains stable over time and temperature is available from Texas Instruments. Single, dual and quad op amps are offered in both a high-speed and a low-power series.

Because JFET op amps employ junction field-effect transistors in their differential input stages, they provide higher slew rates and lower input-bias-current requirements than standard bipolar devices. However, JFET op amps also have higher input-offset voltages that drift significantly over time and temperature. Precision JFET op amps, which have stable offset voltages, have been especially difficult to produce. Until now, precision JFETs available in volume have been singles packaged in metal cans.

The new TI high-speed Enhanced-JFET precision op amps are designated the TL050 series. The corresponding low-power op amps are designated the TL030 series.

Each of the new monolithic devices is pin-compatible and functionally compatible with industry-standard JFET op amps and can be used in upgrades to existing systems as well as in new designs.

This phase meter circuit, which uses TI's Enhanced JFET TL052 op amps, operates from 100 Hz to 10 kHz producing 10 mV per degree of phase delay between V_B and V_A. R8 and R10 provide output gain and zero calibration.



Digital phase meter updates measurement each cycle

by R. E. S. Abdel-Aal
Department of Electronic Science, University of Strathclyde, Glasgow, Scotland

Because this meter measures the phase delay between two low-frequency square waves once every cycle, it is useful in applications where instantaneous readings of this delay are continuously required. The circuit resolution is within 1% for signal frequencies of up to 250 kilohertz.

Generally, the meter counts the number of pulses of a 25-megahertz clock for a time equal to the phase delay between the two incoming waveforms. Then it strobes the measured value into output latches once a cycle. The result is a continuously updated value expressed as a 15-bit binary number plus a sign bit.

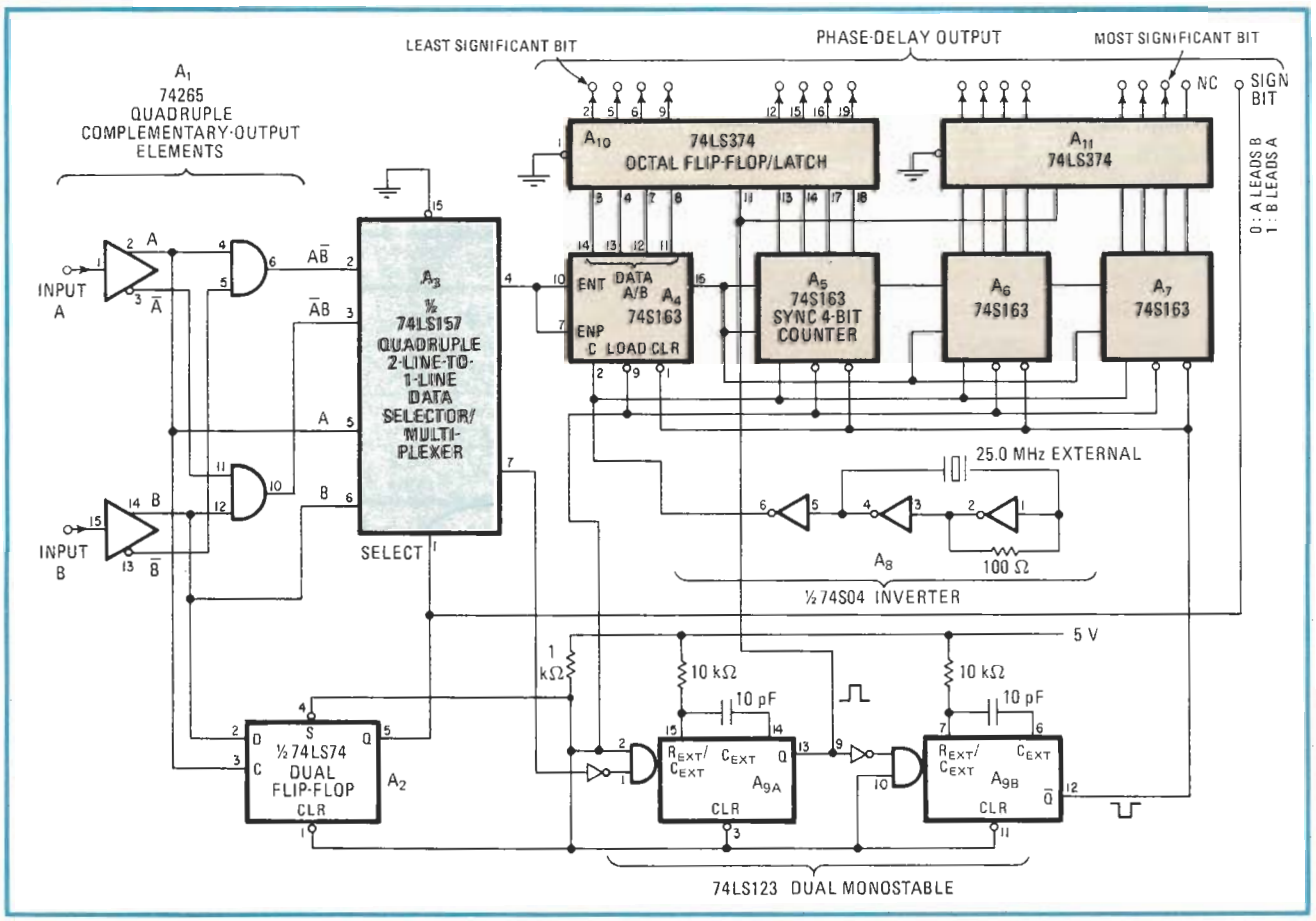
To achieve this, the cycle is viewed as one that varies from plus to minus 180°. By using only one half of the cycle for measurement, the circuit is free during the other half to store the results in the output latches and to clear the phase counters for the next measurement.

The circuit automatically determines which of the signals is to be the reference, with the phase delay measured from the rising edge of the leading signal to the rising edge of the lagging waveform. The falling edge of the reference serves as the latching signal and to set up the counters for the next cycle.

In operation, the two incoming signals, A and B, are applied to two gates of A_1. Here, the complemented signals $\overline{A}$ and $\overline{B}$ are obtained with negligible differential delay. The other two gates in the chip generate gating signals corresponding to $A\overline{B}$ and $\overline{A}B$. Flip-flop A_2 determines which input signal is the reference.

If A leads B, then the Q output of A_2 goes low and gating signal $A\overline{B}$, together with input signal A, drives the 74LS157 selector chip, A_3. Otherwise, gating signal $\overline{A}B$ together with input signal B will be selected.

The selected phase-gating signal is used to enable a chain of synchronous counters, A_4–A_7, which are driven



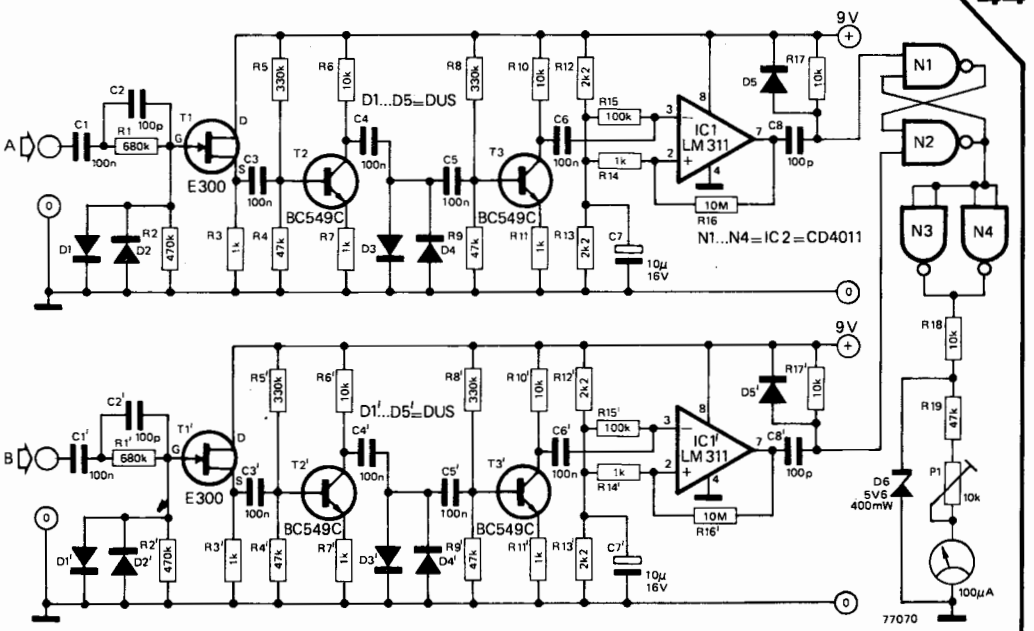
Instantaneous. Circuit continuously compares phases of two incoming square waves, providing a 15-bit and plus-sign output that has a resolution of (f_{kHz}/250)%. With a 25-MHz clock, the practical upper frequency limits that can be handled for incoming signals is 250 kHz, with lowest-frequency boundaries being about 400 Hz. Lower limits can be reduced further by decreasing the clock frequency.

from a crystal-controlled 25-MHz clock built around three inverters in A_8. When the phase-gating signal drops, A_4–A_7 stop counting, holding their final result, which indicates the phase delay, at their parallel outputs. Following this, a short pulse from one-shot A_{9A} latches the results of the count in A_{10} and A_{11}. Then the pulse-counter chain is cleared by a second pulse from A_{9B}. To ensure a proper count and store cycle, the sum of the widths of the two short pulses should be less than half the period of the highest-frequency input signal. Also, the short pulse used to clear the counters should be greater than the clock period.

The upper limit on the frequency of the input signals is set by the resolution of the phase measurement that can be tolerated. With this circuit, the resolution is given by (f/250)%, where f is the frequency in kilohertz.

The lower limit of the signal frequency is set by the overflow of the phase counters before the end of half a cycle of the input signal (that is, the maximum phase delay measured). With a 25-MHz clock and a 15-bit binary number representing the magnitude of the phase (excluding the sign bit), the minimum input frequency will be $25(10^6)/(2(2^{15}-1)) = 381$ hertz. At low input frequencies, however, a lower-frequency clock can be used while maintaining good resolution, and thus the frequency limit can be brought down even further. □

50 phasemeter



This phasemeter will measure the phase angle between two signals over the frequency range 10 Hz to 100 kHz, and is thus extremely useful for measuring the phase response of audio systems.

The principle of operation is as follows: the meter is calibrated so that when the outputs of N3 and N4 are high it reads full-scale. Flip-flop N1/N2 is set at the positive-going zero-crossing of waveform A and reset at the positive zero-crossing of waveform B. While the flip-flop is in the set condition the outputs of N3 and N4 will be high.

If the waveforms are in phase the flip-flop will be reset as soon as it is set and the outputs of N3 and N4 will remain low, so the meter will read zero. When the phase angle approaches 360° the flip-flop will remain set practically all the time and the meter will read full-scale. At a phase angle of 180° the flip-flop will be set for half the time and reset for half the time so the meter will read half-scale.

To ensure that the flip-flop is triggered at exactly the right points independent of the input waveshape or amplitude the input signals must be processed. The two input channels are identical to ensure that any phase shift introduced by the signal-processing is the same in each channel and will thus cancel. Each channel consists of a source follower FET to provide a high input impedance (approx. 1 MΩ/10 pF). R1 and diodes D1 and D2 protect the input against excessive voltages. This is followed by a x10 gain stage T2, with limiting diodes on the output, and a second x10 gain stage T3. The amplified and limited waveform is then fed to a comparator (IC1), which is connected as a Schmitt trigger. The output of this goes low on each positive transition of the input and high on each negative transition. The negative output pulses of IC1 are differentiated by C8, D5 and R17 and used to trigger the flip-flop.

The meter is best calibrated at the 180° point, since it is easy to obtain signals 180° out of phase from the two halves of a centre-tapped transformer secondary. The signals are fed into inputs A and B and P1 is adjusted until the meter reads half-scale or 180°. Alternatively the meter can be calibrated at 360° by grounding the input of N1 and adjusting P1 until the meter reads full-scale. The meter scale should, of course, be marked out linearly from 0 to 360°.

The meter will function with input voltages greater than a few millivolts RMS and is protected against input voltages in excess of 250 V, and can thus operate over an extremely wide dynamic range without adjustment.

C-MOS phasemeter can be built in lab

by M. G. Fishel
Free University of Brussels, Belgium

Since most electronic laboratories need a phasemeter only once in a while, here is a cheap alternative to buying one. All it needs is three identical C-MOS 4011 integrated circuits, some discrete components, and a good voltmeter to measure the output, and all of this should cost less than $10.

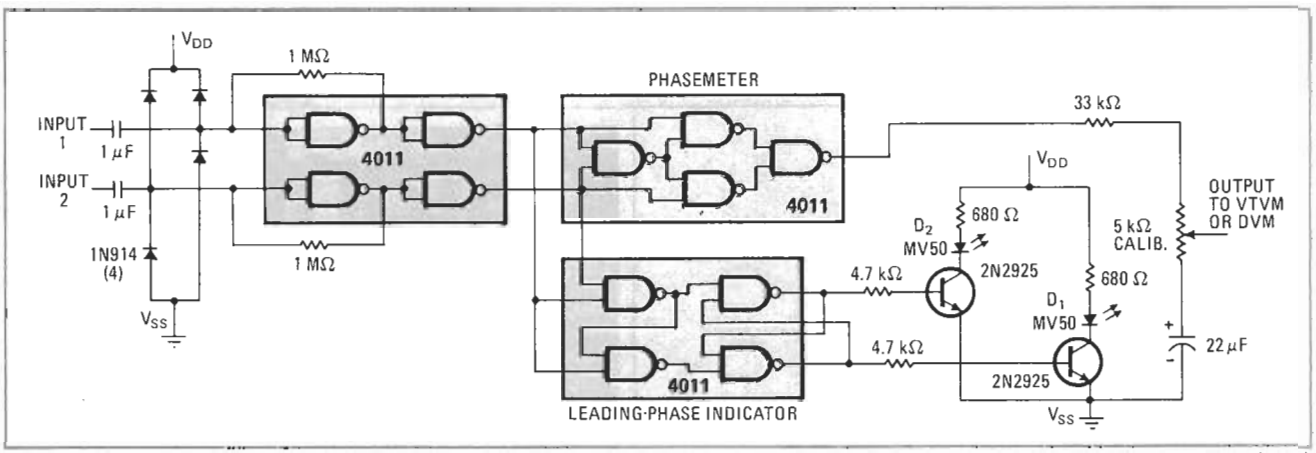
The phasemeter accepts both analog and digital signals as inputs. Its usable frequency range starts at less than 5 hertz and goes up to several megahertz, depending on power-supply voltage.

The input signals are amplified by self-biased inverting ac amplifiers and then are shaped to obtain square waves. The square waves are then fed to two separate circuits, each of which is built around a single IC.

The first of the two circuits is the actual phasemeter; it is in fact a simple EXCLUSIVE-OR gate. The phase comparator's output (at twice the input frequency) is filtered through an RC network to remove the ac ripple. The output voltage is proportional to the phase difference between the input signals. If they are in phase, the meter reading will be zero. A phase difference of 90° yields an output of $(V_{DD} - V_{SS})/2$, and the full supply voltage will appear at the output when the phase difference is 180°. The output can be adjusted to any full-scale value that is convenient by means of the calibration potentiometer.

The second circuit, which is an edge-triggered memory cell, indicates which input signal leads the other. This information is displayed by light-emitting diodes. If the phase at input 1 leads the phase at input 2, D_1 lights, and if the phase at input 2 leads, D_2 lights.

The impedance seen at the inputs is on the order of 10^6 ohms. Both inputs are protected against overvoltage by 1N914 diodes. Power-supply voltage is not critical; V_{DD} can be anywhere between 3 and 15 volts. □



Phasemeter. Incoming digital or analog signals are shaped into square waves in first IC. Then phase difference is measured and displayed as an output voltage that is directly proportional to $\Delta\phi$. Light-emitting diodes indicate which signal has leading phase. Supply voltage can be anywhere in 3-to-15-volt range. Meter can be built for less than $10 and operates at frequencies up to 5 MHz with V_{DD} of 12 volts.

Digital phase meter displays angles in degrees or radians

by Tagore J. John
Meerut, Uttar Pradesh, India

In this unit, the phase angle between two signals is measured and displayed digitally, and so the instrument is less costly than its counterparts that use precision linear circuits and expensive meter movements. The angle can be displayed in degrees, radians, or grads (400 grads = 360°). The accuracy of the instrument is ±1 least significant count, independent of signal differences in amplitude or wave shape.

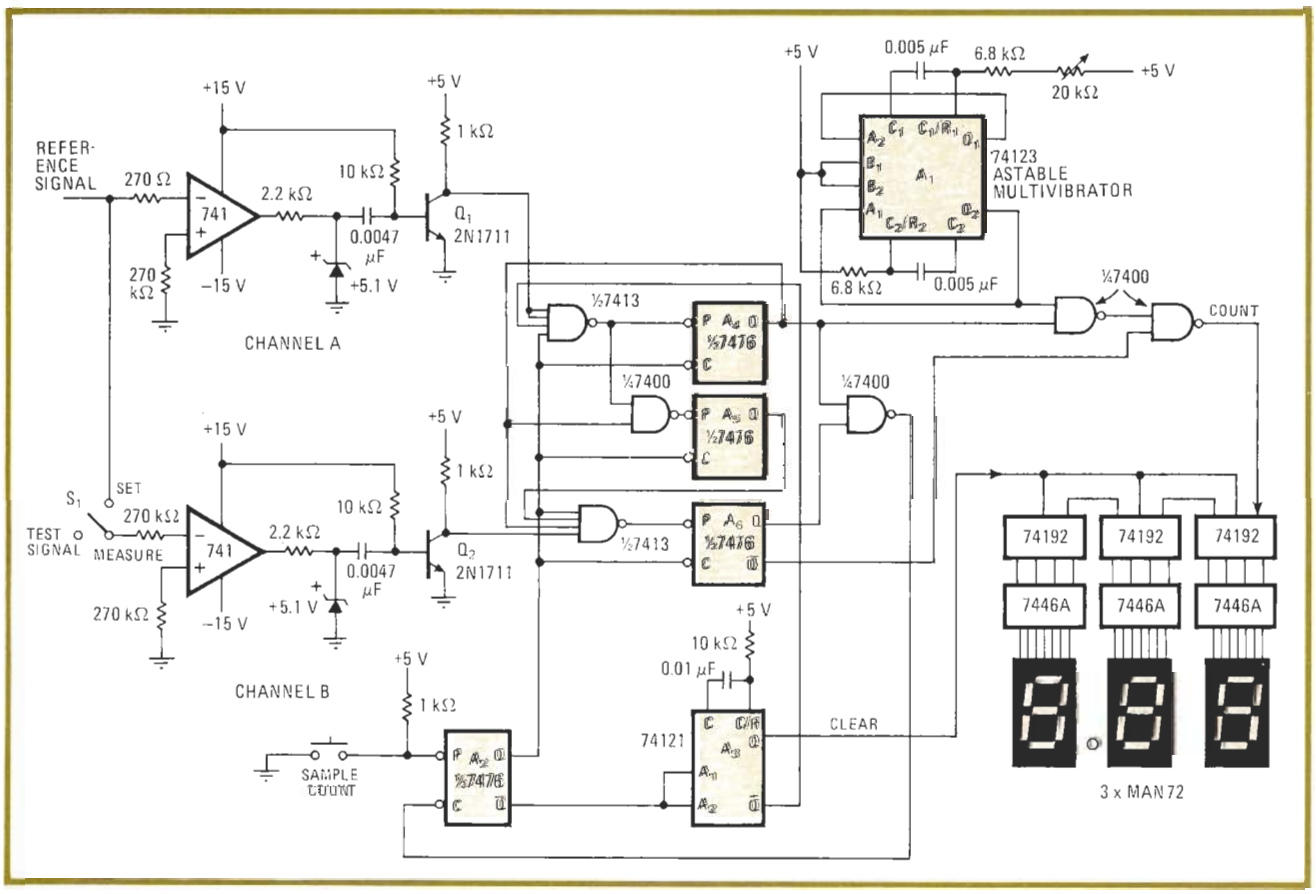
Generally, the reference and test signals are applied to channel A and channel B, respectively, as shown in the figure. Q_1 and Q_2 generate short pulses (i.e. less than 30 microseconds) to the counting logic as each signal passes upward through its zero-crossing point. To initiate the counting cycle, the logic circuit simply gates the output of an oscillator through to the 74192 counters on the first zero-crossing pulse from Q_1. The zero-crossing pulse from Q_2 terminates the count. The number displayed thus represents the phase difference expressed in the desired units, provided A_1's frequency is appropriately selected.

The instrument is calibrated by placing S_1 in the set position, introducing a reference signal, and depressing the sample-count push button as A_1 is adjusted for a display output of 360 (if output in degrees is desired), 400 (in grads), or 628 (in radians).

In normal operation, depressing the sample-count push button initiates the count cycle. Flip-flop A_2 is preset and fires one-shot A_3, whereupon the display is cleared.

Q_1's first pulse sets flip-flops A_4 and A_5 and gates A_1's output through to the 74192 counters. With a pulse from Q_2, flip-flop A_6 is set, and the output of the NAND gate driving the counters is disabled. Meanwhile, A_2 is cleared in order that the unit may then be readied for a new sample count.

The phase angles will be displayed directly. Provision should be made, however, for activating the decimal point to the right of the left-most digit when radians are displayed. □



Digital differential. Phase angle between two signals is determined to within ±1 least significant count. Using standard chips, angle is digitally measured and can be displayed in degrees, radians, or grads, provided frequency of counting oscillator, A_1, is appropriately selected.

Digital logic circuit reads phase difference

by Demetrios K. Kostopoulos
Dalmo Victor Co., Belmont, Calif.

The phase difference between two sinusoidal waves of the same frequency can be measured digitally if the phase difference is converted into a time difference and the time difference is converted into a number of pulses. A count of these pulses then serves as a numerical representation of the phase difference between the two input wave forms.

The basic outline for this simple and inexpensive digital phase meter is shown in the diagram. Signal A is the reference sinusoidal waveform, while signal B is the sinusoidal waveform whose phase (relative to signal A) is to be determined. Both signals must have the same frequency, but they may differ in amplitude. The waveforms are converted into square waves by means of the voltage comparators, and two square waves are then ANDed together.

The output of comparator $COMP_A$ is low when signal A is positive and high when signal A is negative. The opposite is true for the output of comparator $COMP_B$. This makes it possible to detect any phase difference between the two waveforms. When they do not overlap, both comparator outputs are high for a length of time that is proportional to the phase difference between signal A and signal B.

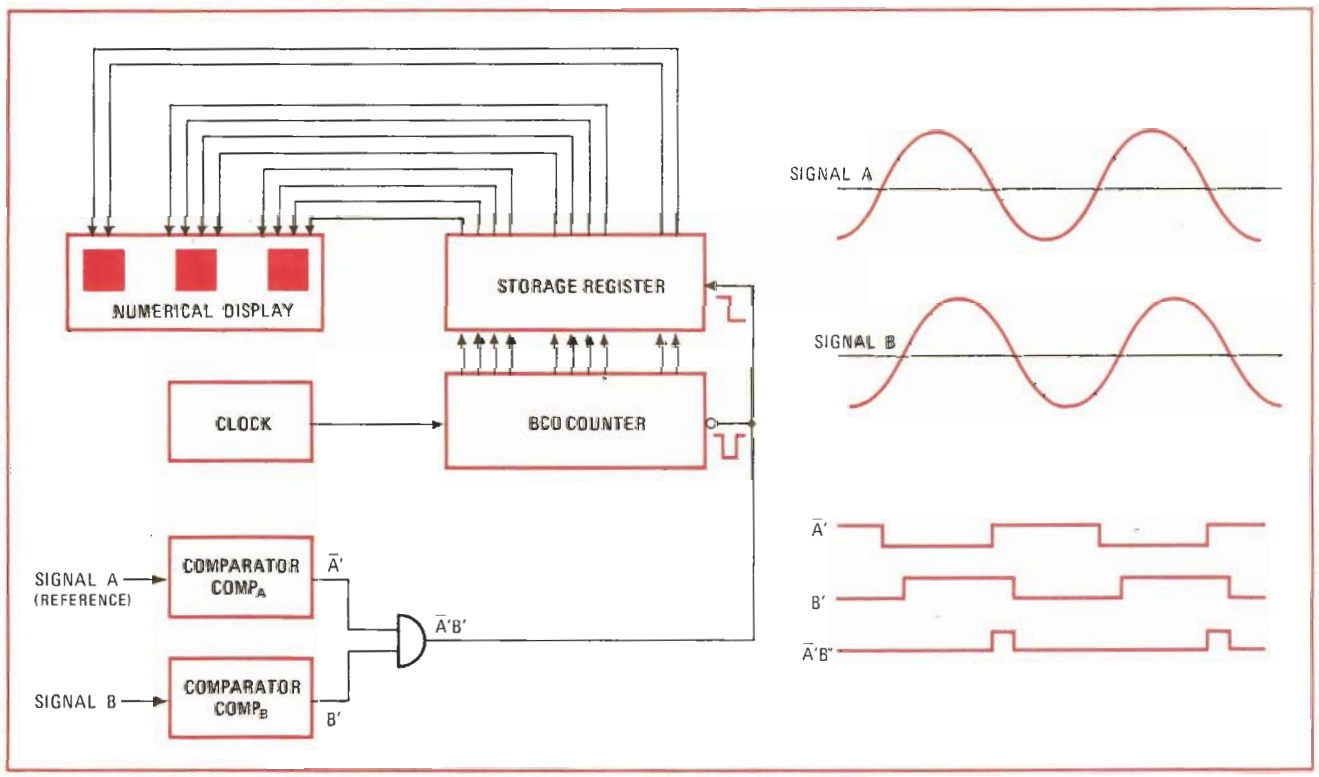
The function of the AND gate is to clear and enable the binary-coded-decimal counter. When both gate inputs are high, the gate output is also high, and the counter is enabled. The counter is cleared when the gate output goes low. The number of gate-output pulses logged by the counter is directly proportional to the time that the gate output is high. Therefore, the final number in the counter is directly proportional to the phase difference between input wave form A and input waveform B.

During the high-to-low transition of the gate output, the counter output is stored in the register. This storage register drives a set of numerical readouts that display the phase difference. The phase weight of the least-significant digit in the display is:

$$\Delta\phi = 360^\circ(f_s/f_c)$$

where f_s is the signal frequency, and f_c is the clock frequency. If $f_c = 360\ f_s$, then the units of the displayed number are whole degrees; and if $f_c = 3{,}600\ f_s$, the units become tenths of a degree. □

Determining phase digitally. Straightforward approach permits standard logic ICs to be used for measuring phase—the phase difference between sinusoidal inputs A and B is converted into a time difference. When the square-wave outputs from the comparators overlap, a phase difference exists, and the AND-gate output goes high, enabling the counter. The final count is stored in the register for display.



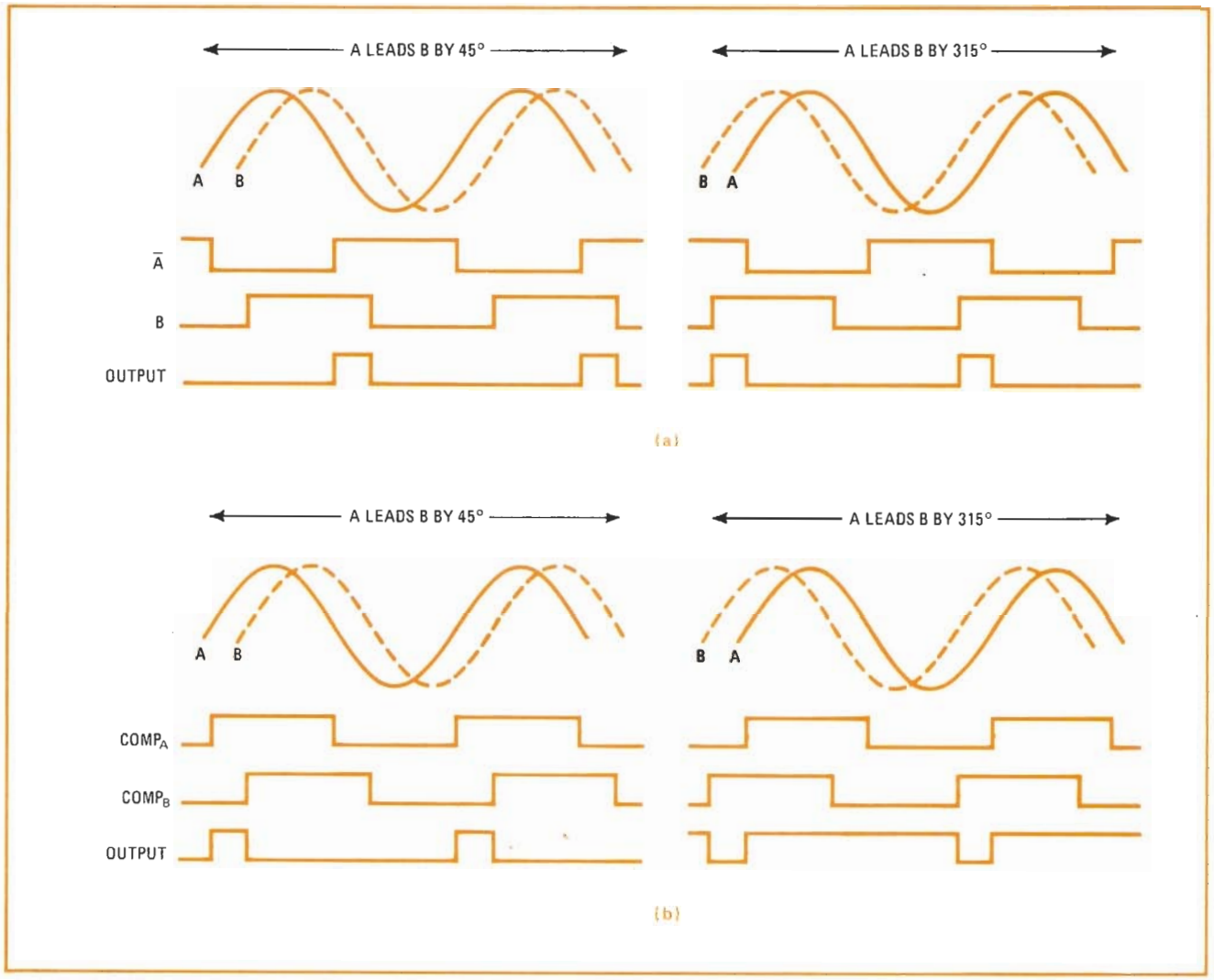
Edge-triggered flip-flops make 360° phase meter

by James C. Hager Jr.
Columbia Gas System Service Corp., Columbus, Ohio

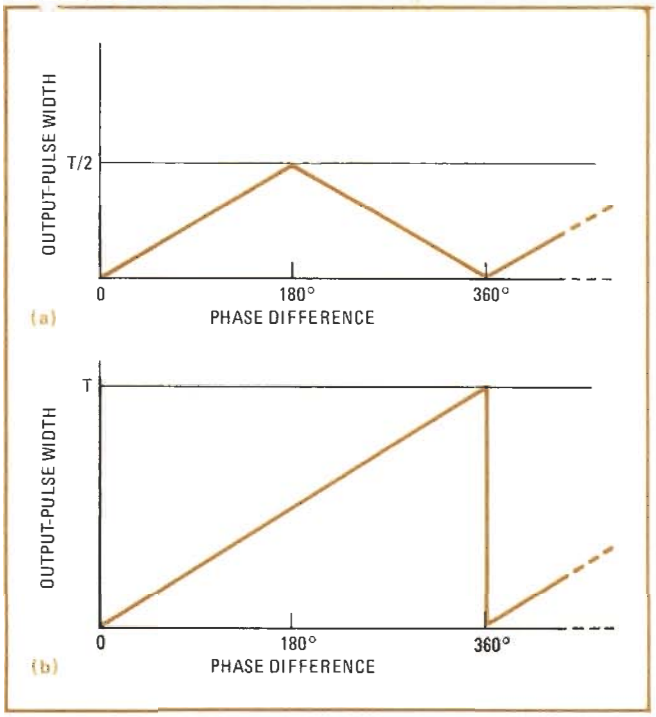
Many phase detectors measure the amount of overlap of two waves to determine the phase difference between the waves. Often designed around some form of AND gate, they can measure a maximum phase difference of 180°, because, for example, they cannot distinguish between a phase difference of 20° and a phase difference of 340°. To measure differences up to 360°, a detector must use circuit elements that respond to the sequence in which the waves arrive. A pair of edge-triggered flip-flops provides this capability.

A representative AND-type circuit by D. K. Kostopoulos appeared on page 119, in the Dec. 20, 1973, issue of *Electronics*. In this circuit, two signals are applied as inputs to comparators. The resulting square-wave outputs become the inputs to an AND gate, with one comparator output inverted with respect to the other. The AND-gate output is a pulse produced by the positive coincidence of the two signals. This pulse has a width proportional to the phase difference between the two input signals; maximum width occurs for a phase difference of 180°, as shown in Fig 2(a). The output pulse can enable a counter for a digital phase measurement, or it can be filtered with an RC network to give an analog signal proportional to the phase difference.

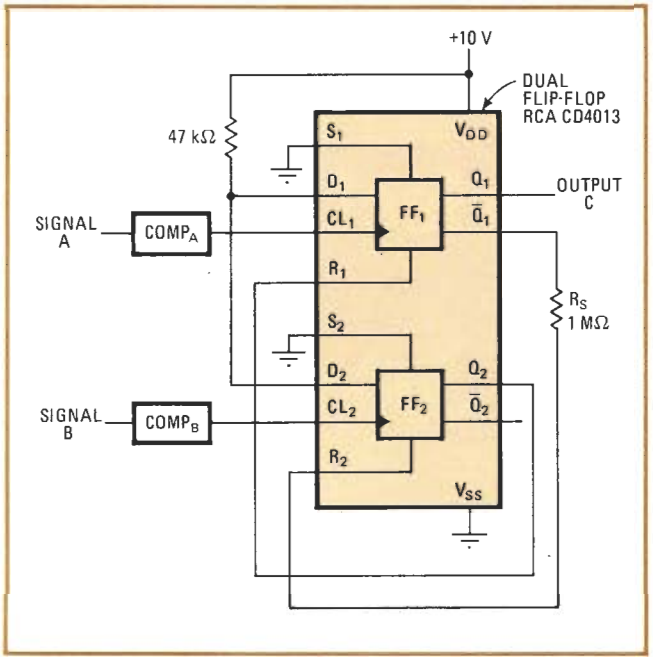
The Kostopoulos circuit can be modified to provide a



1. Two techniques. Performance of phase detector that operates on basis of overlap of two waves is shown in (a). Output is high only while both $\bar{A}$ and B are high. Performance of phase-detector circuit that operates on basis of sequence of leading edges is shown in (b). Output goes high when A goes high, and output does not go low again until B goes high.



2. Output. An AND-gate type of phase detector (a) has maximum output-pulse width at a phase difference of 180°. An edge-triggered phase detector (b) has maximum output pulse width at 360°.



3. Full circle. Use of edge-triggered flip-flops permit this phase detector to measure phase differences up to 360° between signals A and B. This C-MOS circuit can replace the AND gate used in a digital-logic circuit that reads phase difference [*Electronics*, Dec. 20, 1973, p. 119], and thus convert that circuit to full 360° capability.

full 360° phase-measurement capability. The AND gate is replaced with an inexpensive C-MOS CD4013 dual flip-flop, which eliminates the requirement to invert one signal and permits identical comparators to be used (Fig. 3). The CD4013 is configured for 360° phase detection by connecting $\bar{Q}_1$ output of FF_1 to the reset (R_2) input of FF_2 and connecting the Q_2 output of FF_2 to the reset (R_1) input of FF_1. The set inputs (S_1, S_2) of both flip-flops are effectively removed by returning them to ground. The "D" inputs (D_1, D_2), are hard-wired high via a pull-up resistor to +V. The clock inputs (CL_1, CL_2) serve as the inputs to the edge-triggered phase detector, and the output is present at Q_1.

The positive transition of the $COMP_A$ output signal transfers D_1's hard-wired 1 to the output, which causes Q_1 to go high and $\bar{Q}_1$ to go low. With $\bar{Q}_1$ low, the reset level is removed from R_2. Q_1 remains high until, as in FF_1, the positive transition of the $COMP_B$ output causes Q_2 to go high, which resets FF_1 and forces Q_1 low.

The positive transition of the $COMP_A$ output is the leading edge of the output pulse at Q_1, while the positive transition of the $COMP_B$ output becomes the trailing edge. This output pulse has a width directly proportional to the phase difference between the input signals to the two comparators; maximum pulse width occurs for a phase difference of 360°, as shown in Fig. 2(b). Both signals must be of the same frequency, and signal B is assumed to lag behind reference signal A.

The maximum reset-pulse width required for the CD4013 is less than 0.5 microsecond. Assuming at least 2 picofarads input capacitance at the reset terminal (R_2), a value of 1 megohm for R_s ensures that the minimum pulse-width requirements are met. □

Versatile phase detector produces unambiguous output

by L. E. S. Amon and B. Lohrey
University of Otago, Department of Physics, Dunedin, New Zealand

A dual monostable multivibrator and integrator network forms a detector that not only measures phase difference between two signals throughout the entire 360° range, but also produces an unambiguous output signal for various phase-advance and -retard conditions by generating a voltage and slope output combination that is unique for every angle.

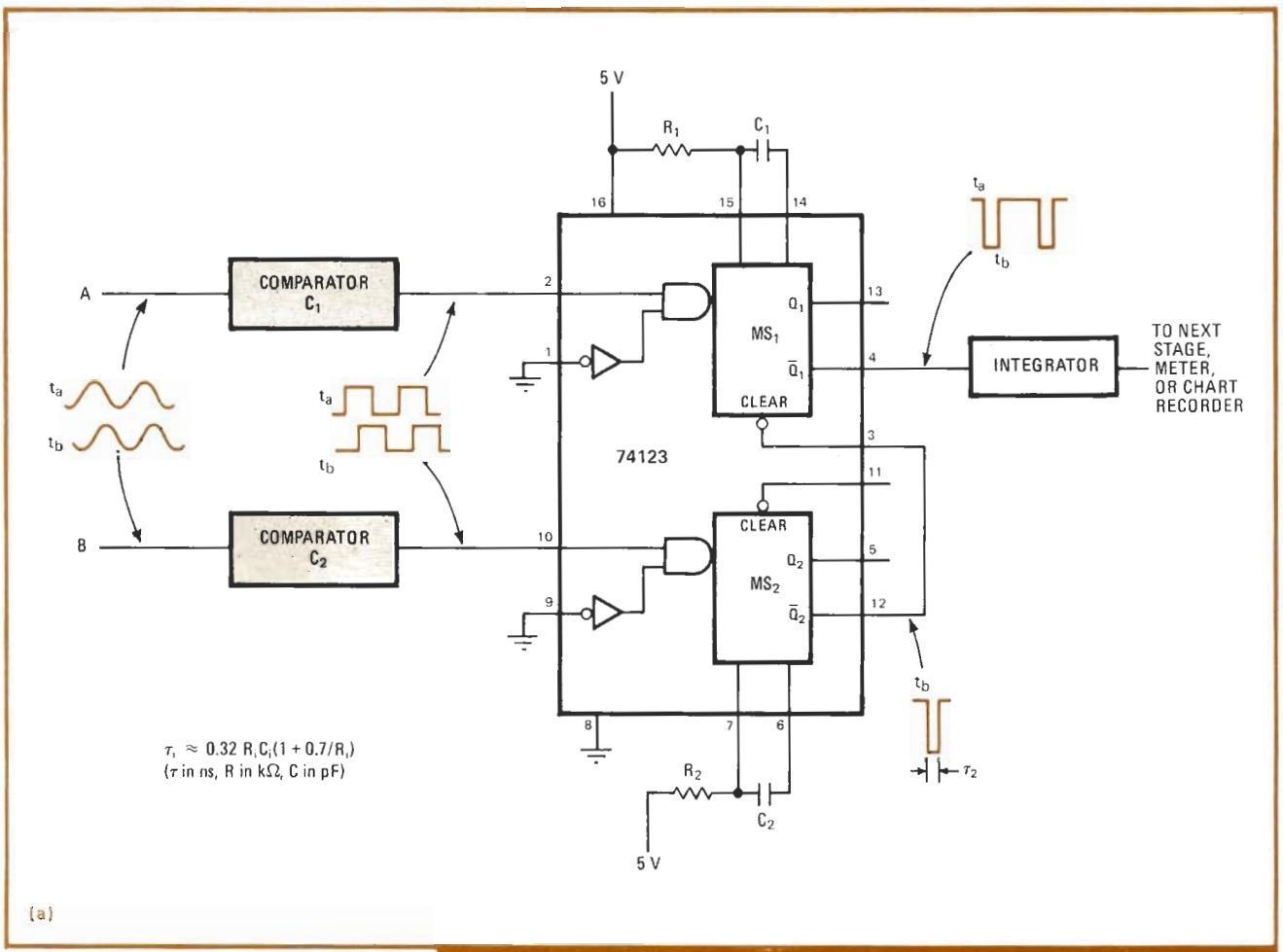
As shown in (a) of the figure, a positive zero crossing of reference signal A triggers the comparator C_1 and one-shot MS_1 at time t_a, where MS_1 is one half of the 74123 device. This one-shot, in the retriggerable mode and set so that its pulse width τ_1 is greater than T_a, the period of the reference signal, stays on until comparator C_2 and one-shot MS_2 are fired by signal B at time t_b. The narrow pulse produced by MS_2 resets MS_1.

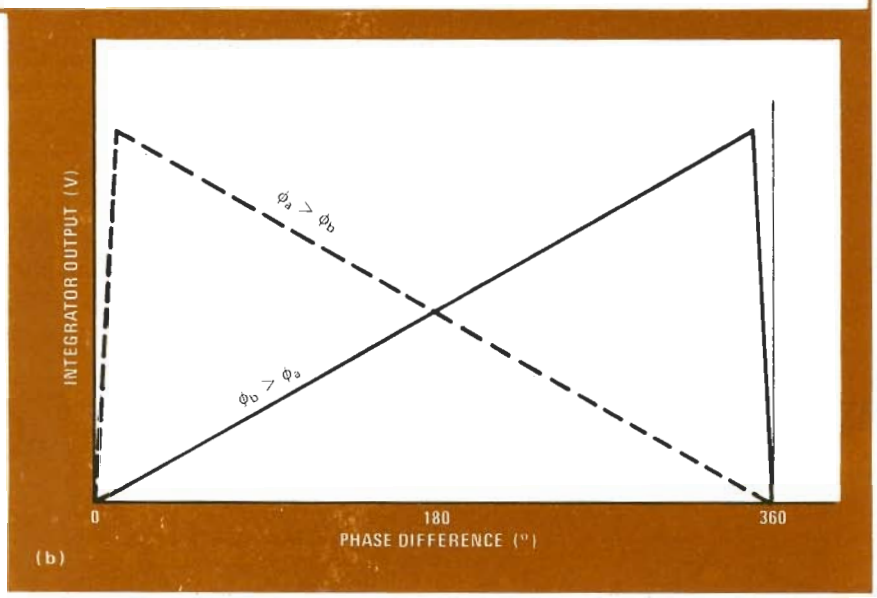
The phase of B with respect to A may be related to the duty cycle of the output signal from MS_1. The duty cycle may be expressed by:

$$W = \frac{t_b - t_a}{T_a}$$

The output signal may be converted to a dc voltage by the integrator network connected to the output of MS_1. Alternatively, the phase may be measured digitally [see *Electronics*, Dec. 20, 1973, p. 119].

As shown in (b), an increase in the dc output of the integrator occurs when the phase angle of B increases





360° phase detector. Dual one-shot and integrator yield unambiguous voltage and slope output combination for changing phase-lead or phase-leg angles (a). Output from integrator is maximum at 360° when A leads B, minimum when B leads A (b).

with respect to A. The output decreases when the phase angle of B decreases with respect to A. Thus the frequency relation of B to A may be determined from the slope of the integrator's output if the two signals are of similar but not identical frequency.

When the two signals are not harmonically related, their phase relationship will change with time. The circuit is therefore useful as a phase-modulation detector for applications in communications receivers.

Further versatility can be achieved by placing frequency dividers at the input ports of the phase detector to achieve a full-scale output at N × 360°. The sensitivity can be increased, on the other hand, if both of the input frequencies are multiplied by N. This reduces the range of phases that yield an identical output voltage to 360°/N. □

Digital phase meter is accurate to ±1°

by Naveen J. Tangri
Indian Institute of Technology, Powai, Bombay, India

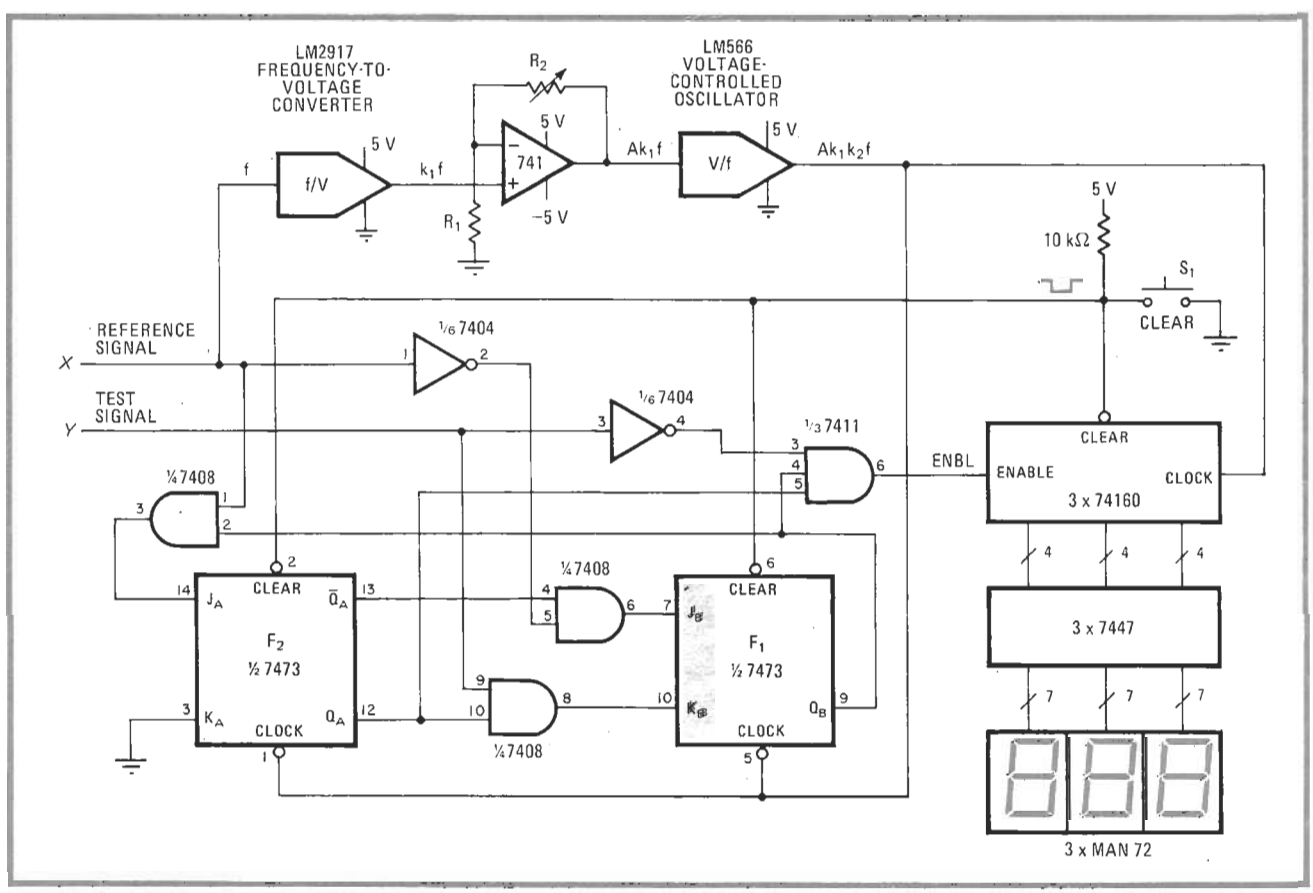
Performing measurements digitally, this meter determines the phase angle between two signals that can be separated by as much as 180°. The resolution of the measurement is ±1°, independent of the shape or the amplitude of the waveforms under observation.

In this circuit, the leading edges of the reference (x) and test (y) signals are used to enable or disable, respectively, the counting of three cascaded 74160 binary-coded decimal counters. These counters are clocked at a much higher frequency than is present at the x or y inputs, and at a rate proportional to the reference frequency. Thus the number of clocked pulses that occur during the enabling time represents the phase delay of the test signal with respect to the reference.

As shown, the LM2917 frequency-to-voltage converter, the 741 op amp, and the LM566 voltage-controlled oscillator convert reference signal x to a frequency equal to Ak_1k_2f, where k_1 and k_2 are the conversion constants of the 2917 and 566, A is the gain of the op-amp stage, and f is the incoming frequency. This signal serves to clock the 74160 counters.

When enabled, the counters advance once each $T_c = 1/Ak_1k_2f$ seconds. Thus the count reached after time Δt is $n = \Delta t/T_c = (\theta/\omega)(Ak_1k_2f)$, where θ is the phase difference between x and y, and ω is the radian frequency (note $\theta = \omega t$). Thus $n = k_3\theta$, where $k_3 = Ak_1k_2/2\pi$. But k_3 can be selected easily (by varying the gain of the op amp) to equal $180/\pi = 1$, so that $n = \theta$ in degrees.

The 7423 flip-flops and their associated logic generate the enable signal, which has a width equal to the phase difference between the x and y pulse trains. The rising edge of the enable pulse ENBL is generated at the first high-going transition of the x signal following a system clear, and the pulse falls on the arrival of the y signal. If the clear command occurs during the time the x signal is low, the J input of flip-flop F_1 is immediately brought high and F_1 is set upon the arrival of a clock pulse. When x goes high, F_2 is set, and the output of the 7411 NAND gate is brought to logic 1.



Count on delay. Phase meter finds angle between two signals to ±1°. Number of pulses counted during enable time, which is determined by the interval between the rising edge of x and test signal y, represents the phase delay, in degrees.

When the y input moves high, pin 3 of the 7411 is brought low and F_1 is reset, also bringing ENBL low and deactivating the circuit until a system clear is again initiated. Meanwhile, the counters advance and their final value is presented to the 7447 drivers and displayed by the MAN 72 seven-segment displays.

If a system clear occurs while x is high, the process is similar. The fact that x may be high at this time has no effect on setting flip-flop F_2 because the Q output of F_1 is low. But F_1 will be set when x moves low, and the rising edge of x's next pulse enables the setting of F_2 and the generation of the ENBL pulse as before. □