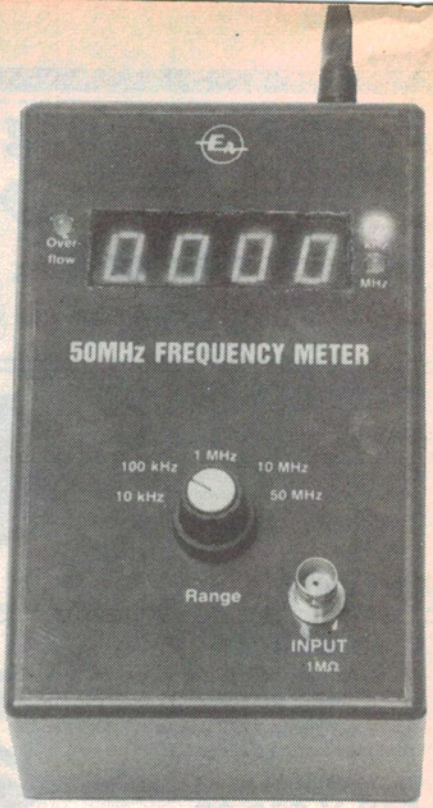
Build this low cost

50MHz Digital Frequency Meter

Here's the latest in our line of inexpensive, easy-to-build test gear: a 4 digit frequency counter. Offering high sensitivity and input impedance, it measures to well over 50MHz. All parts mount on a single PC board.



by MARK CHEESEMAN

Of the frequency counter designs we've published in the last few years, almost all have aimed to provide as high a frequency capability and resolution as possible. Our 500MHz design published in December 1981 and February 1982 has proven to be a popular kit for this reason.

However, in common with other high-performance designs published of late, it uses several rather expensive integrated circuits. While these devices make the design and construction of a frequency counter much simpler than would otherwise be possible, the asking price of $75 to $80 for the display driver chip alone has made it hard for many people to justify the cost of such a kit. In contrast, the total cost of the parts in the design presented here amounts to little more than the price of this IC alone!

Our new design differs from the 500MHz design in two main respects. Firstly, its nominal maximum frequency is 50MHz instead of 500. This saves on the cost of an expensive ECL prescaler. Unless you are a VHF/UHF radio buff (or have extremely good hearing!), this is unlikely to be a major handicap. The vast majority of signals most experimenters are likely to want to measure are well below 50MHz.

Actually, the prototype counts accurately to well over 70MHz, although the actual figure which is ultimately obtained will depend on the performance of the first prescaler stage.

The second main difference is that the number of digits in the display has been reduced from seven to four. This allows the use of a much cheaper counter and display chip. Four digits still gives more resolution than most digital multimeters, and it is possible to deliberately overrange the instrument by two or three ranges (depending on the frequency actually being measured) to see the less significant digits. This still effectively gives a six or seven digit display, even if it isn't quite as convenient. But, considering the money which you have saved, it is not really much of a problem.

The word *counter* in the name of the instrument is derived from the way in which it measures frequency. A digital counter simply counts the number of cycles which occur in a given time period. If this time period is one second, then the count accumulated in the counter is equal to the frequency of the measured signal in Hertz.

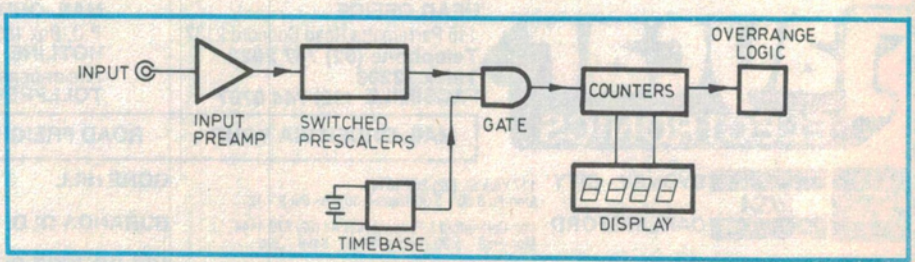
However, a gating time of one second is not the only one which can be used. A tenth of a second makes for an even faster updating speed on the display. The trade-off here is that the maximum resolution now becomes 10Hz. Since the four digit display limits us to this figure on all but the bottom range anyway, we might as well use a tenth of a second gating time on these ranges. Also, as will be shown later, it is possible to obtain a six digit resolution on the three higher ranges, and five digits on the 100kHz range, by simply rotating the range switch back a notch or two.

Circuit details

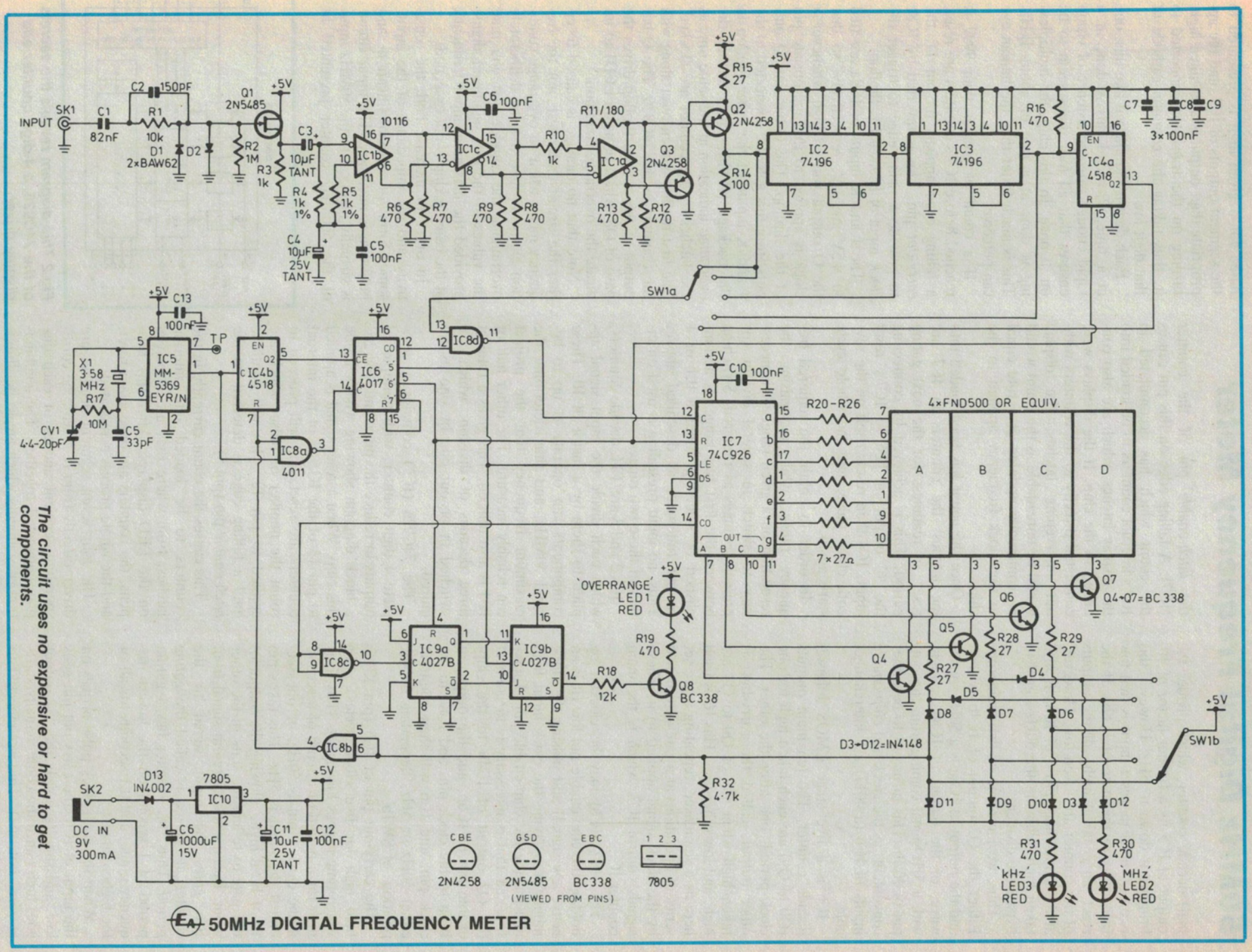
Although the circuit may seem complicated, it is easy to understand how it works if you break it down into sections, and analyse them separately. Fig.1 shows the basic block diagram of the counter.

The main timebase is derived from a 3.579545 "NTSC TV colour-burst" crystal. These are quite cheap, due to mass production for US and Japanese television receivers. IC5, an MM5369 EYR/N, contains an inbuilt crystal oscillator, requiring only an external crystal and a couple of capacitors to complete the circuit. It also contains a factory-programmed 17 stage divider, to divide the crystal frequency down to 50Hz.

IC4b is a BCD (binary-coded deci-



The basic functional blocks of a frequency counter.



50MHz DIGITAL FREQUENCY METER

The circuit uses no expensive or hard to get components.

mal) decade counter, which divides the output of IC5 by a further factor of 10, bringing it down to 5Hz. However this is only true if its *reset* input is tied low (according to the state of IC8b). If the reset pin is taken high, all the outputs of the counter are taken low. However, at the same time, pin 2 of IC8a is also taken high, allowing the 50Hz signal to bypass the divider.

Thus, we have one of two situations. Either the Q2 output of IC4b is low, and the output of IC8a is a 50Hz square wave, or the output of IC8a is high, with a 5Hz signal coming from the output of IC4b. This turns out to be rather convenient, as the *clock* and *chip enable* inputs of IC6 (a 4017) are interchangeable.

IC6 is a five stage CMOS Johnson decade counter. The ten main outputs (Q0 to Q9) are each taken high for one clock period, one after the other. The other output, called the carry-out, is taken high when any of Q0 to Q4 are high, and low otherwise. This IC is used here as a sequencer, repeating a pre-set series of operations at a rate determined by the clock signal applied to it. These signals control IC7, which is the main counter IC.

The 4017 (IC6) may be clocked by holding the chip-enable pin low (it is an active-low signal) and pulsing the clock input, or by tying the clock input high and pulsing the chip-enable pin. Therefore, all that is necessary is to connect the Q2 output of IC4b to the chip-enable pin of IC6b, and the output of IC8a to the clock pin, and IC8a to the clock pin, and IC6 will then count at either 50Hz or 5Hz, depending on the position of SW1b.

The carry-out pin of IC6 (pin 12) is held high for five clock cycles, after which time it goes low again. Thus, it is high for a period of a tenth of a second if the clock input is 50Hz, or one second if the input is 5Hz. This takes pin 12 of IC8d high, allowing the output of this gate to reflect the state of the other input. Because the carry-out signal from IC6 *gates* the input signal to the counter, its period is called the *gating period*. Thus, the counter has a gating period of 1 second on the lowest frequency range, and 0.1 seconds for all of the higher ranges.

When the sixth clock pulse arrives on the input of IC6, the carry-out pin goes low, and simultaneously the "5" output goes high (since the count actually starts at zero, not one). This is connected to the *latch-enable* pin of the counter (IC7). A falling edge on this pin causes the count which has accumulated in IC7's internal counters to be loaded into the display latches, which are also contained in the chip. If the displays were connected directly to the counters without intervening latches, the display would be unreadable as the count would be continually updated at a rate equal to the clock frequency applied to the chip.

Once the count has been loaded into the latches, the counters in IC7 are reset, in readiness for the next gating period. This is achieved by connecting the '6' output of IC6 to IC7's *reset* input. IC4 then resets itself on the seventh clock pulse, and the whole cycle starts again.

In order to obtain the required frequency range, while maximising the resolution on a given range, it is necessary to switch in several divider (or prescaler) stages as required. Switching between the first two ranges is accomplished by selecting either a 0.1 or 1 second timebase, as described above. Thus, no input prescaling is used on either of these two ranges.

ICs 2 and 3 are TTL decade counters, which each divide the input signal applied to them by a factor of 10. These components can operate at up to beyond 50MHz, and thus determine the maximum frequency that the project can reliably measure. The other half of IC4 is also utilised. This gives a total of three decades of division, which are switched in or out one by one as required.

The 74C926 (IC7) contains a complete 4 digit counter, with multiplexed outputs to reduce the pin count. Fig.2 is a block diagram showing what's inside this chip. When a reset signal is applied to pin 13 of the IC, all of the internal counters are reset, and will proceed to count the number of pulses which are applied to pin 12. This will continue until a falling edge is detected on the *latch-enable* pin (pin 5).

This causes the count currently in the counters to be loaded into internal latches, from where they are displayed on the LED displays. After this happens, the counters are once again reset, and the whole process is repeated.

The four seven segment displays are driven directly from IC7, with the corresponding segment anodes of each display connected together. The combination of segments which are to be illuminated for a given digit is presented to the segment outputs of IC7, and the appropriate digit output is also taken high, turning on the transistor connected to it, thus taking the common cathode of that digit low.

Each digit is illuminated like this, one at a time. Provided this is done at a rapid enough rate, persistence of vision ensures that all four digits seem to be on at once. In this chip, the multiplexing is done at a rate of about 1kHz. This is much faster than the human eye can perceive.

If a count of greater than 9999 is reached before IC7's counters are reset, a falling edge appears on pin 14, the *carry-out* pin. This is inverted by IC8c to provide a rising edge to trigger the *clock* input of IC9a, a J-K flipflop.

The J and K inputs of IC9a are tied to +5V and 0V, respectively, so that the Q output will go high whenever a clock is applied to the appropriate pin of the flipflop. The Q-bar and Q outputs from this gate are connected to the J and K inputs of the other flipflop in the package (IC9b), which latches the *overrange* indication at the same time as the latches in the counter are clocked. The first flipflop is then reset along with the counters in the 74C926. The Q-bar output of this second flipflop drives the base of Q8, which turns on LED1 to indicate the overrange condition.

Note that no damage is caused to either the circuit under test, nor the frequency meter when an overrange condition exists. In fact, it is by deliberately overranging the counter that you read the values of the less significant digits, provided the maximum input frequency of the counter chip is not exceeded.

In order to increase both the sensitivity and the impedance of the input, some form of pre-amplification and buffering is necessary. The input circuit is virtually identical to the 50MHz input of the 500MHz counter presented in

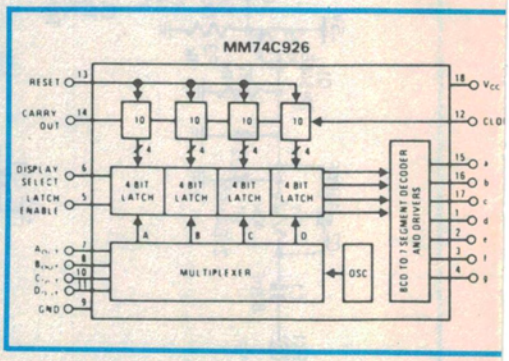
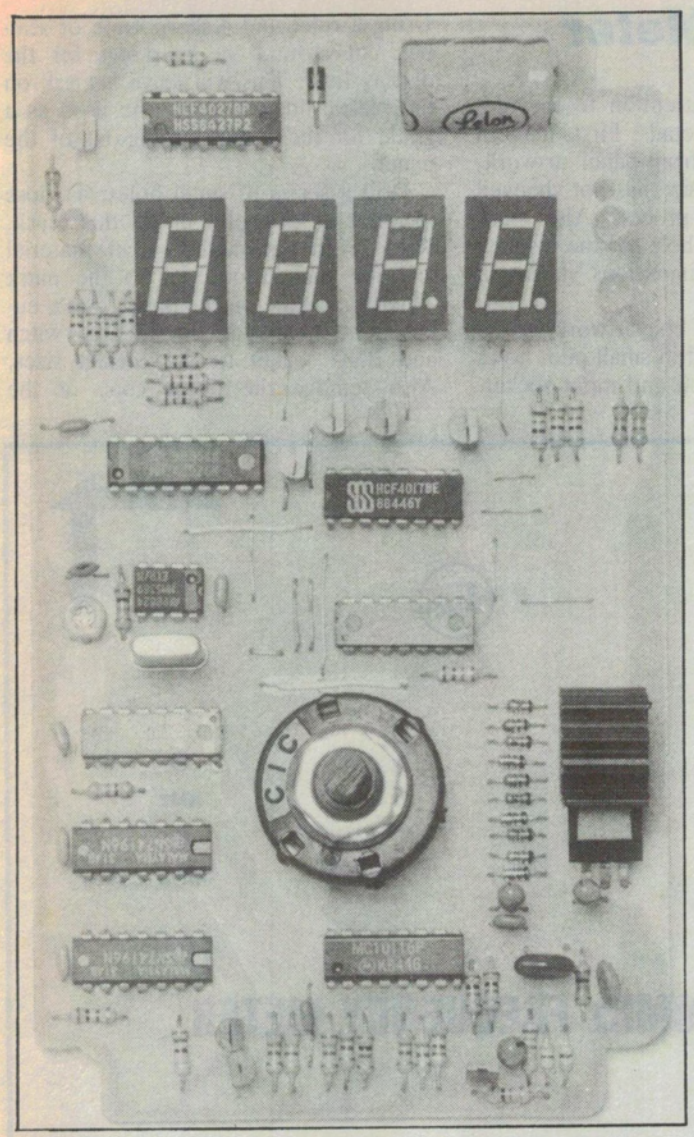
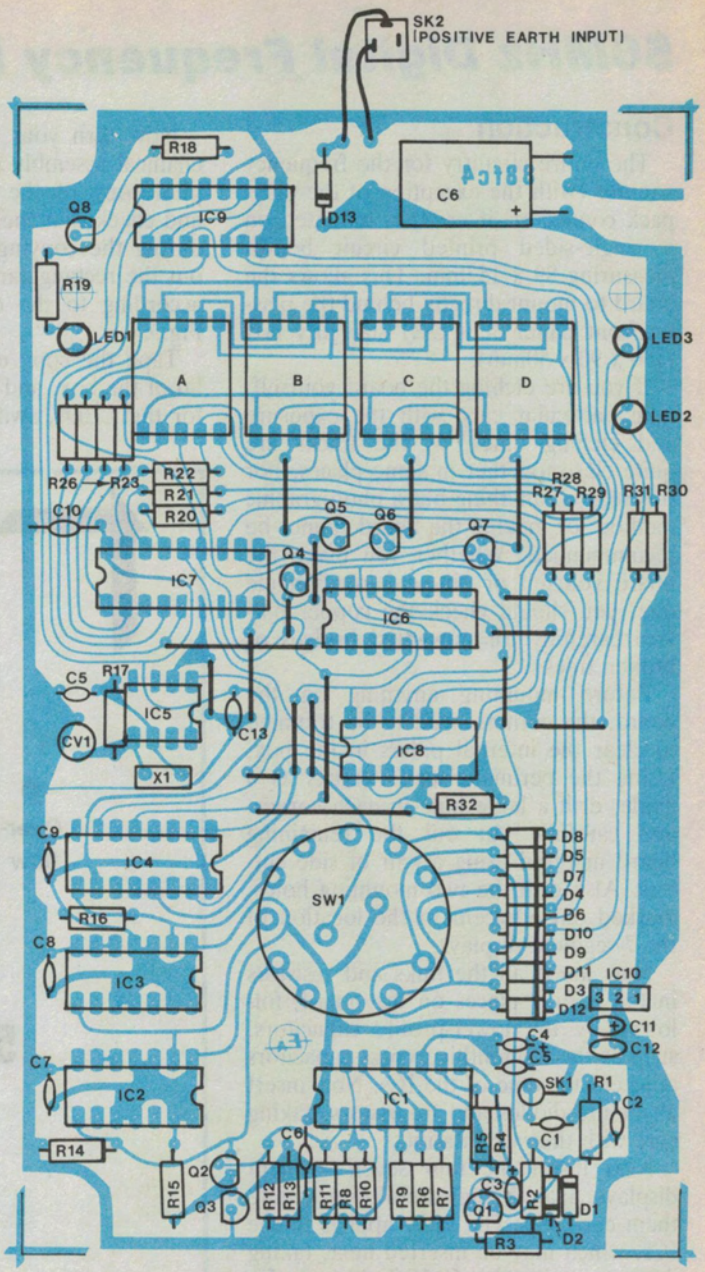


Fig.2 This diagram reveals the secrets of the 74C926, a 4-digit counter and display driver.





The finished product, before mounting it in the box. The 3-terminal regulator may need a larger heatsink than the one pictured here if the plug-pack voltage is a little on the high side.

December 1981. We tried many different types of input stage, but were hard pushed to better the performance and simplicity of the earlier design.

The input is first clamped by the two diodes, D1 and D2, to ensure that large input signals do not destroy the FET which follows it. The FET (Q1) is configured as a source-follower, and serves to provide the counter with a high input impedance. This impedance is determined by the gate-bias resistor, which is 1MΩ.

The FET is capacitively coupled to IC1, a 10116 ECL (emitter-coupled logic) line receiver. This contains three identical stages, the first two of which are used to amplify the signal from the FET input buffer. The third stage is configured as a Schmitt trigger, because of the positive feedback provided by R11. This helps to minimise false triggering due to noise pickup, by introducing some hysteresis.

The differential pair formed by transistors Q2 and Q3 converts the small voltage swings appearing on the output of the ECL chip to the correct levels, for either the TTL divider which follows it (IC2) or the NAND gate (IC8d), depending on the position of SW1a.

Power for the counter is provided from a 9V DC plug pack. This ensures a degree of safety, as all 240V wiring is contained within the plug pack, not within the box of the counter. The DC input first passes through a series diode to protect the devices in the counter from reverse polarity on the supply. There seems to be no standardisation as to whether a plug pack connector should have the positive or negative terminal as the sleeve of the plug: hence the diode. This means that if the plug pack is of the wrong polarity, the counter will simply not work, with no damage to either the counter or the supply.

A 1000uF capacitor (C6) ensures that the incoming DC is relatively free from ripple. IC10, a 7805 three-terminal regulator drops the supply voltage down to the 5 volts required by the counter circuitry. This is then bypassed by C11 and C12, to ensure a low impedance supply at the frequencies which may appear in the circuit. Several other bypass capacitors have been placed close to ICs which may be particularly noisy or sensitive to supply noise, so that internally generated signals (such as the multiplexing oscillator in IC7) do not, say, appear on the input.

50MHz Digital Frequency Meter

Construction

The entire circuitry for the frequency counter (with the exception of the plug-pack connector, if used) is mounted on a single-sided printed circuit board, measuring 89 x 153mm. This allows the board to mount directly behind the plastic front panel of a UB1 size jiffy box (150 x 90 x 50mm).

If you are etching the board yourself, take particular care with the exposure and etching times, as the tracks are quite close together in some places. For this reason, anything but a photographic method for making the board cannot be recommended. Whether you make the board yourself or obtain a ready-made one, you should check the copper pattern carefully for unwanted bridges or broken tracks.

Before mounting anything on the board, the corners need to be trimmed to clear the internal pillars in the box. Using the perimeter earth tracks as a guide, drill a large hole in each corner, and carefully cut out the remaining board material using a pair of side cutters. Also drill the two mounting holes, marked out adjacent to the location of the 7-segment displays.

Now insert all the links and resistors in the correct places on the board, followed by the lower-profile capacitors, such as the monolithic bypass capacitors adjacent to some of the ICs. Now insert all of the diodes and transistors, taking care with their orientation.

Next insert the four seven segment displays, again being careful to orientate them correctly. The same applies to the ICs, which may be inserted next, taking due care with the CMOS devices. Finally, solder the rotary switch to the board, making sure that it sits down as close to the board as possible. Do not apply too much heat to the switch pins, as you may melt the plastic body.

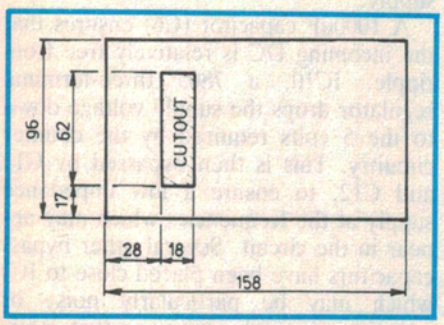
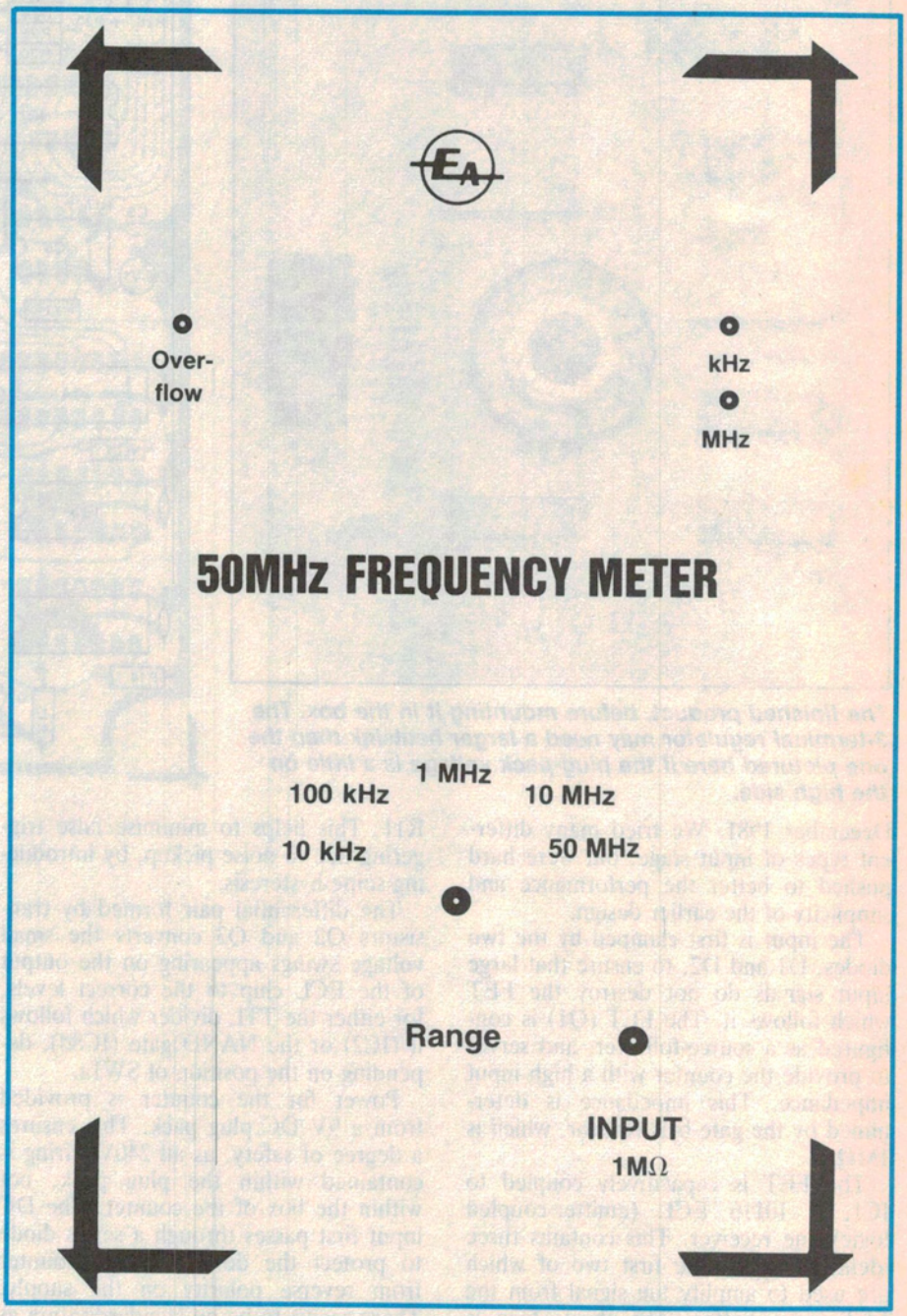


Fig.1 The location and size of the front panel cut-out for the display.

Now turn your attention to the mechanical assembly details. First, make a photocopy of the front-panel artwork, and check that the size has not changed during the copying process. Also mark out the rectangular hole for the display, according to the dimensions shown in Fig.3.

Tape the copy of the artwork to the lid of the box, and drill small pilot holes for the LEDs, switch and input socket. Using a ruler and a sharp knife or scalpel, cut around the markings for the display hole. This will leave a mark on the plastic lid, which can be used as a guide for the actual cutting-out of the panel.

Drill a series of small holes, as close together as possible, inside this mark. Remove the unwanted panel material and file the cut-out out to the mark which was made on the panel. Also, enlarge the holes for the LEDs, switch and BNC socket to the correct sizes. Also remove the paper copy of the



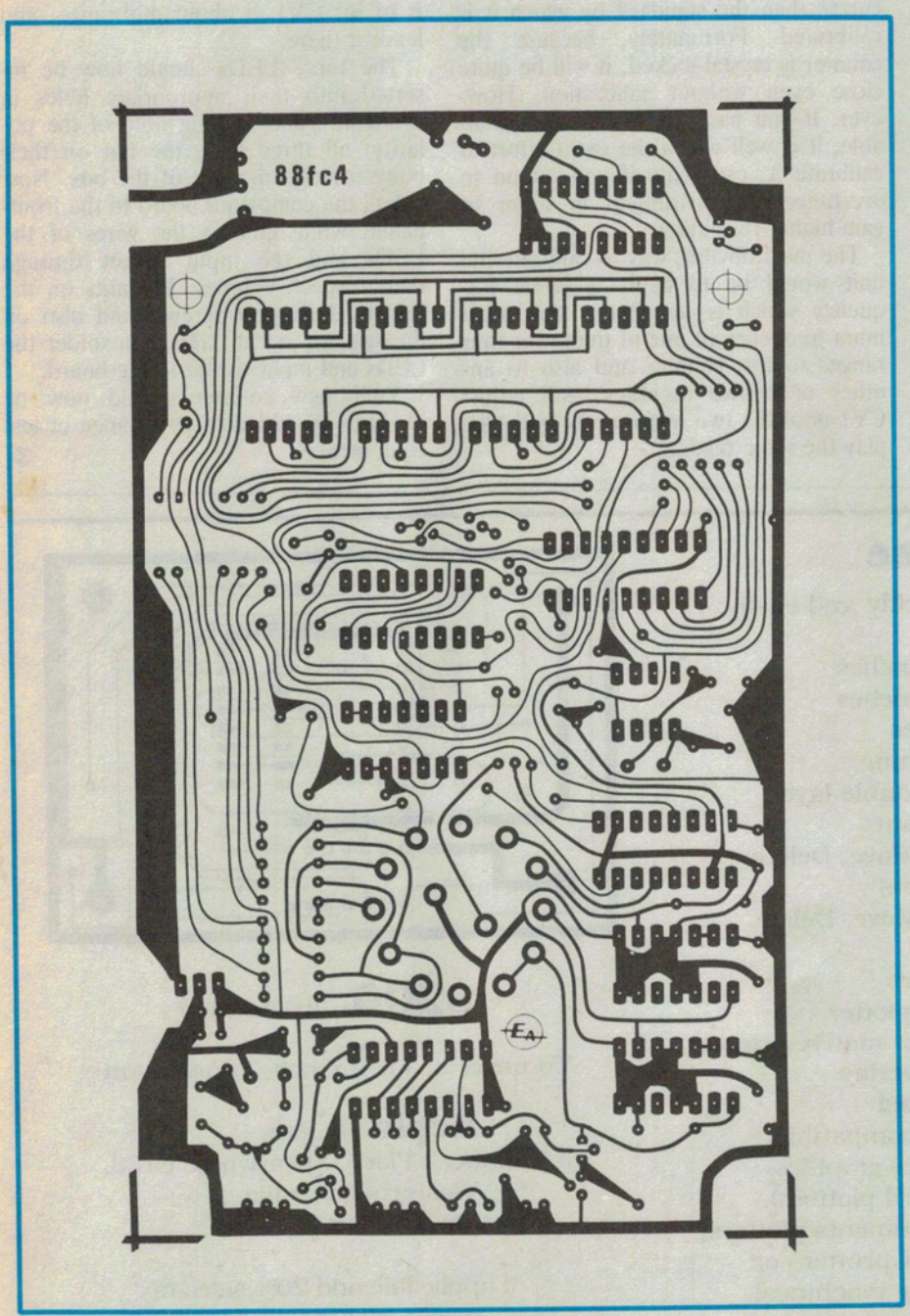
The front-panel artwork, for those who like to 'roll their own'.

front-panel at this point.

Place the assembled PCB in position behind the lid of the box, and align the two so that the display sits properly centered in the appropriate cut-out, and mark out the locations of the mounting holes on the lid using the board as a guide. Carefully countersink the holes, using a large drill bit rotated by hand, so that the mounting screws will lie flush with the surface of the lid and not cause the dress front panel to appear 'lumpy' when it is applied.

Insert a couple of 20mm long 6BA counter sunk screws in these holes, and secure them in place with a nut each. Tighten these nuts well, as the screw heads will be inaccessible when the front panel is fixed in place. Now, carefully attach the dress panel to the lid of the box, making sure to get it right the first time, as the panel cannot be removed without damage once the adhesive has taken hold.

Now, with a sharp implement such as a scalpel, make the holes in the front panel to line up with those drilled in the lid. Insert the BNC socket in the appropriate hole, and tighten the nut on the back. A star-washer between the socket and the panel will ensure good electrical contact between the two, and also help to prevent loosening of the socket. Also, solder a couple of short, stiff



A full sized reproduction of the printed circuit artwork.

Parts List

1 PCB measuring 88 x 152mm coded 88fc4
1 UB1 plastic jiffy box, 150 x 90 x 50mm
1 2 pole, 5 position PCB mount switch
1 knob to suit switch
1 panel mount BNC socket
1 3.579545MHz crystal
1 2.5mm plug-pack socket

Resistors (all 1/5w, 5% unless noted)

11 x 27Ω, 1 x 100Ω, 1 x 180Ω, 10 x 470Ω, 2 x 1k, 1 x 4.7k, 1 x 10k 1 x 10k, 1 x 12k, 1 x 1M, 1 x 10M, 2 x 1k 1%.

Capacitors

1 82nF metallised polyester
1 150pF ceramic
3 10uF 25V tantalum
8 100nF monolithic ceramic ('blue chips')
1 1000uF 25V electrolytic (axial or radial)
1 33pF ceramic
1 4.4-20pF trimmer

Semiconductors

1 74C926 4 digit counter/display driver
1 4518B dual decade counter
2 74196 decade counters
1 4017B Johnson decade counter
1 4027B dual J-K flip-flop
1 4011 quad NAND gate
1 MM5369 EYR/N 50Hz timebase
1 10116 ECL line receiver
1 7805 regulator
5 BC338 NPN transistors
2 2N4258 VHF NPN transistors
1 2N5485 VHF JFET
1 1N4002 diode
10 1N4148 diodes
2 BAW62 high-speed diodes
3 5mm red LEDs
4 FND500 (or equiv) common cathode 7-segment displays

Miscellaneous

6BA countersunk screws and nuts, PCB spacers, red perspex.

wires to the BNC socket to connect to the PCB when this is mounted after calibration.

Although some of the displays which can be used contain an integral red filter, a piece of red Perspex is used in the design presented here. This is because the board is mounted too far from the panel for the displays to protrude through it. A single filter covering the four digits also looks much neater than the separate ones built into the displays themselves. There are two ways in which to mount the filter, depending on your confidence in working with Perspex.

The easiest method is to cut out a rectangular piece of the material a little larger than the hole in the panel (say, 3 or 4mm on all sides), and glue it behind the panel. If you are prepared to invest a little more time, you could trim the Perspex so that it actually fits neatly *inside* the cut-out, and then glue it in place. If this is done carefully, the final appearance can be quite neat and tidy.

The only component which is not mounted on the PCB is the plug-pack socket. If you intend to dedicate a plug-pack to the counter, then it is probably best left off. Otherwise, it is mounted on the top end of the box, but far enough back from the front panel so that it will not hit the PCB when the lid is placed on the box. Solder a couple of pieces of hookup wire between the socket and the DC input pads on the board, being careful of the polarity.

Calibration

No measuring instrument is more accurate than the standard by which it is calibrated. Fortunately, because the counter is crystal-locked, it will be quite close even without calibration. However, if you have the equipment available, it is well worth the extra effort to calibrate it, especially if you intend to *overrange* the instrument in order to gain higher resolution.

The most obvious way to calibrate the unit would be to apply a stable frequency which is just below the maximum frequency of one of the lower four ranges to this counter and also to another of known accuracy, and adjust CV1 until the two instruments both display the same reading.

However a more direct approach is possible, thanks to the MM5369 IC. Pin 7 of this IC provides a buffered version of the actual crystal oscillator frequency. Therefore, simply adjust the trimmer until exactly 3.579545 MHz is read on another (calibrated) counter connected to pin 7.

All of this assumes that you have access to another frequency counter which is already calibrated. If this is not the case, probably the best that can be done is to set CV1 at about mid-range, and leave it there.

The three LEDs should now be inserted into their appropriate holes in the front panel, taking note of the polarity: all three have the flat on their body towards the top of the box. Now attach the completed board to the front-panel, while guiding the wires of the LEDs and the input socket through their respective holes. Put nuts on the two PCB support screws, and also on the selector switch, and then solder the LEDs and input socket to the board.

Your new counter should now be ready to be added to your range of test equipment.