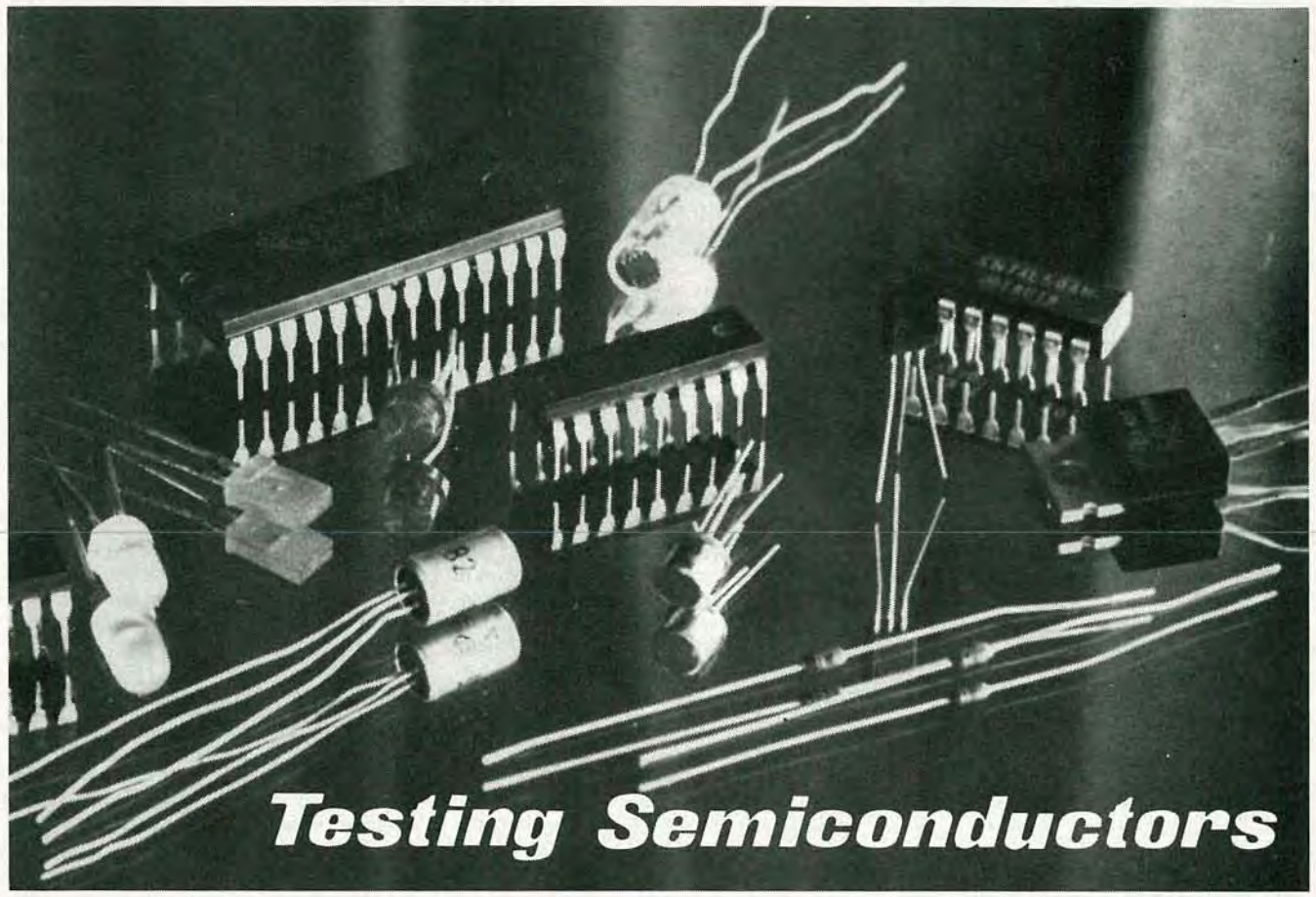

Testing Semiconductors

Our back-to-school series continues this month with a discussion of FET characteristics.

TJ Byers

Part 2 IN OUR LAST INSTALLMENT we investigated the static properties of the bipolar transistor. This time we'll turn our attention to the unipolar transistor, more commonly known as the *F*ield *E*ffect *T*ransistor, or FET.

There are two basic types of FET: the Junction FET (JFET) and the *M*etal-*O*xide *S*emiconductor FET (MOSFET). Like bipolar transistors, FET's comes in two "sexes:" N- and P-gate. In the test set-ups shown here, we'll use N-gate FET's. Those circuits can be adapted to P-gate types simply by reversing the polarities of voltage and current sources, and voltage and current meters.

JFET characteristics

The FET differs from the bipolar transistor in that it has only one junction. The FET is built as shown in Fig. 1. It is a bar of semiconductor material with a diode junction formed around its center. One end of the bar is called the source; the other is called the drain. The connection to the diode junction is called the gate.

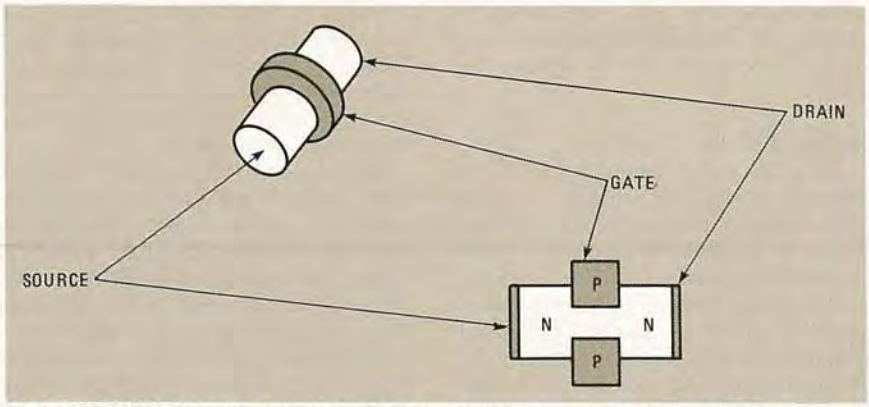

FIG. 1—THE JUNCTION FET is built from a bar of semiconductor material around which a diode junction is formed.

When voltage is applied across the semiconductor bar from source to drain, current flows unrestricted through that bar. If we reverse-bias the gate diode, however, an electric field forms within the bar. That field reduces the effective cross-sectional area of the semiconductor bar by forcing electrons from the voltage source toward the center of the semiconductor material. The smaller cross-sectional area represents an increase in resistance, which restricts the flow of electrons.

The strength of the field is proportional to the applied voltage. As the strength of the field increases, fewer electrons make their way through the tunnel, and current flow decreases proportionally. That phenomenon is called *the pinch effect;* it is what gives the FET its amplifying properties. As field strength increases, eventually it reduces the width of the tunnel so much that current ceases to flow. The voltage at which that occurs is called the cut-off or pinchoff voltage (V_P).

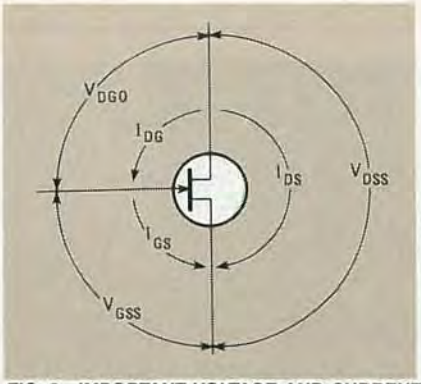

FIG. 2—IMPORTANT VOLTAGE AND CURRENT parameters of the JFET are shown here.

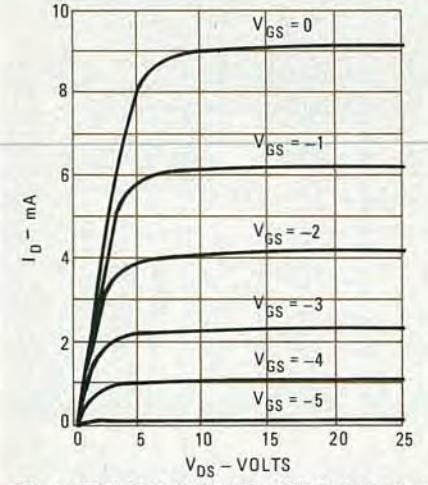

FIG. 3—CHARACTERISTIC CURVES of a typical JFET are shown here. In general, higher values of V_{DS} correspond to higher values of I_D.

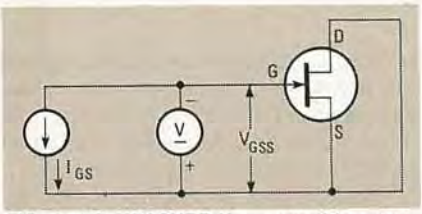

FIG. 4—TO MEASURE V_{GSS}, use this set-up. Gradually increase current (I_{GS}) to the point where further increase in current does not cause a corresponding increase in voltage.

Like the bipolar transistor, the FET has several important voltage and current characteristics; they are indicated in Fig. 2. The voltage characteristics each have three subscripted terms; the first two terms indicate the terminals between which the voltage is measured, and the third indicates the disposition the third terminal. The third term is either O (for open) or S (for shorted). So, for example, V_{DGO} represents the voltage between the drain and the gate, with the source unconnected (open).

In Fig. 2 the subscripted terms representing current indicate the terminals through which that current flows. For example, I_{DG} represents the current that flows from drain to gate.

WHAT IS A FET?

THE TERM FIELD-EFFECT TRANSISTOR IS GENERIC and covers several kinds of devices. But, basically, any semiconductor device whose operating characteristics are influenced by a controlled electric field qualifies as an FET. That generalization has led to the identification of three distinct FET types, labeled A, B, and C.

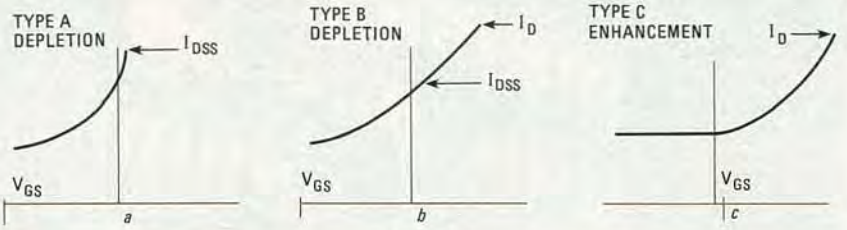

Fig. 1

The type-A FET is characterized as a depletion-mode transistor. As shown in Fig. 1-*a*, it operates only within the depletion-voltage section of the VI curve (quadrant II). In other words, with no voltage applied to the gate, current is free to flow between source and drain, restricted only by the lump resistance of the device. Increasing the negative gate voltage reduces I_{DS} to a very small amount.

The type-C FET, on the other hand, is an enhancement-mode transistor. As shown in Fig. 1-*c*, it requires gate voltage before current will flow from source to drain. At zero gate volts, zero drain current flows.

A type-B FET is a hybrid of the A and C types. It is basically a depletion-mode transistor with enhancement features. As shown in Fig. 1-*b*, at zero gate volts, a current equal to about half the maximum I_{DS} flows. A depletion voltage on the gate reduces I_{DS} and a positive gate input increases it. **R-E**

The characteristic curves of a typical FET are shown in Fig. 3. Each curve shows how I_D varies with V_{DS}, when V_{GS} is held constant. In the lower part of each curve, as V_{DS} increases, I_D increases proportionally. In that more-or-less linear portion of the curve, the FET displays its amplifying properties.

As the voltage across the FET continues to increase, the width of the depletion region (the tunnel) increases until further increases in V_{DS} cause no increase in current, as depicted by the flat parts of those curves. That area of operation is called the constant-current mode; it occurs when the gate-depletion field saturates the drain-to-source path.

If V_{DS} increases further, eventually the device goes into avalanche current multiplication. That occurs at the breakdown voltage of the transistor, which is represented by the term V_{DSS}. The avalanche current, if allowed to continue unchecked, eventually would destroy the transistor.

Testing JFET's

The static parameters of the JFET are measured in much the same way as those of the bipolar transistor. Leakage current is measured with a milliammeter (or microammeter) and a constant-voltage source. Breakdown voltages are determined by allowing a limited amount of current to flow through the device in the avalanche mode and measuring the voltage across the transistor.

Figure 4, for example, represents the setup for measuring V_{GSS}, the breakdown voltage of the gate-to-source junction. To make the measurement, apply a constant current to the diode junction in the reverse mode and measure the voltage across that junction.

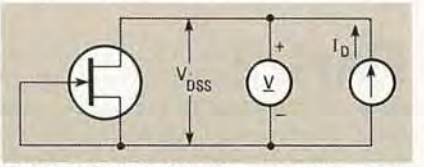

FIG. 5—TO MEASURE V_{DSS}, use this set-up. Gradually increase current (I_D) to the point where further current increase does not cause a corresponding voltage increase.

Note that that measurement is made with the drain shorted to the source. Many FET measurements require that several elements be tied together. Figure 5, for example, shows how to measure V_{DSS}. Generally, the values of V_{DSS} and V_{GSS} are identical, because in essence the gate is shorted to one end or the other of the semiconductor substrate.

In some cases it is necessary to apply a bias voltage to measure a particular parameter. V_{DS}, for example, is measured with a voltage applied to the gate. The voltage on the gate adds to the drain voltage, and that effectively lowers the breakdown voltage of the device. Sometimes a data sheet will identify that parameter as V_{DSX}, where X represents the test voltage applied to the gate.

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SEMICONDUCTORS

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The MOSFET

Developed after the FET, the MOSFET operates somewhat differently. Figure 6 shows the construction of an N-channel MOSFET. Fabrication begins with a slab of high-resistance P-type substrate. Two separate low-resistance N-type regions, called wells, are diffused into the substrate. Those islands represent the source and the drain. Next, a thin, high-resistance N-type region is created between the two wells.

Then a very thin layer of insulating metal oxide is deposited over the N channel separating the source and drain. On top of that layer is placed a metal contact, which becomes the gate of the transistor. Connections are then made to the drain and the source.

In operation, current flows between the source and the drain through the N channel. By applying a voltage to the gate, however, an electric field is created; it forces electrons to travel through the narrow part of the channel. As with the JFET, the field decreases the cross-sectional area of the path and increases its apparent resistance. That resistance decreases current flow in a manner that is proportional to the gate voltage. As gate voltage increases, eventually the electric field prevents the flow of electons altogether.

That description applies to the depletion-mode MOSFET. However, if we replace the N channel with a high-resistance P-type semiconductor, we have an enhancement-mode MOSFET. The enhancement MOSFET *requires* an electric field in its channel before it can conduct current. The stronger the enhancement field, the larger the path's cross-sectional area, and the lower its effective resistance.

MOSFET testing

Althought they are similar in many ways, a MOSFET cannot be treated like a JFET. In addition, not all tests performed on the JFET are applicable to the MOSFET.

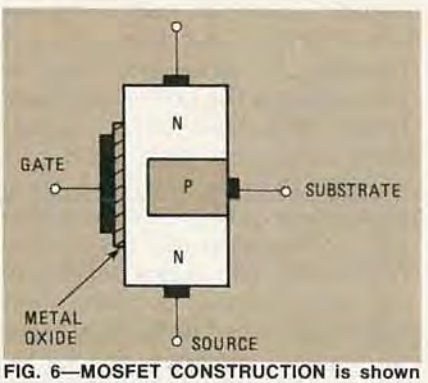

FIG. 6—MOSFET CONSTRUCTION is shown here. The oxide layer is usually silicon dioxide.

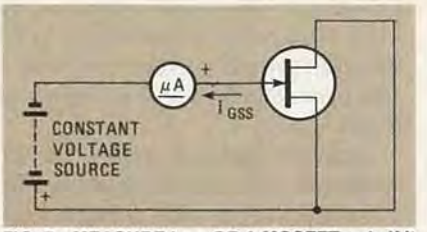

FIG. 7—MEASURE I_{GSS} OF A MOSFET only if it has protective input diodes!

Gate breakdown voltage (V_{GSS}), for example, is not a measurable quantity. The breakdown voltage of a MOSFET gate is determined by the thickness and the purity of the insulating layer. The thicker the layer, the more voltage it can withstand.

To properly measure a MOSFET's V_{GSS}, you must apply a gradually increasing gate voltage until the insulator fails. Unfortunately, when it does, the transistor becomes useless.

Manufacturers "measure" V_{GSS} by measuring the thickness of the insulating layer with sophisticated equipment, and then comparing the results to empirically derived failure curves. Tests of that type, however, are beyond the means of the experimenter.

Many MOSFETs, though, contain a diode in the gate junction that is intended to dissipate high-voltage spikes caused by static discharge. Those spikes could damage the transistor easily. The breakdown voltage of the protection diode is just below that of the gate.

So, if you are testing a protected-input MOSFET, you can measure V_{GSS} without damaging the transistor by simply applying enough voltage across the gate to force the diode into avalanche. Be sure to limit the current flow with a constant-current source so as not to destroy the protection diode. Now measure the voltage across the diode; it is close to the actual V_{GSS}.

Leakage current

Each breakdown-voltage parameter has a related leakage-current parameter. For example, I_{GSS} (*G*ate-to-*S*ource leakage current with drain and source *S*horted) is the term for input leakage of a FET; it is related to V_{GSS}.

Gate leakage is a very important characteristic of an FET because it is inversely related to input resistance. When leakage current is high, input resistance is low, and when input current is low, input resistance is high.

In many cases, you can measure leakage current with equipment similar to that used with bipolar transistors. A test circuit for measuring I_{GSS}, for instance, is shown in Fig. 7. I_{GSS} is normally measured at the V_{DSS} potential listed on the data sheet.

When measuring the I_{GSS} of a MOSFET, the measurement should be

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done in both the forward and the reverse directions, unless a protection diode is incorporated into the device. MOSFET's that have no protection diode should read the same in both directions. Because the insulating properties of the metal-oxide coating are far superior to those of a reverse-biased junction, the value of I_{GSS} in a MOSFET is considerably less than that of an FET.

Another current parameter often specified for FET's and MOSFET's is I_{DSS}, the drain-to-source leakage current with the gate shorted to the source. That test is often used to determine the amount of current flow in the constant-current mode.

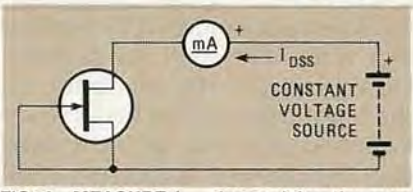

FIG. 8—MEASURE I_{DSS} by applying the manufacturer's stated value of V_{DSS} and reading the milli-ammeter.

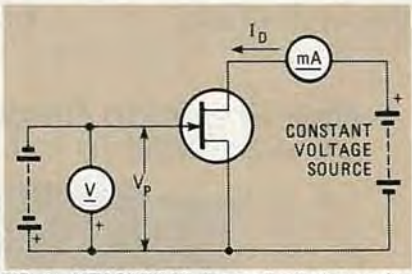

FIG. 9—MEASURE V_P by gradually increasing the gate voltage while monitoring I_D. When current stops increasing, V_P has been reached.

The circuit for measuring I_{DSS} is shown in Fig. 8. The drain voltage is maintained at the V_{DSS} value listed on the data sheet; then current is measured.

A circuit that combines both voltage and current measurements is shown in Fig. 9; that circuit is used to measure V_P. With no voltage on the gate, a normal depletion-mode transistor conducts current from source to drain. In order to halt that flow, a voltage must be applied to the gate. As stated earlier, the point at which source-to-drain current ceases to flow is called the pinchoff voltage. Sometimes you see that value listed as the cut-off voltage, which is a lingering term from our vacuum-tube past.

To measure V_P, gate voltage is gradually increased while drain current is monitored. When a change in gate voltage no longer produces a change in drain current, pinchoff voltage has been achieved. Ideally, current will drop to zero, but

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practically, however, there will always be a small amount of leakage current.

Enhancement-mode transistors, which require a voltage on the gate before they begin to conduct, do not have a pinchoff voltage. It is, obviously, zero. The counterpart to V_P is called *the threshold gate voltage*, or $V_{GS(TH)}$. The threshold voltage is defined as the voltage where I_D just starts to flow; it is measured by increasing the gate voltage until a perceptible increase in drain current is noted.

Whichever term is used (V_P or $V_{GS(TH)}$), the value represents the minimum operating current of the transistor.

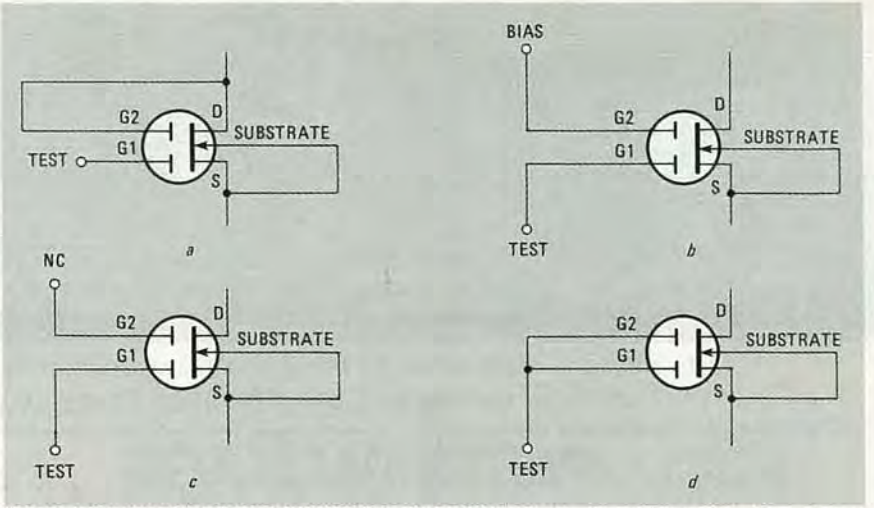

FIG. 10—CHARACTERISTICS OF THE DUAL-GATE MOSFET vary depending on how the gates are connected. The second gate can be connected to the drain (*a*), to the source (*b*), to nothing (*c*), or to the other gate (*d*).

Dual-gate MOSFET's

There is one more member of the FET family that we must look at: the dual-gate MOSFET. It's basically no different than other FET's, except for the additon of an extra control gate. That extra gate is useful for mixers, modulators, AGC circuits, and other applications.

All the test set-ups reviewed earlier are applicable to dual-gate MOSFETs—with one exception. Because there are two gates, the parameters of each gate must be measured separately. While one gate is being tested, the other gate can be configured in one of several ways.

First, as shown in Fig. 10-*a*, the unused gate could be tied to the drain.

Second, as shown in Fig. 10-*b*, the unused gate could be tied to the source, as it would be to measure V_{DSS}.

Third, and least desirable, as shown in Fig. 10-*c*, the unused gate could be disconnected from the rest of the circuit.

Last, as shown in Fig. 10-*d*, the two gates could be tied together. Doing so effectively makes the dual-gate MOSFET act as a single-gate MOSFET.

That does it for this session. In our next segment we'll look at several types of special-purpose diodes. **R-E**