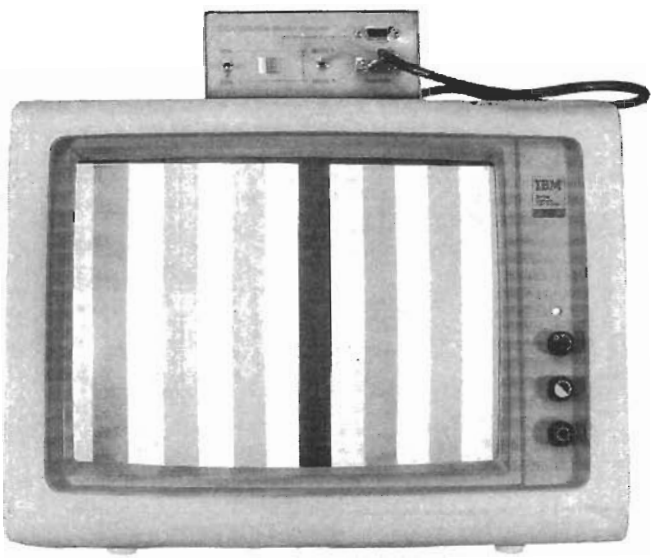
MONITOR TESTER

Our sync generator lets you test computer monitors without having to connect them to a computer.



GARTH PRICE, CET

SERVICING COMPUTER monitors isn't all too different from servicing composite-video monitors and television sets. There are some very important differences, however, the most obvious of which is that most computer monitors don't operate on the NTSC horizontal frequency of 15.734 kHz and vertical frequency of 59.94 Hz. Since your standard video test gear can't be used, you need a new troubleshooting tool—a computer-video sync generator.

We'll show you how to build a "sync generator" that provides horizontal sync, vertical sync, and RGB video for three popular styles of monitors: CGA, EGA, and VGA. Without connecting the monitor to a computer, you'll be able to verify video, deflection, and DC supply generation. Once repairs are made, fine tuning adjustments can be done with the monitor connected to a computer using appropriate software. However, using the sync generator first prevents tying up a computer that could be used more productively elsewhere.

Circuit description

The sync generator is a complex frequency-divider circuit. The starting point is two TTL clock oscillators—one is 5.0688-MHz (OSC1) and the other is 4.9152-MHz (OSC2). Depending upon two switch settings, one of the clock signals gets routed to various divider stages, ultimately leading to the final stage, a 4-bit binary counter.

VGA operation

Referring to the schematic in Fig. 1, switch S2, when closed, places a logic "0" (a low) on pin 1 of IC6, a 74HC158 quad 2-line to 1-line selector, so all "A" inputs will be passed to the "Y" outputs. The output of OSC1, a TTL clock oscillator, is then passed from pin 14 of IC6 (A4) to pin 12 (Y4) and then to the CLK input (pin 8) of IC3, a 74LS164 shift register. (**NOTE:** It is important that the EGA/VGA switch S2 is in the proper position for the type of monitor in use. An improper horizontal sync frequency can easily cause damage to deflection circuits!)

At the same time, the QE output of IC3 (pin 10) is fed through a 74HC14 Schmitt inverter (IC2-d) into the A3 input of IC6 (pin 11). That signal is then passed to the Y3 output (pin 9), through R10, to the base of Q1, and to IC3's CLR input (pin 9). As a result, the clock signal is divided by five and used as a reset, so every fifth clock pulse causes a clear to occur.

As just mentioned, shift register IC3 divides its CLK input (OSC1's output) by five (5.0688/5 = 1.01376). In other words, all of the "Q" outputs have a frequency of ⅕ the clock input, but only when the chip is reset by its own QE output. The QC output (which is also ⅕ the clock input when the chip is reset by QE) of IC3 (pin 5) sends the 1.01376-MHz signal to IC4-a's (a 74LS74 D-type flip-flop) CLK input (pin 3) where it is further divided by 2, so the net division is ten.

With that division by ten, a 506.88-kHz signal is sent to pin 2 of IC6 (A1), passed through to pin 4 (Y1), and on to binary counter IC5's (a 74LS163) CLK input (pin 2). Counter IC5 divides the signal by 16 to produce a horizontal sync of 31.68 kHz with a pulse width of 2 microseconds. Counter IC5 also divides the CLK input by two for generating blue (QA, pin 14), by four for red (QB, pin 13), and by eight for green (QC, pin 12). In other words, blue video is gated eight times the horizontal sync, red video four times, and green twice. The monitor thus lights up with yellow, cyan, green, magenta, red, blue, black, and white bars, and then repeats. (Note that the CGA/EGA

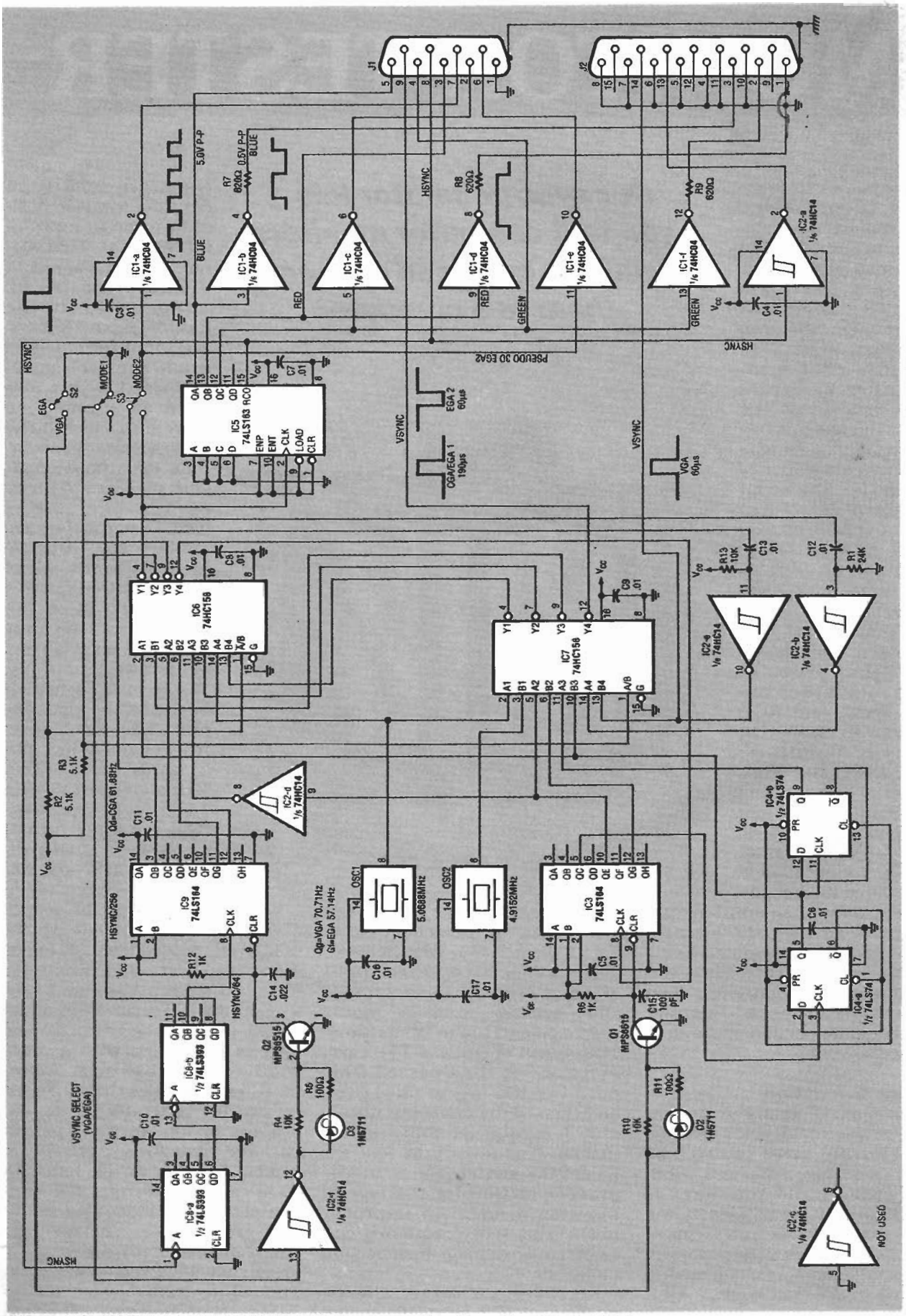


FIG. 1—MONITOR EXERCISER SCHEMATIC. When operating the unit, make sure that EGA/VGA switch S2 is in the proper position for the type of monitor in use. An improper horizontal sync frequency can cause damage to deflection circuits.

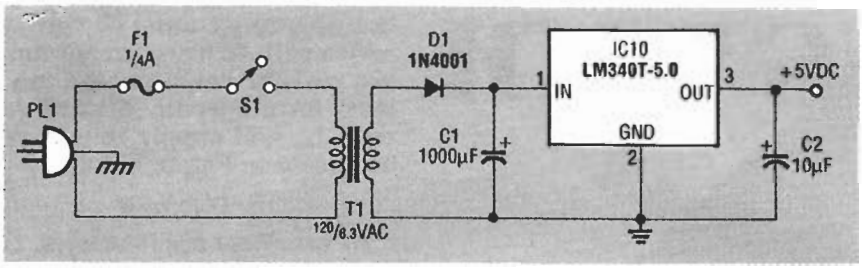


FIG. 2—POWER SUPPLY. If you don't have a suitable 5-volt DC power supply available, you can build this one.

color sequence is the reverse of VGA.)

Vertical sync is generated by sending horizontal sync to pin 1 of IC8-a, a 74LS393 binary counter, where it ends up divided by 64 at pin 10 of IC8-b and fed into the CLK input (pin 8) of IC9, another 74LS164 shift register. The CLR input to IC9 (pin 9) ultimately comes from its own QG output via IC6's A2 input (pin 5), its Y2 output (pin 7), Schmitt inverter IC2-f, and transistor Q2. Using IC9's QG output to reset itself causes a division of its clock input by 7. Therefore, the horizontal sync is first divided by 64 by IC8, then divided by seven by IC9, making a total division of 448. Therefore, a 70.71-Hz signal (31.68 kHz divided by 448) with a 60-µs pulse width is sent from IC9 pin 3 to pin 14 of J2, a 15-pin high-density VGA connector, via C13, R13, and Schmitt inverter IC2-e.

PARTS LIST

All resistors are ¼-watt, 5%.
R1—24,000 ohms
R2, R3—5100 ohms
R4, R10, R13—10,000 ohms
R5, R11—100 ohms
R6, R12—1000 ohms
R7–R9—620 ohms
R14—56 ohms
Capacitors
C1—1000 µF, 50 volts, electrolytic
C2—10 µF, 10 volts, electrolytic
C3–C13, C16, C17—0.01 µF, 50 volts, ceramic
C14—0.022 µF, 50 volts, ceramic
C15—100 pF, 50 volts, ceramic
Semiconductors
IC1—74HC04 hex inverter
IC2—74HC14 hex Schmitt trigger inverter
IC3, IC9—74LS164 shift register
IC4—74LS74 D flip-flop
IC5—74LS163 4-bit binary counter
IC6, IC7—74HC158 2-line to 1-line selector
IC8—74LS393 dual 4-bit binary counter
IC10—LM340T-5.0 5-volt regulator
OSC1—5.0688-MHz TTL clock oscillator
OSC2—4.9152-MHz TTL clock oscillator
D1—1N4001 diode
D2, D3—1N5711 Schottky diode
Q1, Q2—MPS6515 NPN transistor
Other components
F1—0.25-amp AGC fast-blow fuse
J1—DE9S 9-pin female connector
J2—HD DB15S 15-pin high-density female connector
S1, S2—SPST switch
S3—DPDT switch
T1—120/6.3VAC transformer
Miscellaneous: AC linecord, wire-wrap IC sockets, metal enclosure, wire, solder, etc.

CGA/EGA1 operation

When switch S2 is set to "EGA," it places a logic "1" (a high) on pin 1 of IC6, which then connects its "B" inputs to the "Y" outputs. When S3 is set to "Mode 1," it places a logic "0" (a low) on pin 1 of IC7, another 74HC158 selector, which connects its "A" inputs to the "Y" outputs. Now IC7 uses OSC1 as its timing source which is input at pin 2 and output at pin 4. That, in turn, is input to pin 13 of IC6 and output at pin 12. From pin 12 of IC6, OSC1 is to IC3's CLK input (pin 8). Because IC3's QE output (pin 10) is tied back to its CLR input (pin 9) via IC7 pins 5 and 7, IC6 pins 10 and 9, R1, and Q1, IC3 divides OSC1 by five.

Output QC of IC3, which is also OSC1/5 because QE is used as the clear signal, routes 1.014 MHz (5.0688/5) to pin 3 of IC4-a, causing further division by four at pin 9 of IC4-b for a total division of 20 (253.44 kHz). The 253.44-kHz output from IC4 pin 9 is connected to pin 3 of IC6 via IC7 pins 11 and 9. The input to pin 3 of IC6 is output at pin 4, and from there it goes to S3 and the CLK input of IC5 (pin 2). After IC5 divides the 253.44 kHz by sixteen, the horizontal sync measures 15.84 kHz.

Vertical sync is generated by dividing horizontal sync (15.84 kHz) by 256 at pin 8 of IC8. That output connects to C12, R1, IC2-b, and pin 14 of IC7. The 61.88 Hz vertical sync signal with a 190 µs positive pulse width is then sent to pin 9 of output jack J1 via IC7 pin 12.

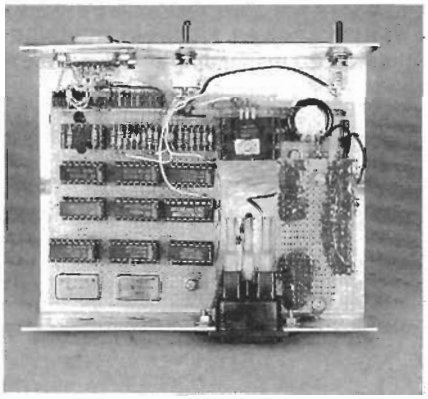


FIG. 3—THE AUTHOR'S PROTOTYPE. Perforated construction board and wire-wrap techniques were used to assemble the project.

EGA2 operation

When S2 is set to "EGA," it places a high on pin 1 of IC6, which then selects its "B" inputs. With S3 set to "Mode 2," it places a high on pin 1 of IC7 so it also selects "B" inputs. With the "B" inputs selected, IC7 uses OSC2 as its timing source and 4.9152 MHz passes from pin 4 of IC7 to pin 13 of IC6. The signal then connects to IC3's CLK input (pin 8) from pin 12 of IC6. The QG output from IC3 is connected to IC6 pin 10 via IC7 pins 6 and 7. The signal is then output at pin 9 of IC6, and connects back to the CLR input (pin 8) of IC3. The OSC2 signal is divided by seven by IC3 producing 702.17 kHz at IC3's QC output. The QC output from IC3 ties to IC4-a, which causes an additional division by 2, for a net of 14. The 351.08 kHz from IC4-a pin 5 is connected to IC5's CLK input (pin 2) via IC7 pins 10 and 9, and IC6 pins 3 and 4. The signal is further divided by

continued on page 94

16 by IC5 to produce a horizontal sync of 21.94 kHz.

Vertical sync is generated by dividing the horizontal sync by 64 at IC8's Q_B output (pin 10). The Q_F output of IC9 connects back to its own CLR input via IC6 pins 6 and 7 causing IC9 to divide by 6, for a net division of 384. That gives us a vertical sync of 57.14 Hz at IC9's Q_A output. That Q_A output is connected to IC2-e pin 11, which is configured as a one-shot, and outputs a 60-microsecond negative pulse to IC7 pin 13. The pulse is output at pin 12 of IC7 which is connected to pin 9 of connector J1. Switch S3 routes 351.08 kHz to the low-byte RGB inputs of an EGA monitor. That causes the monitor to display a pseudo three-dimensional pattern to display on the monitor.

As a few final notes, VGA RGB inputs are 75-ohm impedance. Resistors R7–R9 reduce the amplitude of the color signals to 0.5-volt p-p. 400-line operation is produced by making horizontal sync negative polarity and vertical sync positive. EGA monitors switch from Mode 2 (enhanced) to Mode 1 by changing the polarity of vertical sync; in Mode 1 it's positive, in Mode 2, it's negative.

Construction

The use of perforated construction board and wire-wrap is recommended for this project. Try to keep the TTL clock oscillators (OSC1 and OSC2) as close to IC6 and IC7 as possible. Also, decouple all IC's and the oscillators with the 0.01 μF ceramic disc capacitors as shown in the schematic in Fig. 1. (You can solder them directly to the V_{CC} and ground wire-wrap pins).

This project requires +5-volts to operate. If you've already got a suitable power supply you can use it. Otherwise, Fig. 2 shows a suitable one for the project.

Once the circuitry is completed, you should put the assembled boards in a metal project box and tie earth ground to the case. Figure 3 shows the author's completed prototype. **R-E**