Winner of 2nd prize in the Parameters-EA contest:

Improved Logic Probe for TTL & CMOS

Here is the design which won second prize in the Parameters/EA Grand Instrument Contest No. 1. Much lower in cost than comparable commercial probes, it offers high input impedance, one-shot pulse stretching, "open" and "short to rail" detection, and the ability to test both TTL and CMOS circuitry.

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Although many logic probe designs have appeared from time to time, most have been very limited in their range of applications, and suffered from low input impedances. Based on three common IC's, this probe boasts six displayed conditions in TTL and four in CMOS. It operates from supplies between 5 and 15 volts and its inherent high input impedance (approximately 3 megohms) ensures minimal loading upon the gate under test. Beside the normal high and low levels, shorts to positive and negative rails (TTL only), incorrect (mid rail) levels and pulses down to less than 1 microsecond are detected and displayed.

The probe was designed with compactness and simplicity of circuitry in mind and to this end 0.125in LEDs were chosen as a display medium. To remove any ambiguity, orange LEDs were used for short to rail, green for high, red for low and orange for pulses. The incorrect level state is shown by an absence of any display.

Referring to the circuit diagram, it will be seen that IC1, an LM324 quad op amp, has each of its elements connected as voltage comparators with one input connected to a fixed reference voltage and the other commoned to the input probe. The outputs of IC1 are decoded by IC2, a 7400 NAND gate, which also drives the display. The 555 timer IC3 is arranged as a non-retriggerable, negative edge triggered monostable with an output pulse of approximately 300 milliseconds.

The input probe is held under quiescent conditions at approximately 37% of the rail voltage by R1 and R2 and the voltage at this point is fed via R3 to pins 3, 6, 9 and 12 of IC1. Section A of IC1 is used to detect shorts to the positive rail. Its inverting input, pin 2, is held at a reference of 50mV from the positive rail by resistors R4 and R5.

Logic high is detected by IC1B. The reference voltage at the inverting input, pin 12, is changed for CMOS or TTL circuits by Switch SW1A. In the TTL position the reference of 2.4 volts is obtained from resistors R6, R8 and R9, while the combination of R6 and R7 provide a reference of approximately 70% of rail voltage for a CMOS high.

When the input voltage on the probe exceeds the references of IC1A and IC1B, output pins 1 and 14 go high. The diode-resistor combinations R16-D1 and R18-D2 limit this voltage to a compatible level for IC2.

The last two sections IC1C and IC1D are used to detect logic low and shorts to the negative rail respectively. Resistors R14 and R15 form the 50mV from rail reference, which is connected to pin 10 of the non-inverting input of

LIST OF PARTS

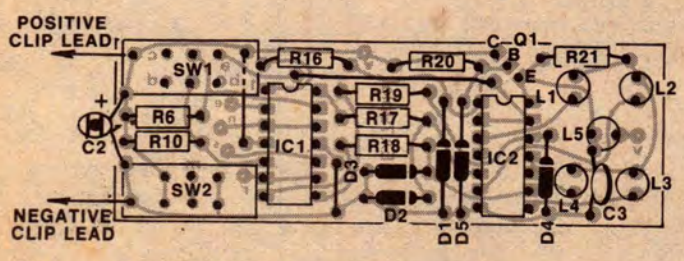
PCB 79/pl/a, 79/pl/b
IC1 LM 324 quad op amp
IC2 7400 quad gate
IC3 555 Timer
L1-5 3mm LEDs (three orange, one red, one green)
PCBs (2) 81 x 26mm, 79p1a/b
Q1, Q2 BC182-3-4 or similar
D5 5.6V/400mW Zener
D1-4 3.3V-4.7V/400mW Zeners

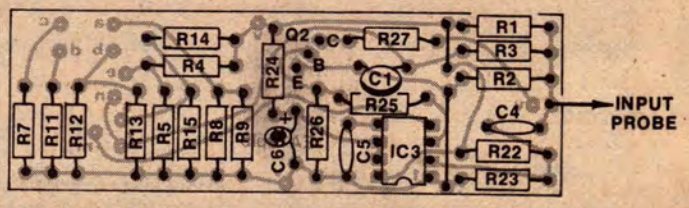
RESISTORS (all ¼ or ½W 5%)

R1 5.6M
R2 3.3M
R3 27k
R4 100 ohms
R5 10k
R6 1.5k
R7 3.3k
R8 1.5k
R9 15k
R10 3.3k
R11 1.5k
R12 680 ohms
R13 8.2k
R14 10k
R15 100 ohms
R16 560 ohms
R17 560 ohms
R18 560 ohms
R19 560 ohms
R20 330 ohms
R21 470 ohms
R22 3.3M
R23 2.7M
R24 330k
R25 2.2k
R26 470 ohms
R27 470 ohms

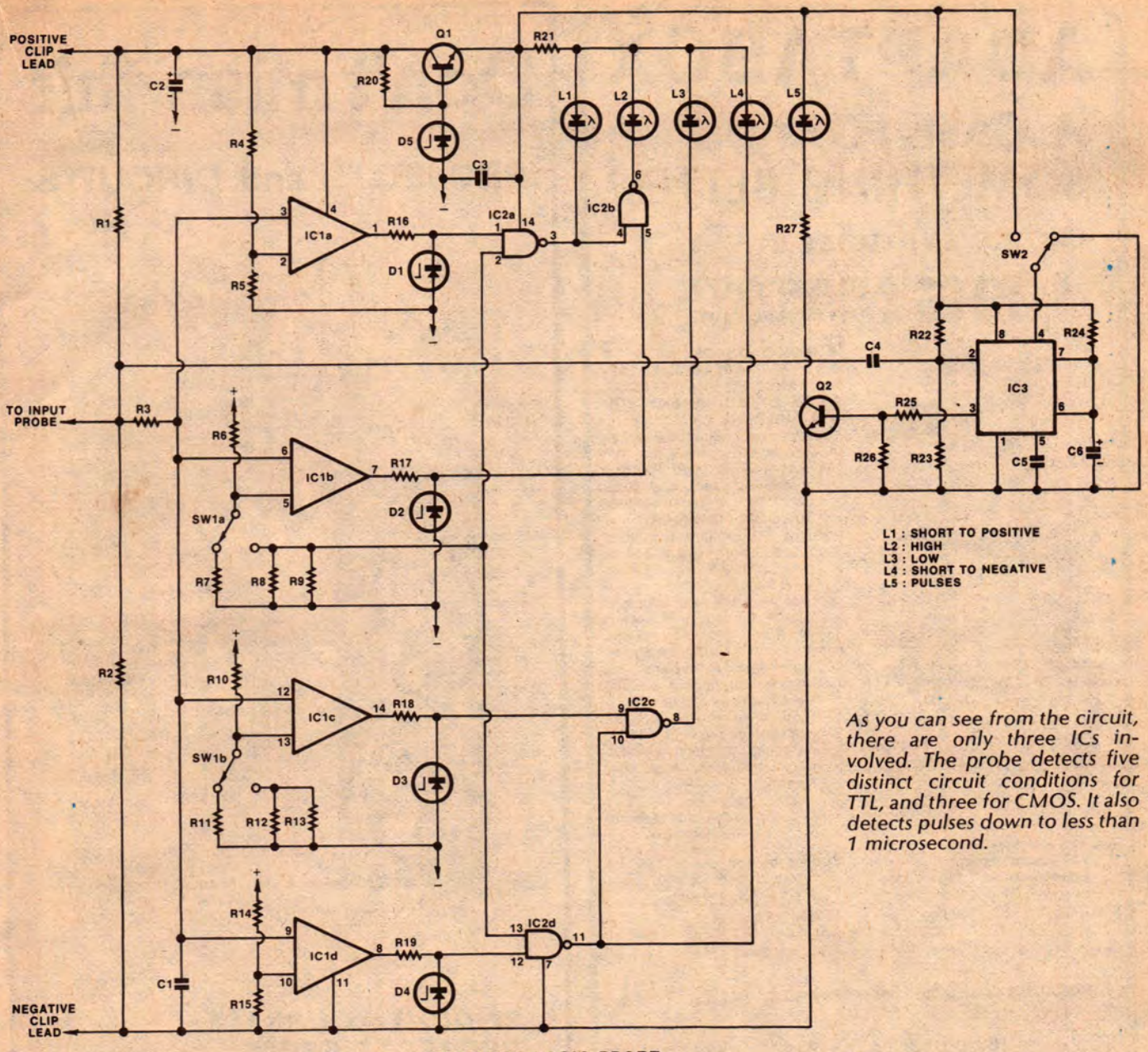
CAPACITORS

C1 .047uF 50V disc ceramic
C2 10uF 20V tant. bead
C3 0.1uF 50V disc ceramic
C4 .01uF 50V mylar or polyester
C5 .01uF 50V mylar or polyester
C6 1uF 20V tant. bead
Note: Smallest physical size is the most important parameter for C4 and C5.
SW1 Miniature DPDT slider.
SW2 MINIATURE DPDT slider.





Here are the overlay diagrams for the two PC boards.



TTL-CMOS LOGIC PROBE

As you can see from the circuit, there are only three ICs involved. The probe detects five distinct circuit conditions for TTL, and three for CMOS. It also detects pulses down to less than 1 microsecond.

IC1D. The logic low reference for TTL is derived by R10, switch SW1B, R12 and R13 and is set at 0.8V. The CMOS low reference of approximately 30% rail voltage is formed by R10, switch SW1B and R11.

Like the "short to rail", the "low" reference is connected to the non-inverting input, pin 5, so that when the probe goes low and the voltage falls below these references, output pins 7 and 8 go high. As with the previous sections the resistor-diode combinations limit this voltage to a TTL compatible level. The value of the zener diodes D1 to D4 can be anything from 3.3 volts to 4.7 volts.

IC2 drives the respective LEDs, and also performs gating to prevent the normal "high and "low" logic level LEDs from being illuminated in "short to line" situations. This is done by connecting the outputs of IC2A and IC2D to the second inputs of IC2B and IC2C, as shown. As a result, if either of the "short to line" situations is detected, sending the output of IC2A or IC2D low, this holds the output of IC2B or IC2C high and prevents the second LED from illuminating.

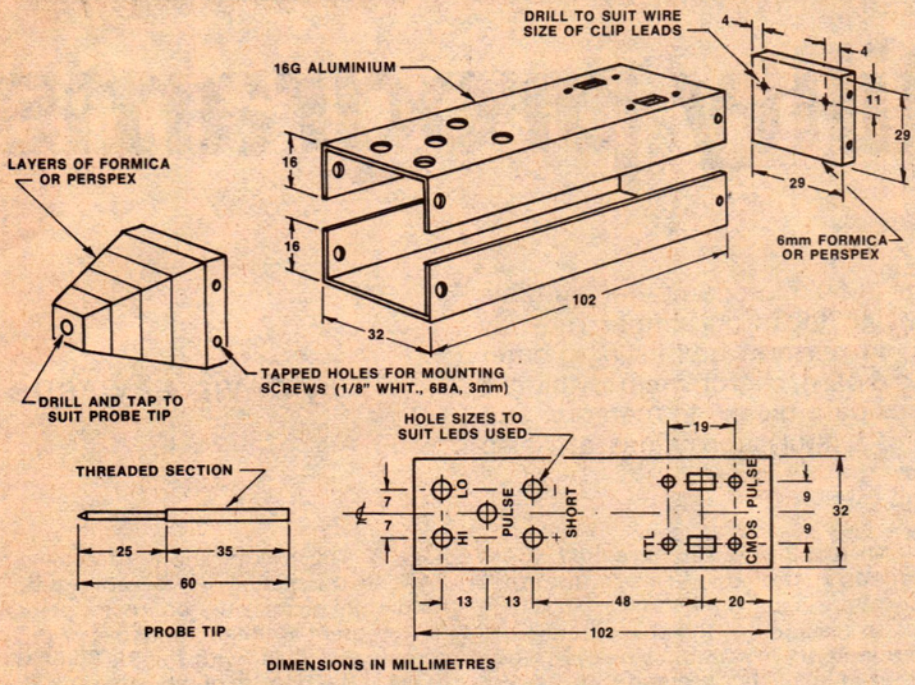
Because with CMOS the difference between a normal low or high and the rail voltages is only a few millivolts, a "short to rail" indication is impractical. IC2 is therefore arranged also to disable the "short to rail" LEDs when the probe is switched for CMOS levels. This is done by connecting pins 2 and 13 to the top of the R8/R9 combination. When SW1A is switched to the TTL position, this point becomes a logic high, enabling both IC2A and IC2D and the "short to rail" LEDs; but when SW1A is switched to the CMOS position pins 2 and 13 fall to the low logic level, disabling the LEDs.

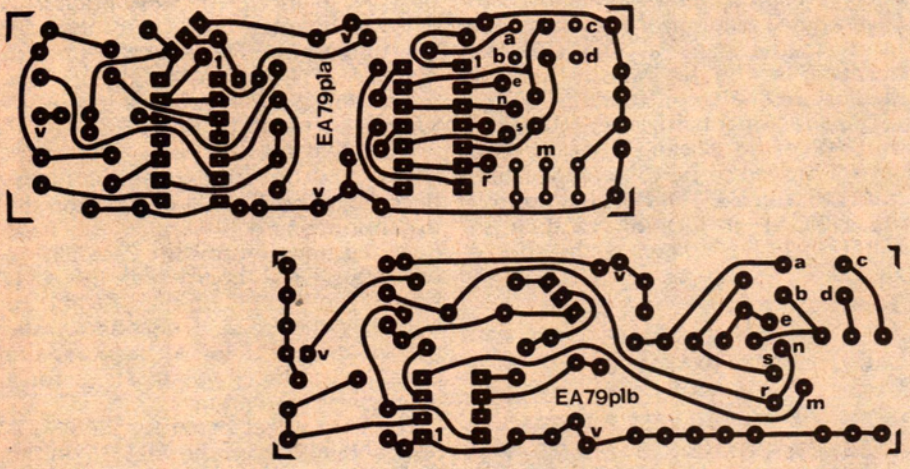
The five volt rail required for IC2 is provided by a simple series regulator comprising Q1, R20 and D5. To maintain a constant light output over the wide voltage variations of the probe, this rail also supplies the LEDs, with R21 and R27 limiting the current.

IC3 is the pulse detector. Resistors R22 and R23 help increase its sensitivity so that in practice, pulses even shorter than 1us and pulse trains in excess of 5MHz are still detected. Transistor Q2 inverts the output and drives the "pulse" LED. The switching of pin 4 by SW2 enables this LED to be held off when not required as it would pulse every-time the probe is brought into contact with a LOW.

The method of construction of the probe will depend largely upon the resources and ingenuity of the constructor. The layout shown consists of two PC boards mounted inside a folded

Improved TTL-CMOS logic probe . . .





Full details of the probe housing are shown in the upper diagram, with the PCB patterns shown actual size below.

aluminium case but equally well, it could be made in any type of container that has a minimum internal dimension of 29mm square by 90mm in length.

The components and links, with the exception of the LEDs and switches are assembled on the boards as shown in the diagram. Next the LEDs are mounted in the case and the legs of the outer four bent to suit the PC board. The switches are fitted to the case and 20mm lengths of tinned copper wire are soldered to their terminals. Lengths of wire are also soldered to the pads marked "e", "n", "s" and "r".

Board "A" is now fitted onto the legs of the LEDs and switches and soldered into place. The legs of the LEDs are trimmed as are the centre wires of switch SW1, the outer and unmarked centre wire of the switch SW2.

Three Vero pins (large) are used to space the boards and also provide positive and negative supplies to board "B" as well as a connection between the pulse LED and transistor T2. These pins are soldered to the pads marked "v" on each board. Board "B" is now fitted in place and all spacers and interconnecting wires are soldered and trimmed. The voltage supply clip leads are connected to board "a" and pass through holes in the end of the case; they should be 400-500 mm in length. The input probe is connected to board "B" via a short length of hookup wire.

It is difficult to estimate a cost for building this probe, but purchasing everything at retail prices, it should not involve more than $25.00, which should compare more than favourably with commercially available probes.