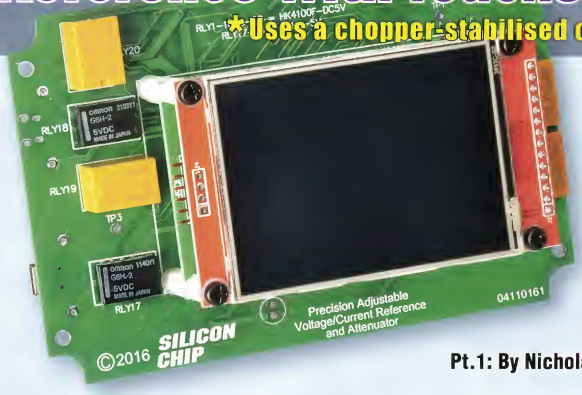
Precision Voltage & Curren
Reference With Touchscree

★ Uses a chopper-stabilised op amp



Pt.1: By Nicholas Vinen

This new design lets you produce any voltage from 0-37V with 0.1% or better accuracy, with the convenience of a touch-screen interface. It can also act as a precision current source or sink from 1mA to several amps (with up to 2.5W continuous dissipation) and is largely self-calibrating. It can also be used as a precision AC signal or DC voltage attenuator/divider.

WE CAME UP with the idea for this project after selling hundreds of kits for the Accurate Voltage/Current/Resistance reference project described in the August 2015 issue. That project's popularity is no doubt due to its simplicity and low cost to build. But it's also quite limited, with just one reference voltage, one unbuffered current option and one resistance value.

So we decided to come up with a new project which would be a lot more useful, offering a huge range of reference voltages and currents without being too expensive, large or difficult to use. This unit is the result.

We decided to use the Micromite LCD BackPack as the user interface. This makes the user interface nice and simple, with no buttons or knobs – all settings are done via the touchscreen. You can simply punch in a voltage or current value or attenuator ratio. Or you can swipe to adjust the already set value. It also gives a nice clear read-out of the current state of the unit. We also decided it should be powered from a USB socket, due to the prevalence of suitable supplies, both mains-based and battery-based.

The PIC32 in the LCD BackPack does all the control work, so we just needed to add a precise voltage source, an accurate gain stage and programmable divider, a voltage-to-current converter, a boosted supply to provide a usefully wide voltage range and some switching to allow the user to easily switch between the various modes.

Design process

We immediately decided to use the same Maxim voltage reference IC as the earlier reference project. It has the advantage of being relatively cheap

n Control

with a good basic accuracy of ±0.04% and low noise.

To attenuate its output, we considered using either a precision DAC or a discrete "R-2R" resistor ladder network switched by relays, like Jim Rowe used in his Lab-Standard 16-Bit Digital Potentiometer project, from the July 2010 issue.

You would think a single DAC IC would be the cheaper option but high-precision DACs are surprisingly expensive. We now have sources of suitable relays and high-precision SMD resistors that are cheap enough that the discrete option ends up being the same cost, or even lower.

Using a DAC IC would give us the ability to quickly vary its output, eg, for pulse testing purposes. However, that is not the primary intention for this project; it was envisioned more as a DC reference so that was not considered an important feature. Anyway, the relays do allow for output "bursts" as long as they are not too short.

The discrete ladder approach has further advantages which convinced us to stick with this approach. It allows the unit to be used as an attenuator for a wide range of external AC signals or DC voltages, including those which swing below ground. It also provides full isolation from the unit's own power supply in this mode.

Double-sided PCB

By producing a double-sided PCB which is stacked with the LCD Back-Pack PCB, we can easily fit the 16 relays and 50-odd resistors required for the precision attenuator into a standard jiffy box, with room for the other components required to provide the various extra modes.

Besides having more features, another important advantage of this design over the Lab-Standard Digital Potentiometer is the fact that our R-2R ladder uses resistors which are all the same value. This is made possible since precision SMD resistors are both smaller and cheaper than their through-hole equivalents, so we could simply create one value by combining two resistors.

We're using pairs of 12kΩ 0.1% resistors in parallel to form 6kΩ 0.1% resistances, so the R/2R ladder is in fact 6kΩ/12kΩ. This gives a divider impedance four times that of the earlier design, which used 1.5kΩ/3kΩ. This keeps the input impedance above 3kΩ at all times, making it easier to drive from an external source. The higher output impedance is partially solved by adding an optional buffer.

Using a single value gives us the benefit of the fact that resistors from the same batch are likely to be closer in value to each other than the tolerance would otherwise suggest. In addition, they should also have closely matched temperature coefficients, so the division ratio should not drift much with temperature.

Another advantage of this scheme is that the actual resistor value is not critical. If the 12kΩ resistors become difficult to acquire or expensive, constructors can simply substitute 10kΩ or another similar value. As a bonus, you can take advantage of the volume discounts often available when buying 50 or more resistors of the same value.

Chopper-stabilised op amp

As well as the precision divider and voltage reference, we have added an op amp to provide reference voltage gain, to expand the range of available output voltages. This op amp uses a boosted supply so that the 5V USB input isn't a limiting factor.

Features & Specifications

- Four modes: AC/DC attenuator/divider without buffering, AC/DC attenuator/divider with buffering, voltage reference, current reference
- Interface: 320 x 240 pixel colour TFT touchscreen
- Power supply: 5V 1A USB supply (micro or mini connector)
- Protection features: over-voltage disconnect (buffered attenuator & voltage reference mode); over-voltage, over-current & over-heat disconnect (current sink/source mode)

Unbuffered attenuator/divider mode

- Maximum input voltage: ±60V
- Input impedance: variable, displayed on screen; 3.5-114kΩ
- Output impedance: fixed; 2.4kΩ
- Attenuation steps: 65,535
- Attenuation accuracy: typically within ±0.01%

Buffered attenuator/divider mode

- Input voltage range: 0-38V
- Input impedance: variable, displayed on screen; 3.5-114kΩ
- Output impedance: effectively 0Ω
- Output current: 12mA source; 12mA sink above 1V, reducing to ~5mA @ 0V
- Bandwidth: >50kHz
- Attenuation steps: 65,535
- Attenuation accuracy: typically within ±0.01%

Voltage reference mode

- Output voltage range: 0-5V in 0.1mV steps; 5-10V in 0.5mV steps; 10-37V in 1mV steps
- Output current: 12mA source; 12mA sink above 1V, reducing to ~5mA @ 0V
- Uncalibrated accuracy: ±2mV 0-2.5V; ±3mV 2.5-5V; ±5mV 5-10V; ±10mV 10-20V; ±20mV 20-37V
- Typical output noise (1MHz BW): <200µV RMS 0-2.5V; <5mV RMS 2.5-37V
- Typical output noise (50kHz BW): <100µV RMS 0-2.5V; <500µV RMS 2.5-37V

Current reference mode

- Output current range: 0.5mA-5A in 0.5mA steps.
- Maximum applied voltage: 30V
- Calibrated current reference accuracy: typically better than ±0.1%
- Continuous sink/source current: up to 83mA
- Continuous dissipation: up to 2.5W
- Peak dissipation: 50W (10ms), 20W (100ms)

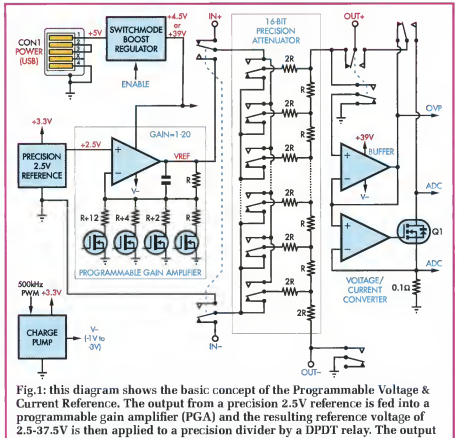


Fig.1: this diagram shows the basic concept of the Programmable Voltage & Current Reference. The output from a precision 2.5V reference is fed into a programmable gain amplifier (PGA) and the resulting reference voltage of 2.5-37.5V is then applied to a precision divider by a DPDT relay. The output of the divider can be accessed directly at the OUT+ terminal or optionally routed through either a buffer op amp or a voltage-to-current converter.

For this, we need an op amp with a very low input offset voltage, to avoid prejudicing the accuracy of the reference, along with low drift, low noise and a very low input bias current, to avoid errors due to the divider's output impedance (when acting as a buffer).

We originally planned to avoid chopper-stabilised op amps because, while they have a very low input offset voltage, they tend to have high noise due to the "chopping" (switching) action. However, in the end, the op amp we found that best suited our needs at reasonable cost is of this type, albeit one with very low noise.

It's the ADA4522-4ARZ from Analog Devices which has four op amps in one package, a maximum input offset of just 5μV, drift of just 2.5nV/°C, a low typical input bias current of 50pA (maximum 150pA @ 25°C) and very low noise at just 5.8nV/√(Hz). As a bonus, it will run off a supply voltage of up to 55V. We decided on 39V (since the boost regulator's internal Mosfet is rated at 40V peak), allowing reference voltages up to about 37.5V.

This quad op amp not only provides the gain stage but also drives a voltage-to-current buffer, allowing the unit to sink or source a programmable current between 0.5mA and 5A (within certain dissipation limits). Another of its stages is used as an optional output buffer.

Operating principle

Block diagram Fig.1 shows the basic operation of the device. We're ignoring the LCD BackPack and its control logic, for the moment. At its heart is a 16-bit precision attenuator with all the switching done by relays. With the control relays in their off (default) states, the positive and negative input voltages for the precision attenuator come from an external voltage source via the IN+ and IN- banana sockets. Similarly, the divided voltage, with the attenuation ratio set by the state of the 16 relays in the R-2R ladder network, appears across the OUT+ and OUT- terminals. Normally, OUT- and IN- are both connected externally to GND.

A DPDT relay can switch the IN+ and IN- terminals out of the circuit and connect the input side of the attenuator to the output of the programmable gain amplifier (PGA) instead. This is fed from the 2.5V precision reference. With the four PGA Mosfets off, the attenuator receives 2.5V and this can be divided into 65,536 discrete voltages at the OUT+ terminal; the OUT- terminal can be internally connected to ground via a relay, for convenience.

Should a voltage above 2.5V be required, the switchmode boost regulator can be enabled, raising the PGA op amp's supply voltage from USB 5V up to 39V. Its gain can then be increased to give a reference voltage from 5V to 37.5V, increasing the range of output voltages available from the divider.

A simple charge pump driven by the micro in the LCD BackPack provides a negative rail for the op amp that's typically 1-3V below ground, so that its outputs can reach 0V even when sinking several milliamps. This is a common issue with "rail-to-rail output" op amps; while in theory their outputs can swing to the supply rails, in practice they usually fall a bit short.

A DPDT relay at the OUT+ terminal can insert one of these high-precision op amps in series with the output, to buffer the voltage. The relay shown at upper right switches the buffered output from voltage mode to current mode. In this mode, current from the OUT+ terminal passes through Mosfet Q1 to the OUT- terminal. An op amp varies Q1's gate voltage so that it sinks the programmed current, by monitoring the voltage across the 0.1Ω shunt and comparing it to the reference voltage from the divider.

Finally, the micro in the BackPack uses its analog-to-digital converter (ADC) to monitor the dissipation in Q1 along with its drain voltage and current, and the voltage at the output of the buffer op amp. It can then disconnect the output terminal from this circuitry should any of these be driven outside their design ranges.

Circuit description

Fig.2 shows the full circuit diagram of the Precision Voltage & Current Reference. The main 2.5V reference is provided by REF1, a MAX6071-2.5 with an initial accuracy of ±0.04%. Its power supply is derived from the regulated 3.3V rail of the BackPack module via an RC low-pass filter (100Ω/4.7μF) in order to cut out switching hash from the microcontroller. We're using the 3.3V supply as it's likely to be less noisy than the unregulated 5V input.

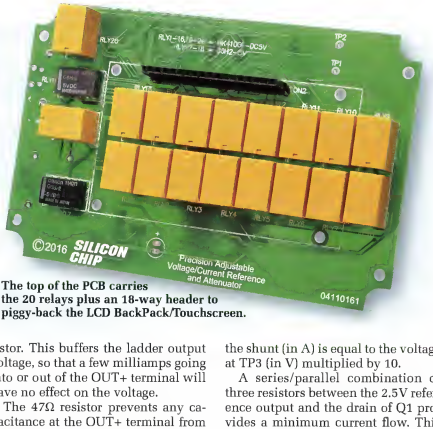
The 2.5V output is fed to IC5a which forms the PGA. By default, with outputs O4-O7 of IC3 in their high impedance state, the op amp's feedback is via the 12kΩ resistor and parallel 100nF capacitor (for stability and noise re-

duction) and this gives unity gain, ie, V_{REF} = 2.5V.

However, if IC3's output O4 switches low, this forms a 1:1 divider (ie, 12kΩ/12kΩ) and so the op amp gain becomes two, giving V_{REF} = 5V. The 0.1%-tolerance resistors ensure this value is close to ideal but any error is automatically calibrated out, as explained later.

Similarly, if O5 switches low, the gain becomes four times and V_{REF} = 10V. Various combinations of O4-O7 can be switched to give a gain of 1-19, resulting in a V_{REF} between 2.5V and 37.5V.

When V_{REF} = 2.5V, IC5a runs from the 5V supply via Schottky diode D1 and inductor L2, resulting in around 4.5V. Before the PGA gain is set above unity, pin 12 of CON2 is brought low, enabling boost regulator REG1. This lifts IC5a's supply voltage up to 39V [1.276V x (22kΩ ÷ 750Ω + 1)]. The operation of REG1 will be explained later.



The top of the PCB carries the 20 relays plus an 18-way header to piggy-back the LCD BackPack/Touchscreen.

Voltage divider

When relay RLY18's coil is energised, V_{REF} is connected to the top end of the R-2R divider ladder while the bottom end is connected to GND. On the PCB, the GND connection is routed so that no additional current will flow along this path, ensuring accuracy; just that passing through the ladder.

The ladder itself consists of 47 12kΩ 0.1% tolerance resistors, chosen for the reasons explained earlier. Relays RLY1-16 connect various points in the R-2R ladder to either GND of V_{REF}. Depending on which combination of these relays are energised, the ladder output at TP3 ranges between GND and just a tiny bit below V_{REF}. For example, if RLY16 is energised and the other 15 are not, assuming all components are exactly the expected value, that will give V_{REF} x 32768 ÷ 65,535 or just slightly more than V_{REF}/2 at TP3.

When RLY17 is not energised, this voltage is available at the OUT+ terminal. Normally, RLY19 will be energised and so the OUT- terminal will be connected to GND.

Output buffering

When RLY17 is switched on, the voltage at TP3 is routed to the non-inverting input of op amp IC5c, another high-precision op amp. At the same time, this op amp's output is connected to the OUT+ terminal, via RLY20's normally-closed contact and a 47Ω resistor. This buffers the ladder output voltage, so that a few milliamps going into or out of the OUT+ terminal will have no effect on the voltage.

The 47Ω resistor prevents any capacitance at the OUT+ terminal from destabilising op amp IC5c. This would normally cause a voltage shift, however, this op amp stage actually has "zero DC output impedance" due to the 10kΩ resistor between the output end of the 47Ω resistor and the inverting input. In other words, DC feedback comes from the output end of the 47Ω resistor. But AC feedback comes from the other end, via a 47pF capacitor, so the op amp still benefits from the stability improvement provided by the 47Ω resistor.

Current sink & source

In current reference mode, RLY20 is energised. The OUT+ terminal is then connected to the drain of N-channel Mosfet Q1 and its source is connected to GND (and thence to OUT-) via a nominal 0.1Ω shunt. The voltage from this shunt is proportional to the current sunk by Q1 and this is fed back to the inverting input of IC5d, another precision op amp stage, via an RC filter.

The non-inverting input of this op amp, pin 12, is connected to the output of buffer stage IC5c via a 1kΩ resistor. So, as an example, let's say V_{REF} = 2.5V and the R-2R ladder is set up to divide this by 100, ie, with 25mV at TP3. This 25mV is applied to pin 12 of IC5d.

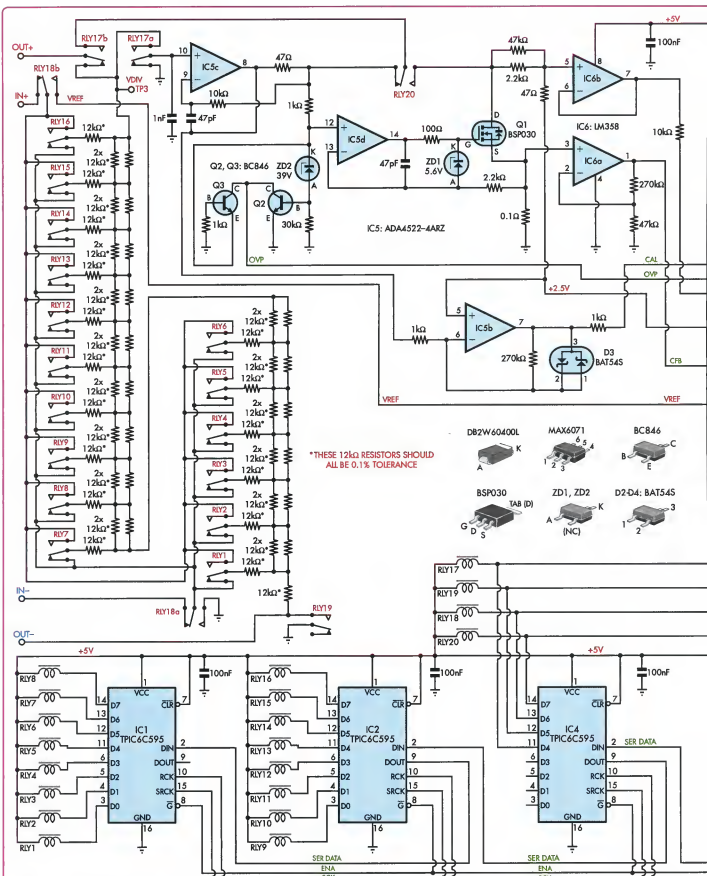
IC5d then controls the gate of Mosfet Q1 to sink enough current so that 25mV appears across the 0.1Ω shunt, ie, 250mA. Thus, the current through the shunt (in A) is equal to the voltage at TP3 (in V) multiplied by 10.

A series/parallel combination of three resistors between the 2.5V reference output and the drain of Q1 provides a minimum current flow. This prevents Q1 from being switched off fully when Q1's gate voltage drops, which could cause overshoot upon recovery.

Similarly, zener diode ZD1 keeps Q1 in linear operation during those times when Q1 can not sink the programmed current from the external voltage source. Once its gate voltage rises above 5.6V or so, Q1 is already switched on fully and ZD1 pulls its inverting input (pin 13) up to prevent any further rise in the output voltage at pin 14. This allows it to reduce Q1's conductance more quickly when current regulation resumes.

The 2.2kΩ/47pF filter in its feedback arrangement compensates for the phase shift due to Q1's gate capacitance and turn-on/turn-off time. Without these, the output at pin 14 would oscillate rather than reach a steady level to sink the required current. Essentially, the 47pF capacitor forms an AC feedback path between the pin 14 output and pin 13 inverting input, reducing gain to unity at high frequencies while leaving DC feedback high for precise current control.

Note that the 0.1Ω shunt resistor tolerance of ±1% means that the current reference will initially be much less precise than the voltage reference. But if the shunt's resistance can be accurately measured, this can be programmed into the unit and the er-



PROGRAMMABLE PRECISION VOLTAGE & CURRENT REFERENCE

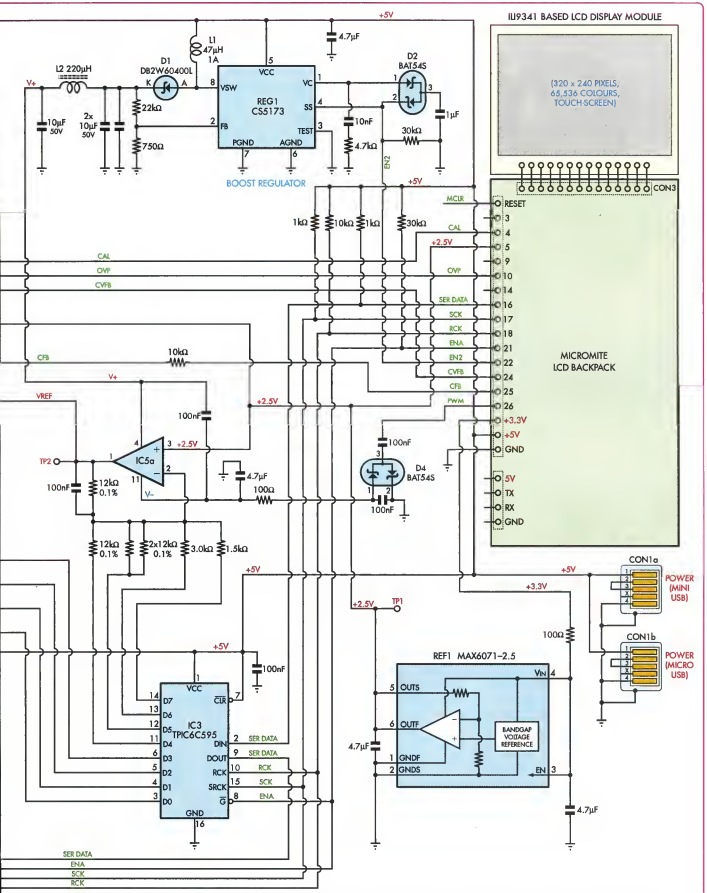
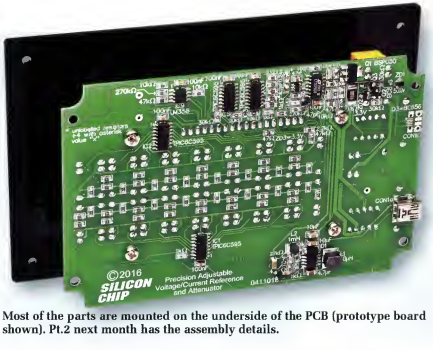


Fig.2: this is the complete circuit of the Programmable Reference, with the LCD BackPack and its associated PIC32 microcontroller shown in the upper-right corner. The precision attenuator (shown at left) is formed from 16 SPDT relays and 47 x 12kΩ ±0.1% resistors, with the control logic below. The switchmode boost converter, for reference voltages above 2.5V, is built around controller REG1 while the voltage reference is in the lower-right corner and the PGA above and to its left.



Most of the parts are mounted on the underside of the PCB (prototype board shown). Pt.2 next month has the assembly details.

ror calibrated out. More on how to do this later.

Note that while the circuit can only sink current, because the whole device is effectively floating (assuming the 5V supply is not earthed), it can just as easily be used as a current source, by connecting the OUT+ terminal to a positive voltage and then drawing current from the OUT- terminal. The circuit won't "know" the difference.

Boost regulator

Before configuring the PGA to give a V_{REF} of 5V or higher, the PIC32 in the Micromite LCD BackPack brings pin 12 of CON2 high. This is normally held low by a 30kΩ pull-down resistor. When high, REG1 is activated. At first, nothing happens since its internal current source at pin 1 must charge a 1µF capacitor via Schottky diode D2. But once the voltage at that pin rises sufficiently, it will begin to periodically sink current from pin 8, with a frequency of around 560kHz and a duty cycle that starts very low and steadily increases.

Each time REG1 brings pin 8 low, L1's magnetic field charges up. When it ceases sinking current from this pin, the voltage at pin 8 shoots up above the 5V supply, due to the magnetic field of L1 discharging. 2A, 60V Schottky diode D1 is forward-biased and the two parallel 10µF capacitors are charged up to a voltage which increases as the switching duty cycle builds.

Eventually, the voltage across these capacitors reaches 39V. The 22kΩ/750Ω divider across these capacitors results in a voltage of 1.276V at the feedback pin (pin 2) of REG1 for an output of 39V and when this is reached, REG1 dials back the duty cycle to keep the output voltage steady. The 10nF capacitor and series 4.7kΩ resistor provide frequency compensation, to avoid oscillation in this voltage.

The 39V supply is filtered by 220µH inductor L2 and another 10µF capacitor, to remove as much of the switching residual as possible. Note that L2 has a DC resistance of around 17Ω so it's effectively an RLC filter, ie, you can consider L2 as an ideal 220µH inductor with a 17Ω resistor in series. This 39V supply powers quad op amp IC5 only.

Relay control

In addition to the 16 relays which are used in the R-2R divider ladder, four relays switch between the various modes; RLY17 and RLY18 are DPDT types while RLY19 and RLY20 are the same SPDT types as used in the divider. All have 5V DC coils.

All 20 relay coils are driven directly from the 5V input supply rail and switched by one of three 8-way open drain serial-to-parallel latches (IC1, IC2 & IC4). These are similar to the 74HC595 but have open-drain outputs rated to 33V/100mA with diode clamps to allow direct switching of inductive loads.

Another identical IC, IC3, is used to switch the ground ends of the four PGA gain resistors. Note that while the coils of RLY17-20 are connected to outputs of both IC3 and IC4, only those outputs on IC4 are programmed to pull low by the software; the extra connections are simply for PCB routing convenience.

While we're only using 24 of the 32 available outputs, we need four ICs rather than three. That's because if the same IC was used to switch relay coils and the PGA gain resistors, the ground shift caused by the much larger relay coil currents would affect PGA gain accuracy.

IC1-IC4 are daisy-chained with a single 3-wire SPI serial bus. Serial data is fed to pin 2 (D_{IN}) of IC3 and is shifted out eight clock cycles later at pin 9 (D_{OUT}). This signal is fed to IC4's D_{IN} and thence on to IC2 and IC1 in a similar manner. Pin 15 of each IC is the data clock (SCK) and these are driven in parallel. Once 32 bits have been shifted through all four ICs, the parallel-connected RCK inputs (pin 10) are pulsed high, transferring that data to the output latches.

The fourth control line, G-bar (pin 8) is also connected in parallel between the four ICs and this is pulled high initially by a 30kΩ resistor from the 5V supply, disabling all 32 outputs by default. It isn't until data is loaded into the output latches that the micro pulls this line low, enabling the ICs.

Since IC1-IC4 run off 5V and their inputs are not compatible with 3.3V logic levels, as used by the PIC32 micro, all four of these lines are driven by 5V-tolerant open drain outputs on the micro and each line has a pull-up resistor from the 5V supply. The lines driving the D_{IN} and SCK inputs have a 1kΩ pull-up resistor as these need to be switched at a much higher frequency than the other control lines (ie, each toggled up to 32 times when the relay and PGA states are to be updated, compared to once).

Protection circuitry

Several protection features prevent damage in case the device's outputs are back-driven by excessive voltages or currents, especially in current reference mode. If this happens, the outputs are disconnected by RLY17.

The maximum continuous current for Q1 is 5A, as in this case, the 0.1Ω 3W shunt dissipating $5A^2 \times 0.1\Omega$ = 2.5W. But the dissipation in Q1 itself depends on both the current and its drain voltage. While it can handle more than 2.5W for short periods, in the long term, it can overheat.

The software keeps track of the drain voltage by monitoring the output of IC6b, which buffers a voltage derived

from Q1's collector. The divider resistors at its pin 5 non-inverting input have an effective ratio of around 45 times and bias the result by 2.5V, allowing it to sense voltages from well below 0V up to about 36V.

This is important since if the drain is pulled below ground, Q1's parasitic diode could conduct a lot of current, quickly overheating it. So if its drain goes below -0.5V or above its +30V rating, it's immediately disconnected.

The micro also monitors the current through Q1 via op amp IC6a which amplifies the shunt voltage by a factor of 6.75, giving 675mV/A, allowing measurement of up to 5A. Again, should this limit be exceeded, the output will immediately be disconnected.

While operating as a current reference, the micro subtracts the implied shunt voltage (ie, 0.1Ω times the measured current) from the drain voltage and then multiplies this by the current to obtain the instantaneous dissipation. This is then integrated over time, with a thermal model allowing for heat to be radiated and conducted away from Q1.

The micro therefore continuously estimates Q1's junction temperature and can disconnect the output should it approach a dangerous level (>125°C). This allows relatively high dissipation to be maintained in Q1, for higher reference currents, as long as they are only brief tests. The user can safely connect the test load and allow the unit to disconnect before Q1 overheats. The estimated junction temperature is displayed on the TFT display while using the current reference mode.

Additional protection features operate when the buffered output is enabled. If OUT+ is pulled above 39.5V, zener diode ZD2 conducts and switches on NPN transistor Q2, pulling pin 10 on the Micromite low. It then switches off RLY17 to protect IC5. Similarly, if OUT+ is driven negative, Q3 switches on and also pulls pin 10 low.

Self-calibration support

The 2.5V reference's initial accuracy is good and it does not require calibration. However, should you have the equipment to accurately measure its output, the software will allow you to enter the exact measured reference voltage for improved precision.

But the PGA gain is not necessarily as accurate as REF1; it should be within ±0.25% with a V_{REF} of 5V, 7.5V or 10V due to the use of 0.1% resistors but this is already worse than REF1's tolerance. At higher gains, the gain error could exceed 1%.

Fortunately, this can be automatically corrected by the software. It measures the actual PGA gain on each range the first time the unit is powered up and this can be repeated at any time, via the touchscreen user interface.

It works as follows. First, the PGA is set up for a gain of two, ie, V_{REF} = 5V. Then, relays RLY17, RLY18 & RLY19 are energised and the precision divider is set for a ratio as close to 2:1 as possible. In theory, this should result in a voltage very close to 2.5V at the output of IC5c, since the PGA's gain of two and the attenuator's gain of one-half should cancel out.

The difference in the output of IC5c and the output of REF1 is amplified by a factor of -271 by precision op amp IC5b and fed to pin 3 of CON2, which is connected to one of the Micromite's analog inputs. Pin 4 of CON2 is connected to the 2.5V reference rail. The micro measures the voltages at pins 3 and 4 and compares them.

If the PGA's gain is actually greater than two then the output of IC5c will be more than 2.5V and so the output of IC5b will be below 2.5V (it's an inverting stage). The gain factor of 271 means that even though the micro's ADC only has 10-bit precision, the micro can accurately measure the error. It can then adjust the precision divider's ratio and re-measure, repeating this until the output of IC5c is as close to 2.5V as possible.

Then, by using the attenuation setting and difference between the voltages at pins 3 and 4, the micro can calculate the exact voltage at V_{REF} when the PGA is set for a nominal gain of two. The software will then use this value to determine the correct divider ratio to get an accurate reference voltage between 2.5V and 5V.

This process is repeated for the other PGA gain settings, for example, PGA gain is set to three times (V_{REF} = 7.5V) and the attenuator is set to one-third; PGA gain is set to four times (V_{REF} = 10V) and the attenuator is set to one-fourth, and so on.

Note that this process takes a few seconds because the micro needs to wait for the output of the PGA to settle each time before performing measurements. The 100nF capacitor across its feedback resistor, required for stability and low noise operation, does take a little time to charge (~one second).

Once all the PGA gain measurements are made, the results are stored in flash memory for future use. They can be overwritten later if necessary. Similarly, if the user provides a more accurate measurement of REF1's output, this too is stored in flash.

Current mode calibration

The easiest way to calibrate the current sink is to use an accurate 4-wire resistance meter to measure the shunt's actual resistance and program this into the unit via the touchscreen. This is then stored in flash memory and used to compensate the control voltage.

The shunts included with our short-form kits will be supplied with a resistance reading made in this manner, using an accurate bench meter.

In theory, you could calibrate the unit by measuring the actual current sunk/sourced and adjusting the shunt value until it matches the set value. However, the average DMM only has a DC current measurement accuracy of ±1%, so that's a non-starter.

A more practical approach would be to purchase a 0.1% resistor of around 1kΩ. You would then check and possibly adjust your DMM's accuracy measuring 10V, using this unit. Next, set the unit to current mode and program it to sink 10mA, then apply 12V to OUT+ via the 1kΩ precision resistor. You can then adjust the unit's shunt value setting until you measure exactly 10V across this resistor (10mA x 1kΩ = 10V).

Coming next month

Next month, we'll describe how to assemble the PCB, attach the Micromite LCD BackPack, program it and mount it inside a box. We'll also show screen grabs and explain how to use it. SC

Changing The R/2R Resistor Ladder Value

As mentioned in the text, the 12kΩ resistor value used in the divider ladder is not critical. If all the 12kΩ resistors are changed to another, similar value (eg, 10kΩ), you only need to change two additional components: the 3kΩ and 1kΩ resistors in the PGA. These should be as close as possible to 1/4 and 1/12 the ladder resistor value. For example, for 10kΩ ladder resistors, use 2.4kΩ and 820Ω respectively.