Highly efficient design uses switchmode technique

50V/5A laboratory power supply: Pt.1

This is the first of two articles describing a new and very efficient variable power supply using the switchmode principle. The new power supply can deliver voltages anywhere in the range from three to 50 volts DC and at voltage settings of 35V or less, it can deliver currents up to five amps. It is easily the most powerful DC supply we have ever described, with a maximum power output of 175 watts!

by JEFF SKEEN

Not only is this new power supply the most powerful we have ever produced, it is also the most efficient, and for its rating, the most compact. In fact, if we had not had the benefits of the switchmode principle, the supply would be a great deal more bulky and expensive. At the lower voltage settings the supply would have had to dissipate powers in excess of 150 watts. To do that, you need very large heatsinks which would probably have to be fan-cooled.

Most computers these days use switchmode power supplies as these are a practical and efficient method of providing a highly regulated supply with high current output.

This month's article will be devoted to the principles of switchmode power supplies while next month's will contain the full constructional details of the new supply.

Basic principles

To gain an understanding of the operating principles involved in a switchmode power supply we will start our circuit explanation with the simplified diagram shown in Fig. 1.

In this circuit transistor Q1 is an ideal switch with "on" and "off" (or open and closed) times controlled by a pulse width modulator (PWM) circuit attached to the base. By ideal we mean that Q1 has no voltage drop between emitter and collector when conducting.

When Q1 is on (base voltage is low) current I1 is drawn from Vcc, passes through Q1 and L1 and supplies both the load, RL, and charges the output capacitor, CO. The voltage at the cathode of the diode, D1, is the same as Vcc so the diode is reverse biased and non-conducting.

While Q1 is on, energy from the current I1 passing through L1 is stored in the magnetic field developed by the coil. When the signal on the base of Q1 goes high, Q1 turns off and ceases to pass current. The energy stored in the magnetic field must now be dissipated and this energy is delivered to the circuit as current, I2, which is driven by the voltage induced across L1 by the collapsing field.

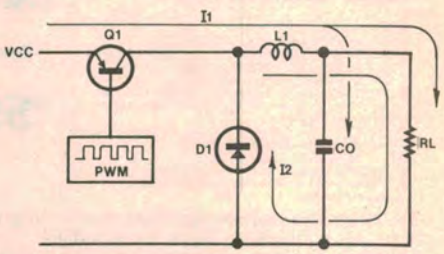
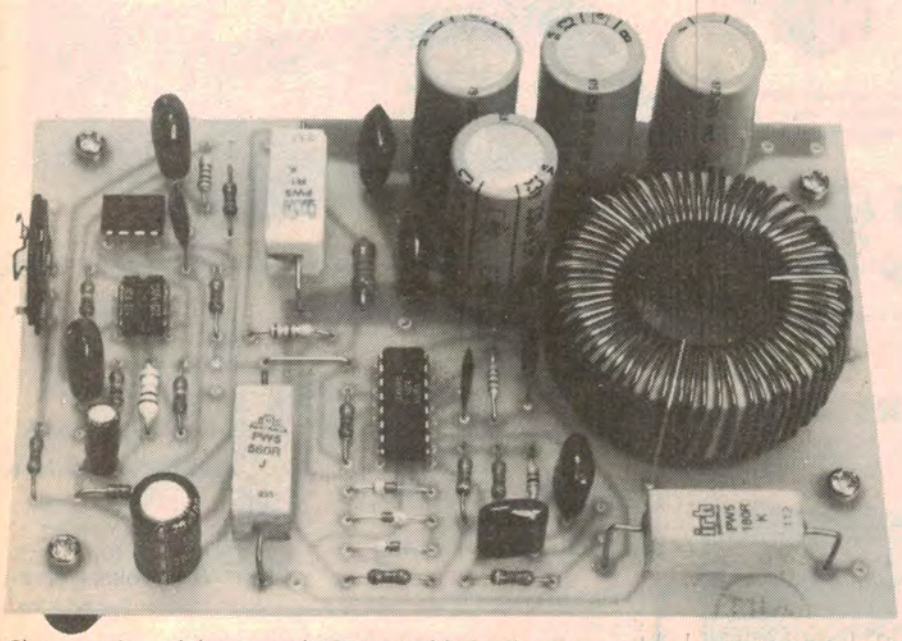


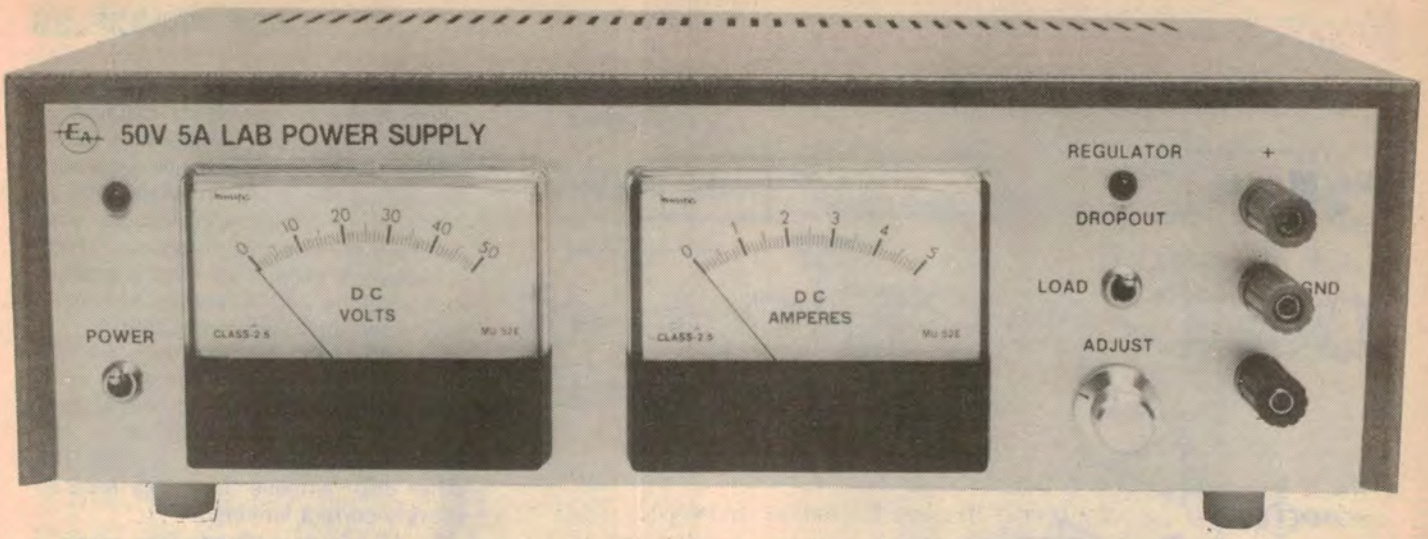
Fig. 1

The induced current I2 flows from the coil, through the load, through D1 (which is now forward-biased) and back to the coil. In addition, CO begins to discharge, also supplying current to the load.

When the PWM signal at the base of Q1 goes low again, Q1 will turn on and pass current (I1) once more. D1 will again be reverse-biased and non-conducting, and current from Q1 will pass through L1, recharging CO and powering the load. This current will also rebuild the magnetic field around L1, preparing it for the next Q1 off-cycle.

The inductor L1 together with the capacitor CO forms a filter which


Close-up view of the control PCB assembly for the new power supply. Note that the final version differs slightly from this early prototype.



Our new switchmode supply has adjustable voltage output from 3 to 50V and a maximum 5A output at voltages below 35V.

averages out the waveform from the collector of Q1 to give a DC voltage across RL. The magnitude of this voltage is given by the equation,

$$V_{out} = Vcc \times t_{on}/T$$

where t_{on} is the period when Q1 is conducting and T is the total period of the waveform applied to the base of Q1.

For an ideal power supply, this output voltage is independent of the output current. This is another way of saying that the power supply has zero output impedance.

From the above formula we can see that any factors which would tend to cause changes in the output voltage can be compensated for by adjusting the on-time (or duty cycle) of Q1. To do this we need a control circuit which can modulate the pulse width of the signal applied to the base of Q1 while monitoring the output voltage for any changes. This is then referred to as "pulse width modulation".

The reason for the high efficiency of the switchmode regulator is that the pass transistor, which is the principal source of losses, is operated at its two most efficient points. At cutoff, there is a large voltage across the transistor but little current through it. Conversely, at saturation there is little voltage across the transistor but a large current through it.

Either way, very little power is dissipated in the switching transistor so efficiency is high. And heatsinks can either be small or, in some cases, dispensed with entirely.

Basic PWM circuit

Now refer to Fig. 2 which illustrates the basic components of a PWM circuit and how they function together. There is an RC oscillator which produces a sawtooth output, an error amplifier which monitors the output voltage and a comparator which actually produces the square wave pulse train which is fed to the base of switching transistor Q.

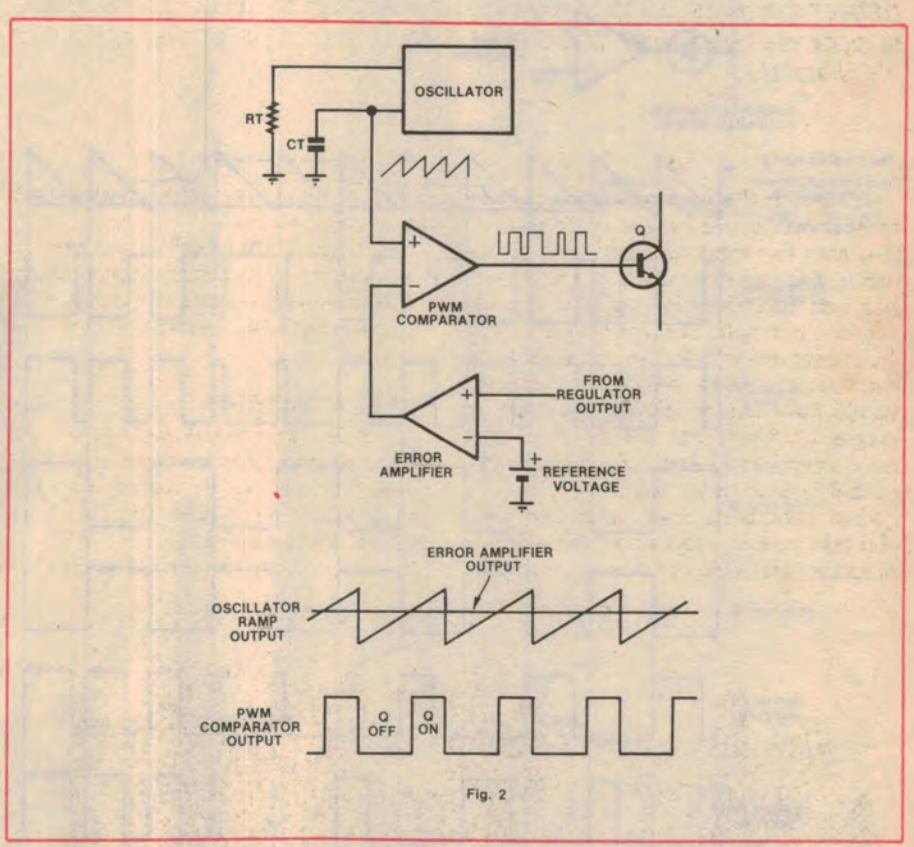


Fig. 2

OK. Now the RC oscillator produces a sawtooth waveform with its period defined by RT and CT. Not that surprising really, is it? In our power supply, the operating frequency is just beyond the limit of audibility, at around 20kHz. But the actual frequency is not important.

The error amplifier performs the same function as the error amplifier in any linear regulator circuit. It compares a proportion of the power supply output voltage against a very stable reference voltage. The output of the error amplifier is then essentially a constant voltage on which is superimposed an amplified version of the small fluctuations in the power supply output. In other words, as far as we are concerned, the output of the error amplifier is essentially a constant DC voltage.

This voltage from the error amplifier is compared to the sawtooth voltage from the oscillator by the PWM comparator. When the sawtooth voltage is the higher, the PWM comparator will have a high output and Q will be turned on. When the error amplifier voltage is the higher the PWM comparator output is low and Q is turned off.

By looking at the timing diagram which is part of Fig. 2, this operation can be fur-

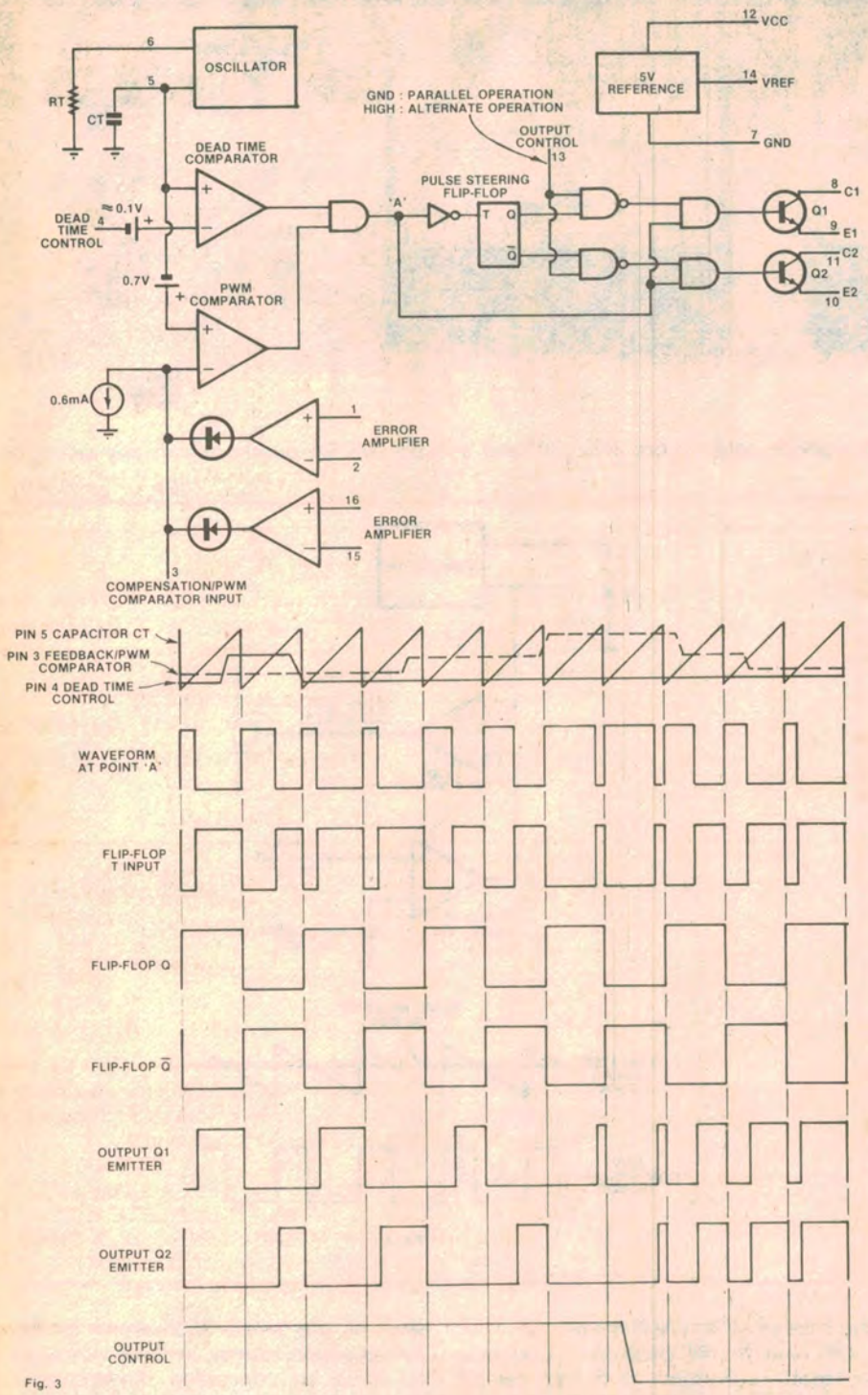


Fig. 3

ther elucidated. Note that if the error amplifier output was higher than shown in the timing diagram, the intersection times of the two waveforms would be shorter and hence the pulses from the comparator output would be correspondingly shorter (although still having the same repetition rate, ie, 20kHz).

By the same process, if the error amplifier output was lower, the intersection times of the two waveforms would be longer and the comparator's output pulses would also be longer.

Well, that essentially describes how a pulse-width modulation circuit works. Such a circuit could employ a number of discrete semiconductors at the simplest level, or in the most refined versions use a specially designed IC. Such an IC is the Fairchild μA494 switchmode regulator which is the heart of our new power supply.

Fig. 3 is a full block and timing diagram for the internal circuit of the μA494. It differs from the simplified diagram in several ways. Firstly, components for an extra mode of operation have been added so that the μA494 may be used in push-pull or bridge type circuits with transformer coupled outputs. These components include an extra transistor, logic circuitry and an extra comparator (called the dead time comparator).

Secondly, instead of one there are two error amplifiers provided. One error amplifier is used for output voltage control in the same manner as in the simplified diagram of Fig. 2 while the other error amplifier is usually used to provide current limiting.

To do this the voltage drop across a small resistor in series with the load is measured. If the voltage drop exceeds a preset value (indicating excessive current) then the output of the error amplifier rises and reduces the output transistor on time so that the output current is kept to a safe level.

Logic circuitry

The logic circuitry is arranged so that the mode of operation of the output transistors can be selected by the appropriate voltage level applied to the output control, pin 13. A high level on the output control and the output transistors turn on and off alternately in sympathy with the flipflop outputs. A low level (or ground) applied to the output control causes both output transistors to operate in parallel and ignore the flipflop outputs.

With the output control grounded, the state of the output transistors at any time is dependent upon the output state of the dead time and PWM comparators. Both comparators high and the output transistors are on, either or both comparators low and the output transistors are off.

The inputs to the comparators differ from the simplified diagram in that there are DC offset voltages applied. To gain an understanding of the operation of the comparators assume firstly that the dead time control (pin 4) is connected to ground. The 0.1V offset which is now applied to the inverting (–) terminal of the dead time comparator means that for the comparator output to go high, the voltage (ramp) across CT must be greater than 0.1V.

Since CT is discharged below this voltage at the beginning of each ramp, there will always be a short interval at the beginning of each cycle when the output of the comparator is low and hence the output transistors are off. This is called "dead time" and is required to preclude the possibility of both output transistors being on together when con-

nected in the push-pull mode.

Due to storage effects in the bases of the switching transistors, it will take a short while for them to respond to the controlling signal applied to their bases and turn off. If sufficient time is not allowed between their on cycles, the transistors may form a short circuit across the power supply with potentially disastrous results.

The PWM comparator is designed to compare the ramp voltage across CT plus a 0.7V offset, against the voltage present on pin 3, the compensation/ PWM comparator input. Most of the time the voltage present at pin 3 will be held low by the 0.6mA current sink and so the non-inverting input will have the higher voltage on it. This will cause the PWM comparator to have a high output most of the time.

If either error amplifier detects an error then the voltage at the inverting (–) input of the PWM comparator will rise since the error amplifiers can supply enough current to swamp the 0.6mA current sink. The PWM comparator output will remain low, and hence the output transistors will remain off, until the voltage at the non-inverting (+) input of the PWM comparator rises above the voltage at the inverting input.

This is shown by the dotted voltage level in the first line of the timing diagram.

The outputs of the error amplifiers are connected to pin 3 via diodes which form an OR gate and isolate one error amplifier output from the other. In this way error amplifier outputs may swing high or low independently of each other.

If required, the voltage of pin 3 may be raised with an offset to reduce the duty cycle of the output pulses in the same manner as the 0.1V offset on the dead time control. This feature may be used to provide a "soft start" facility on a power supply to minimise current transients upon turn on.

The last section of circuit to be covered is the 5V voltage reference. This generally forms the reference against which the power supply output voltage is compared. It can also be used as a supply voltage for external circuits and will provide up to 20mA of current in this mode.

Next month we shall present the full constructional details of the new power supply together with performance specifications.

Fairchild μA494: basic data

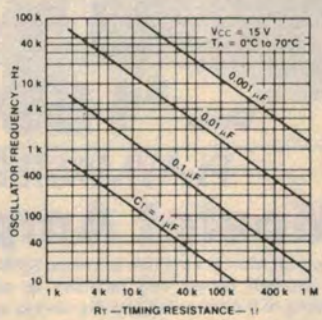


Fig. 4: oscillator frequency vs timing resistance.

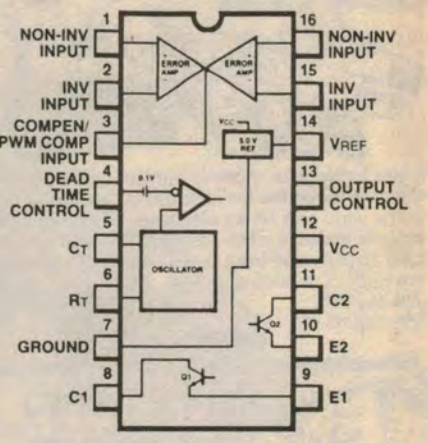
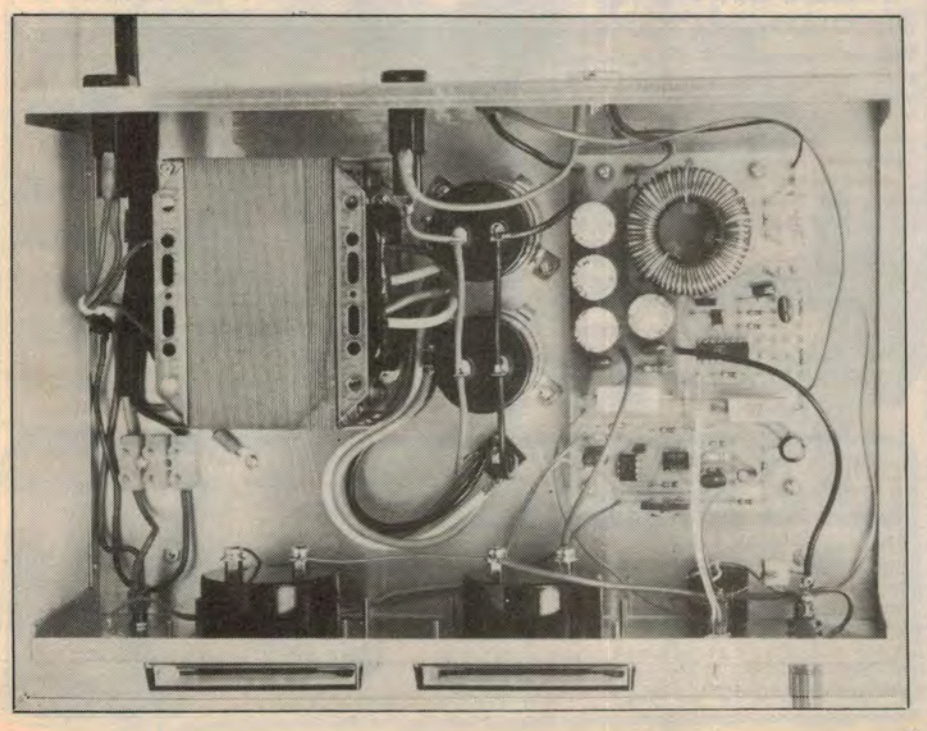


Fig. 5: connection diagram for the μA494 PWM control circuit.

NOTE: Figs. 4 & 5 and the accompanying table reproduced from the Fairchild linear data book, courtesy Fairchild Australia.

Recommended Operating Conditions

Symbol	Characteristic	μA494C Min	μA494C Max	Unit
V_{CC}	Power Supply Voltage	7.0	40	V
V_{IN}	Voltage on Any Pin Except Pins 8 and 11 (Referenced to Ground)	−0.3	V_{CC} +0.3	V
V_{C1}, V_{C2}	Output Voltage	−0.3	40	V
I_{C1}, I_{C2}	Output Collector Current		200	mA
C_T	Timing Capacitor	470		pF
			10	μF
R_T	Timing Resistor	1.8	500	kΩ
f_{osc}	Oscillator Frequency	1.0	300	kHz
T_A	Operating Ambient Temperature Range	0	+70	°C



◀ *LEFT: here is a sneak preview inside the prototype. Full constructional details will be published next month.*