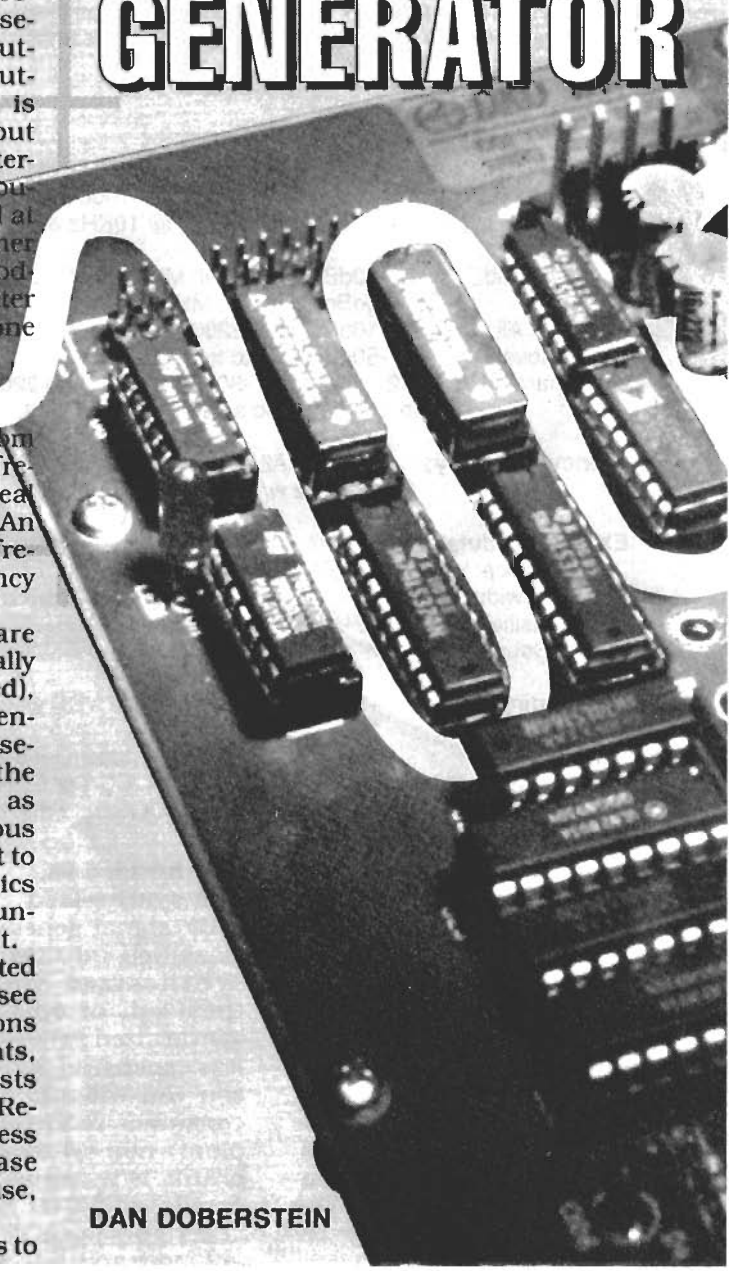
A look at the design of a 2-GHz RF signal generator.

PC-BASED RF SIGNAL GENERATOR



DAN DOBERSTEIN

RF (RADIO FREQUENCY) SIGNAL GENERATORS ARE essential equipment for radio-frequency design. The TG2000 described in this article is a PC-based synthesized signal generator. It can also function as a tracking generator for DKD Instruments' Models 810B and 1800C/H PC-based spectrum analyzers. The model 810 spectrum analyzer was the subject of an article in **Radio-Electronics**, August and September 1991.

The TG2000 is a IBM-PC compatible card that can be installed in an 8-bit slot on the PC bus. (Alternatively, it can be interfaced to a parallel port, although an external power supply is needed for that.) Software for the TG2000 is a stand-alone package that is available on the *Electronics Now* BBS (516-293-2283, 9600, V.32, V.42bis).

By reviewing the key specifications shown in Table 1, it can be seen that the TG2000 covers the band from 4 to more than 2048 MHz in progressive octave bandwidths. Its output is phase-locked to a 4-MHz crystal reference and its output power ranges from −5 dBm to 0 dBm. Output impedance is nominally 50 ohms and is provided via an F-connector. An optional output connector provides an attenuated output. External FM modulation is supported via an AC-coupled RCA jack input. A sync pulse is provided at another RCA jack for triggering scopes and other equipment. System requirements are very modest for stand-alone operation; a PC/XT or better with CGA or better monitor, 512K RAM, and one floppy drive are all you need.

RF generator basics

Figure 1 shows the RF output spectrum from an "ideal" generator that produces a single frequency or tone with infinite purity. The real world is more complex than Fig. 2 shows. An actual spectrum consists of the fundamental frequency, as well as other undesirable frequency components.

The unwanted frequency components are broken down into three categories: Harmonically related, spurious (or non-harmonically related), and residual modulation close to the fundamental frequency that are due to noise and phase-locked loop (PLL) processes. Harmonics pose the least problems, and at times could be desired, as in frequency multiplication or mixing. Spurious response is generally never useful, and it's best to minimize its content and power. Subharmonics or outputs at whole number fractions of the fundamental are almost always undesired output.

To understand the third group of unwanted outputs "zoom in" on the fundamental line (see Fig. 3), where the small residual modulations can be seen. Of all the unwanted components, this one is the toughest to eliminate. It consists of phase noise and residual FM sidebands. Residual FM is generally caused by the PLL process and cannot be completely eliminated. Phase noise is caused by random fluctuations or noise, and it cannot be completely eliminated.

One way to visualize residual modulations is to

TABLE 1
MODEL TG2000 SPECS

Frequency coverage: 4 to 2100 MHz, Single Output, F/SMA Connector.

Power output: 0 dBm to –10dBm
w/Option P-01 ; +7 dBm to –10dBm,
Total power Flatness; ±2 dB over the band 10 to 2000 MHz

Frequency step sizes:

Step	Band
250.00000 Khz	1024 to 2048 MHz
125.00000 KHZ	512 to 1024 MHz
62.50000 KHz	256 to 512 MHz
31.25000 KHz	128 to 256 MHz
15.62500 KHz	64 to 128 MHz
7.81250 KHz	32 to 64 MHz
3.90625 KHz	16 to 32 MHZ
1.95312 KHz	8 to 16 MHz
0.97656 KHz	4 to 8 MHz

With option DDS-01 step sizes are reduced by:
Max step size (@ top of band); Take above step sizes divide by 238
Min step size (@ bot of band); Take above step sizes divide by 476

VSWR of Output (50 ohm): < 1.3 all bands.

Frequency Output Spec's:
Primary Oscillator Phase locked to Crystal or DDS reference.
Reference Sidebands; > -50 dBc typ. @ 1000 MHz
Phase Noise; > -70 dBc/Hz @ 10KHz offset @ 1000 MHz
Harmonics;
2nd; > -10dBc 68 to 2200 MHz
> -5dBc 5 to 68 MHz
All others > -10dBc 5 to 2200 MHz
Spuruous; > -50dBc TYP to to 2200 MHz
Subharmonics, LO/2; > -20dBc, -30dBc typ. 1100 to 2200 MHz
5 to 1100 MHz no subharmonic content.

Frequency Accuracy; +/- 30Khz All bands @ room temp.
+/- 200Hz w/ Optional TCXO reference.

EXT. FM Modulation Input:
Impedance; >10K ohm
Bandwidth; >5KHz
Max Sensitivity; 1v/100MHz
Coupling; AC

(Optional) Ext. AM Pulse Modulation:
Impedance; TTL
Bandwidth; 5KHz
ON/OFF Ratio; >30db
Copuling; TTL Levels

Power Requirements: +5 VDC @ 0.5 amps, +12 VDC @ 0.2 amps, -12VDC @ 0.1 amps
Interfaces: PC Bus or Parallel Interface (Centronics).
System Requirements: 360K Disk Drive, VGA, EGA or CGA graphics adapter, 512k Ram, DOS 3.0 orhigher.

imagine a perfect FM radio receiver. If the output of a perfect RF generator were fed into the perfect radio, nothing would be heard from the speaker. If a signal containing phase noise and residual FM were fed into our perfect radio receiver, the phase noise would be heard as a hiss, and the PLL sidebands would be heard as a single tone (assuming that the sidebands were audio frequencies within the human ear's frequency response range).

Synthesized vs. non-synthesized

RF signal generators can be classified into two categories: synthesized and non-synthesized, or open-loop. Non-synthesized generators tend be less expensive, and for that reason you will still find them in consumer receivers. An example of a non-synthesized RF generator is a voltage-controlled oscillator (VCO). Synthesized generators such as the TG2000 are more accurate and frequency-stable than non-synthesized generators.

A VCO can be converted into a synthesizer with the addition of a PLL. This turns the open-loop VCO into a closed-loop control system in which frequency can be controlled with much greater precision. There is a price for this accuracy though: VCOs essentially have infinite frequency resolution and fast settling

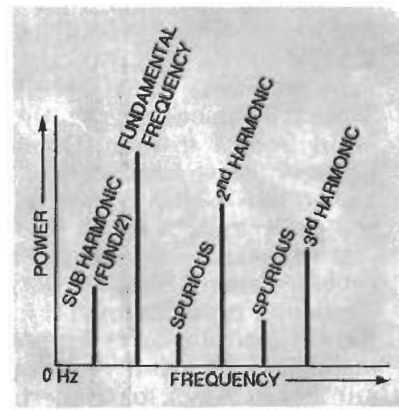


FIG. 1—IDEAL RF OUTPUT SPECTRUM from an ideal generator. The ideal generator produces a single frequency or tone with infinite purity.

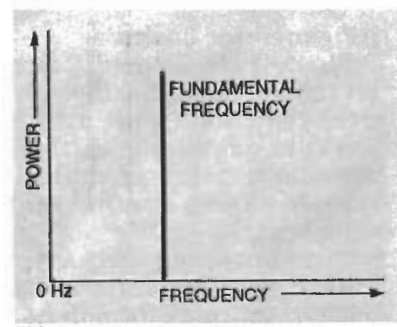


FIG. 2—THE PRACTICAL GENERATOR is considerably more complex than an ideal one. The actual spectrum consists of the fundamental frequency that we want, and other frequency components which we don't want.

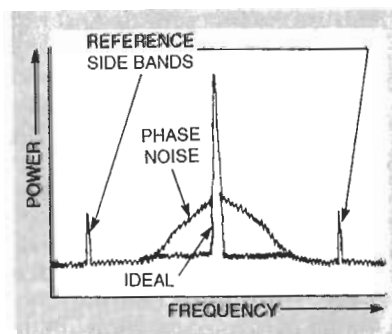


FIG. 3—TO SEE THE THIRD GROUP of unwanted outputs you can "zoom in" on the fundamental line.

times. Once a PLL is coupled to the VCO, the oscillator has fixed-frequency steps and, in general, slower settling time. A benefit to PLL control of a VCO is that the phase noise declines dramatically over that of the open-loop VCO.

The PLL

The minimum number of components for a common PLL-based synthesizer are a VCO, a phase/frequency detector, a loop filter, and a crystal reference (see Fig. 4). The PLL divides the crystal reference down to form the reference frequency, typically on the order of 10 to 500 kilohertz (kHz). The output of the VCO is also divided down and then compared with the reference frequency at the phase/frequency detector. This generates an error voltage that, when filtered and fed to the VCO, forces the VCO frequency to be an exact multiple of the reference frequency. The filter for the error voltage is called the loop filter. The time constants of this filter and other characteristics will greatly effect PLL performance. Phase noise, reference sideband levels, and settling time will all be influenced by the loop filter.

As already mentioned, the reference frequency is found in the RF output as sidebands that are symmetrical about the fundamental. This is the approach used in the TG2000.

Another common element found in RF PLL synthesizers is the prescaler, which reduces the frequency of a VCO to one that can be handled by the programmable dividers. Prescalers come in many divide ratios, and some have multiple divide ratios. Dual-modulus prescalers are a special class of prescalers. These dividers have two divide ratios, typically N and N + 1. The active divide ratio depends on a separate control input. Dual-modulus prescalers allow finer step sizes for a given divide ratio than fixed prescalers.

A trade off

Ideally, a synthesizer has infinitely small step sizes and no phase noise. Unfortunately as step size is reduced, phase noise increases. There are some exceptions to this rule but, in general, to obtain the cleanest possible output in terms of phase noise, larger step sizes or equivalently larger reference frequencies are needed. As a rule of thumb, every time the reference frequency is reduced by a factor of 2, the phase noise increases by 6 dB. A technique that's just starting to be widely used, called fractional synthesis or arithmetically locked loops, offers some relief in the phase noise/step size trade off.

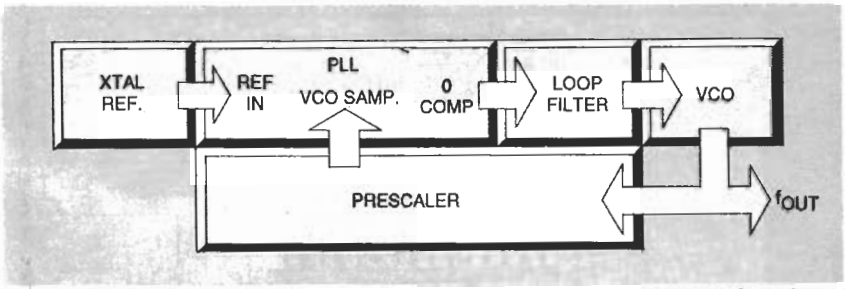


FIG. 4—THE COMPONENTS for common PLL-based synthesizer are a VCO, a phase/frequency detector, a loop filter, and a crystal reference.

The 125-kHz reference frequency is the highest that can be accepted by the TG2000 while providing its complete frequency range. This limitation on frequency range is caused by the dual modulus characteristic of the MB1501 prescaler.

Multiple octaves

A typical VCO can span, at best, a frequency range roughly double that of the VCO's lowest operating frequency. This is called its octave bandwidth. For example, a VCO with a 0- to 28-volt control voltage range that outputs 1 GHz with zero volts at its control point will output 2 GHz with 28 volts of control voltage. It becomes obvious that to cover 4 to 2048 MHz with one VCO is not practical. To overcome this limitation, many strategies are used in RF generators. They usually involve mixing a VCO octave band down or up.

The TG2000 uses a progressive-division technique. A 1024- to 2048-MHz VCO is phase locked, and then a series of divide-by-2 prescaler ICs creates the frequencies between 4 and 1024 MHz in progressively smaller octave bandwidths. To cover the 4- to 8-MHz band, for example, the 1024- to 2048-MHz VCO output is divided by 256, or 2^8. One advantage of progressive division is that phase noise improves with each increase in divide ratio. The power of two relation also applies to the minimum step size available in each octave band.

Each divide-by-2 divides this minimum step size in half. A disadvantage of this method is the relatively high harmonic content caused by the dividers and higher frequency bleed-through due to limitations in high frequency RF isolation.

Another disadvantage of the progressive-division technique is a relatively large step size. The TG2000 uses a reference frequency of 125 kHz, which the divide-by-2 prescaler translates as a 250-kHz step for the 1024- to 2048-MHz bands. Provision has been made in the design of the TG2000 for the addition of an optional direct digital synthesis (DDS) reference. The DDS reference, which can replace the fixed crystal reference, has the ability to select frequency with approximately 2-hertz (Hz) resolution. This would permit much finer steps for the combined system with virtually no loss in phase-noise performance.

The MB1501 PLL

The Fujitsu MB1501 PLL IC is the heart of the TG2000 generator. The block diagram of the 1501 is shown in Fig. 5. The MB1501 incorporates a built in serial interface for loading the programmable reference divider, two counter registers (A and N), a high-speed, dual-modulus divider (64/65 or 128/129), and two phase/frequency detectors.

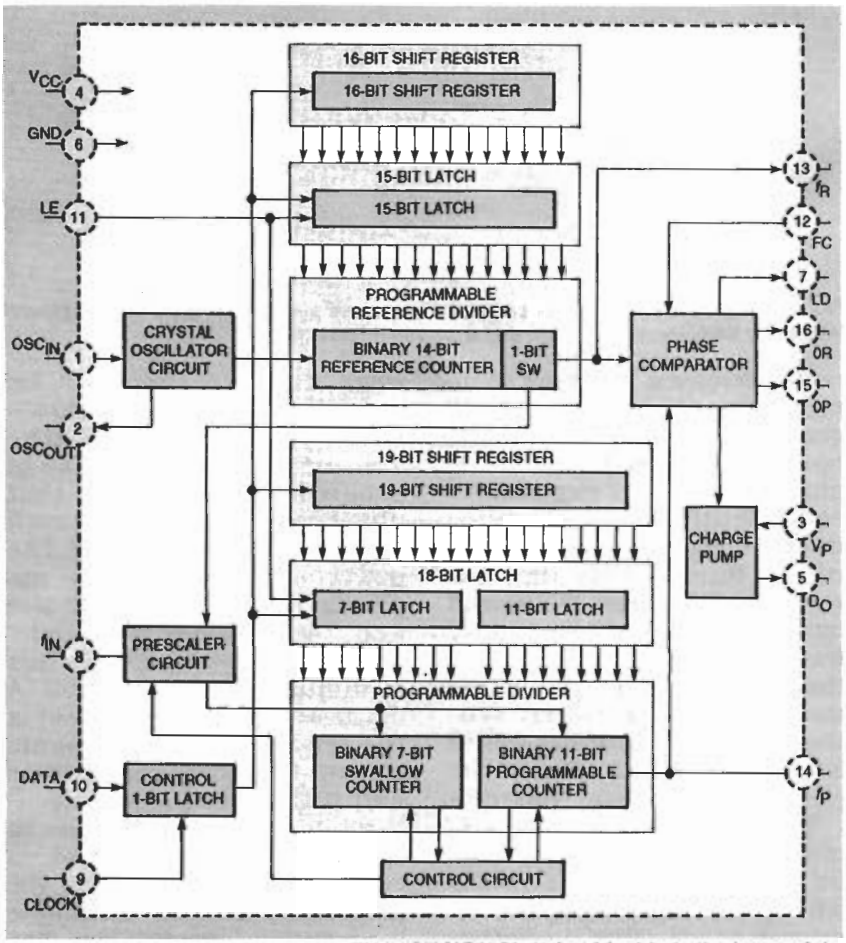


FIG. 5—BLOCK DIAGRAM OF THE FUJITSU MB1501. This PLL chip is the heart of the TG2000 generator.

The output frequency of the VCO is determined by the integers loaded into the R, A and N registers by the following formula:

$$f_{VCO} = [(P^N)+A]^2[f_{OSC}/R]$$

where P = 64 or 128

The TG2000 uses the dual-modulus prescaler in the divide by 64/65 mode, or P=64. The VCO can oscillate only at frequencies that are integer multiples of the reference frequency, f_{OSC}. The factor of two accounts for the fixed divide-by-2 operation (done by an NEC584 prescaler) that the VCO output carries out before it reaches the VCO input which has a maximum frequency of 1100 MHz (refer to Fig. 4).

The MB1501's internal dual-modulus prescaler is needed to reduce the input frequency of the VCO to the point where the N and A counters can operate. This dual-modulus ability overcomes the effect of a fixed-modulus prescaler—step-size multiplication. For example, for a fixed-modulus prescaler of 64, the minimum step sizes would be multiplied by 64. That would translate to a 16-MHz step size in the 1024 to 2048 MHz band for the TG2000. The N/A counter in combination with the dual-modulus divider avoids this problem with the limitation that N must always be greater than or equal to A.

The restriction that N be greater than or equal to A has some not-so-obvious ramifications, such as placing limits on frequency range versus reference frequency, as discussed earlier. Essentially, for a given reference frequency (f_{OSC}/R), the generator is limited to a minimum frequency that can be synthesized while still providing full coverage at minimum step size. For P=64, R=32, and f_{OSC} =4 MHz, the minimum frequency is 512 MHz. Since the generator has a fixed divide-by-2 prescaler, that results in 1024 MHz at the VCO. Below that frequency, not all integer multiples of the reference frequency are possible due to the N>=A restriction. In other words, you could not sweep the VCO frequency from 900 to 1024 MHz at step sizes of 250 kHz.

While all this might seem confusing, a general rule is that if you want a large step size for improved phase noise, *and* your PLL uses a dual-modulus approach, the dual-modulus divide ratio should be as small as possible.

All fixed divide ratios, step sizes, and prescalers are a power or multiple of two. Other numbers could be used, but when it is time to compute A, N, and band switching points for a given output frequency, the power/multiple-of-two relationships pay off.

Two phase/frequency detectors are included with the MB1501 PLL. The bipolar on-chip charge pump permits a minimum number external components for the loop filter. The differential phase-comparator outputs require an external charge pump, usually an op-amp. In the TG2000, an external LM358A op-amp (IC1-a) boosts the bipolar charge pump voltage from 0 to 5 volts to −0.5 to 28 volts. In addition, the op-amp and its associated feedback network acts as an active loop filter. Polarity of the phase-detector output can be inverted by the PLL's FC input. This input is required to compensate for op-amp inversions or VCOs with a negative voltage-versus-frequency slope.

The digital interface to the MB1501 is serial—a block diagram of it is shown in Fig. 6. Three lines are used; CLOCK, DATA, and LOAD ENABLE. Data is clocked in serially, and after an appropriate number of bits (determined by what you are loading) a LOAD ENABLE is sent. A 15-bit word serves as the reference divider, and a 19-bit word holds both the A- and the N-count values. The C source code for the routines that send the N-, A-, and R-register values to the

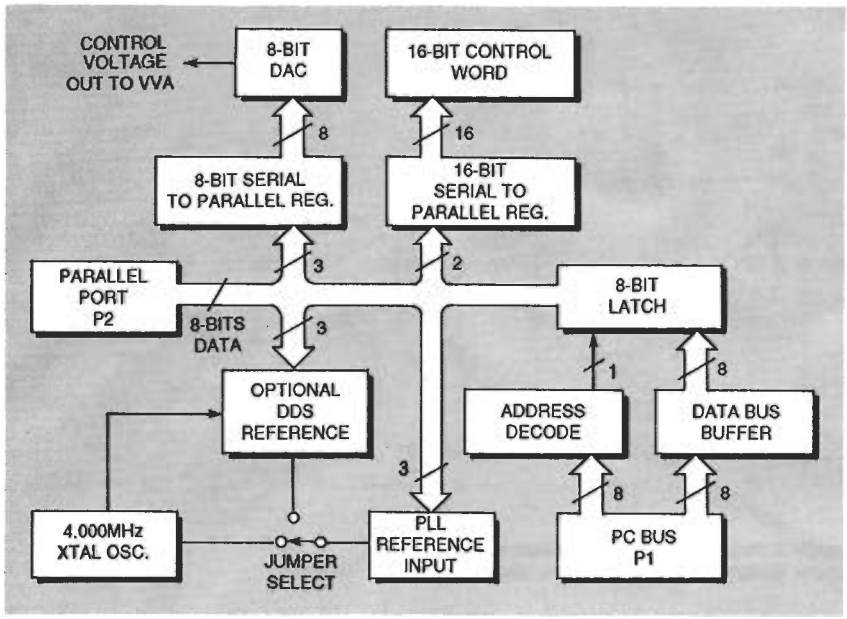


FIG. 6—MB1501 DIGITAL INTERFACE block diagram.

MB1501 are provided on the *Electronics Now BBS* as part of a file called TG2000.ZIP.

Overall operation

As already discussed, the synthesis technique used in the TG2000 is successive division. Every band except the one from 1024–2048 is the output of a divide-by-2 divider. The computer determines the band being used and turns on the appropriate dividers and a single output amplifier path is activated; the other amplifiers are turned off. Five paths cover the 4–2048 MHz band. The band from 256 to 2048 is covered in three paths, with each path covering one octave. The band from 4 to 256 MHz is covered with two paths, each covering 3 octaves. A total of nine octaves are covered in this fashion from 4 to 2048 MHz. The three octave paths are possible due to the divider used which has selectable 2/4/8 divide ratios available. See the block diagram in Fig. 7.

The summed signal is passed through a voltage-variable attenuator (VVA) pin-diode array (a Seimens BAR60), which can be seen in Fig. 8 as D12. The VVA corrects output power variations and provides variable output power. An 8-bit DAC controls the VVA. The signal then passes through a final amplification stage and out to the RF output connector. The VVA requires a 0- to 10-volt control signal and bias voltage for proper operation. The device has a non-linear attenuation versus control-voltage response. These nonlinearities do not affect attenuation control because the computer uses a look-up table to control it.

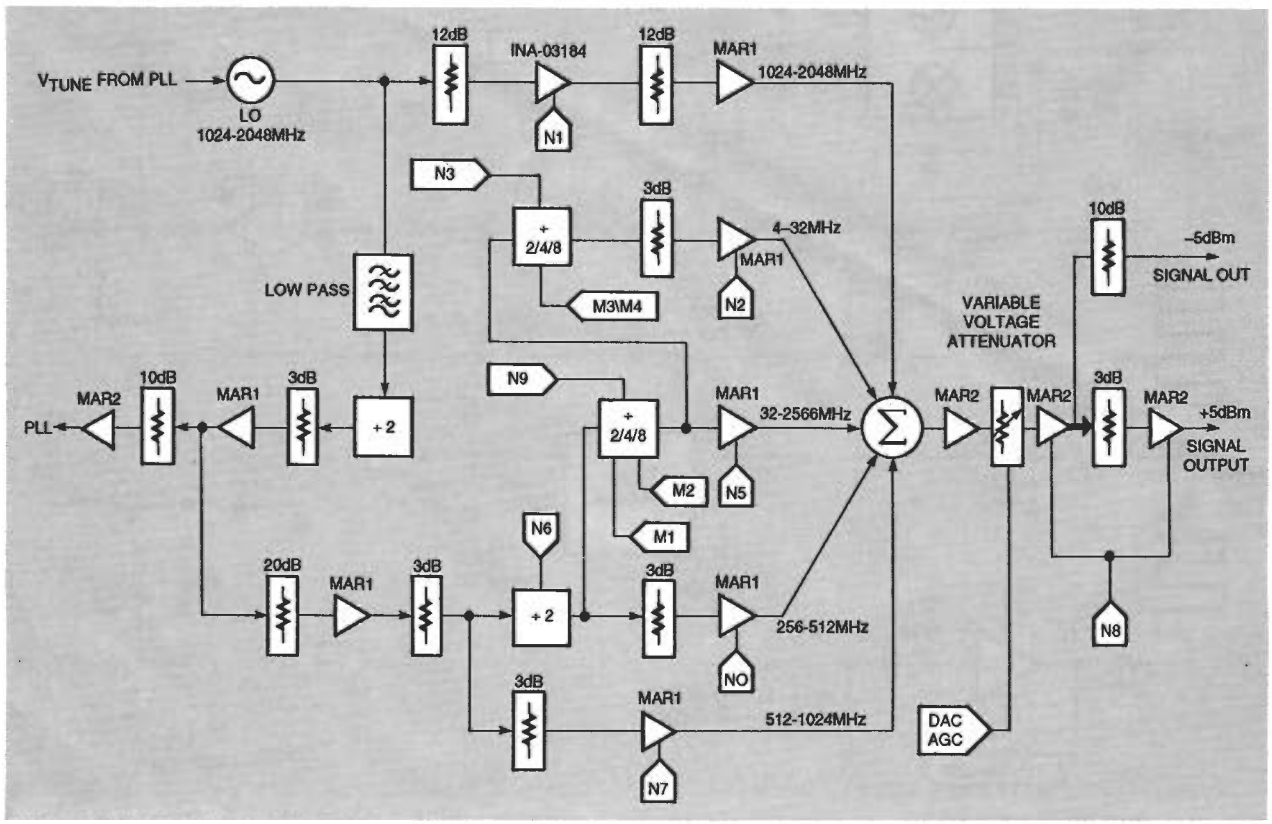


FIG. 7—DIVIDER BLOCK DIAGRAM. The TG2000 uses a successive division technique for synthesis.

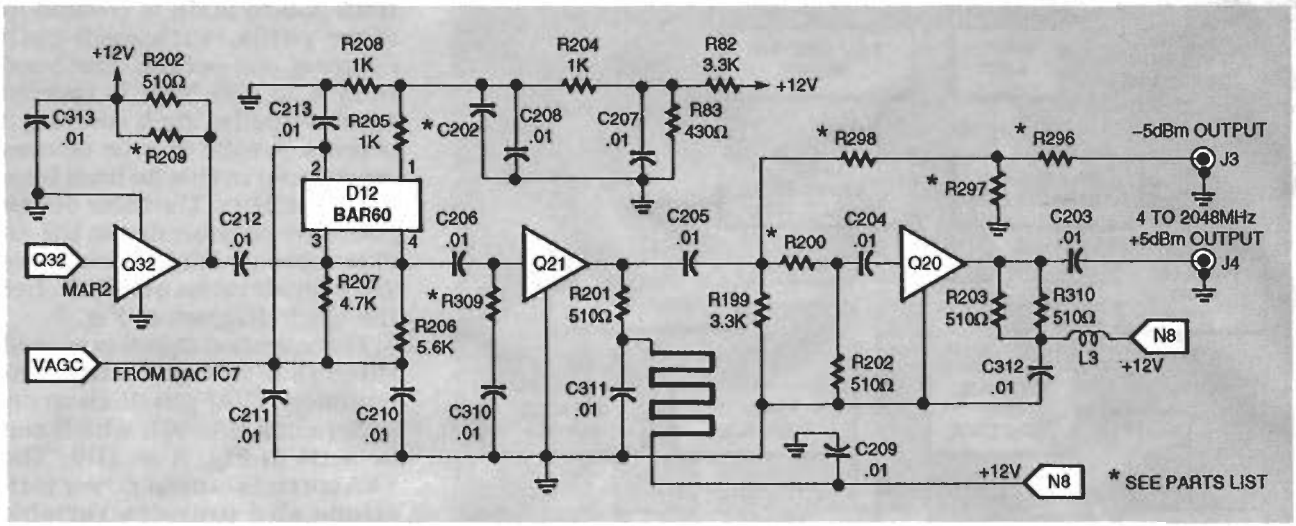


FIG. 8—THE SUMMED SIGNAL is passed through a voltage-variable attenuator pin-diode array (D12), which corrects output power variations and provides variable output power.

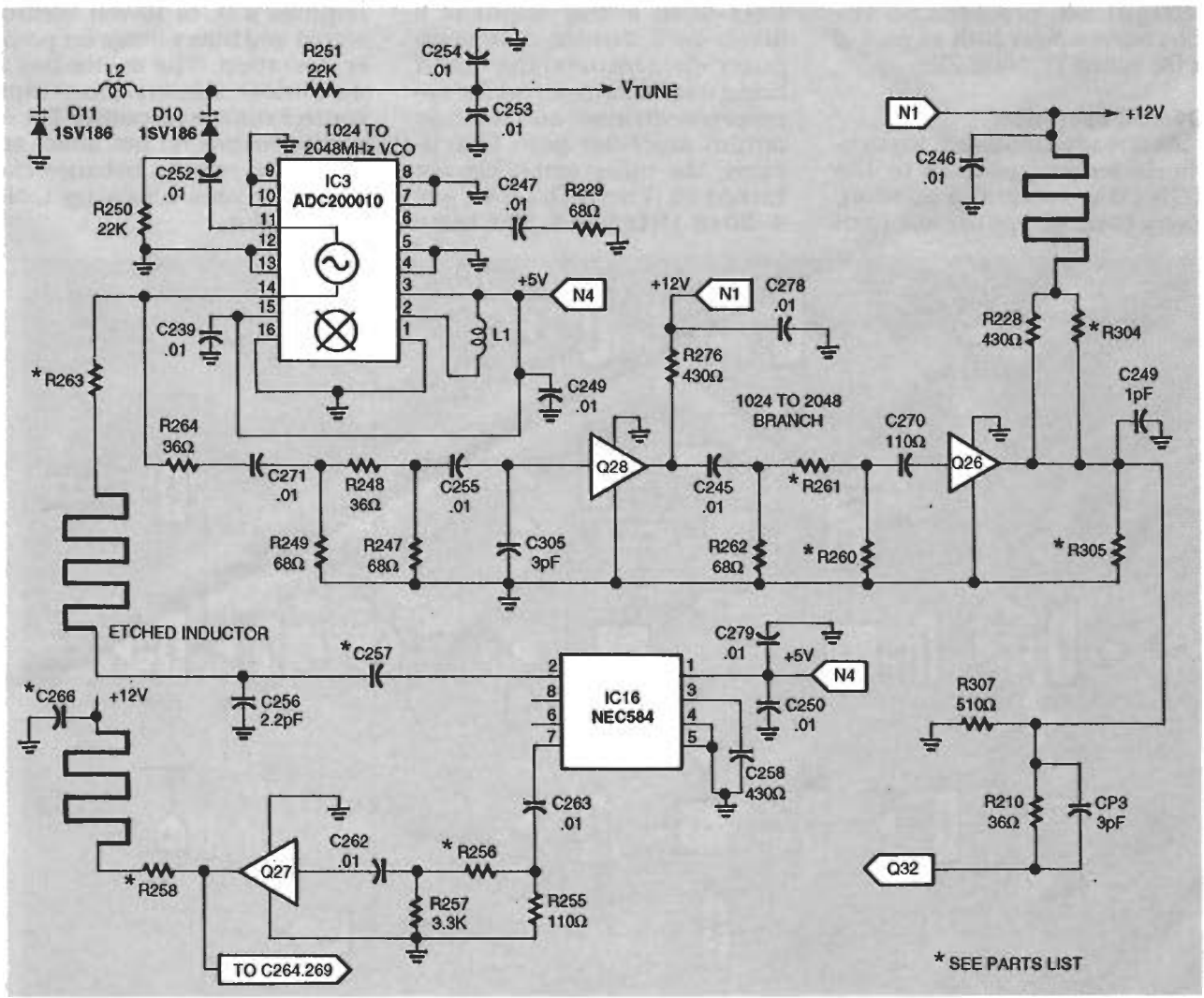


FIG. 9—THE FIRST NEC548G (IC16) acts as a prescaler, reducing the output frequency of the VCO by a factor of 2. It becomes the 512-to-1024 divider when this band amplifier is switched on.

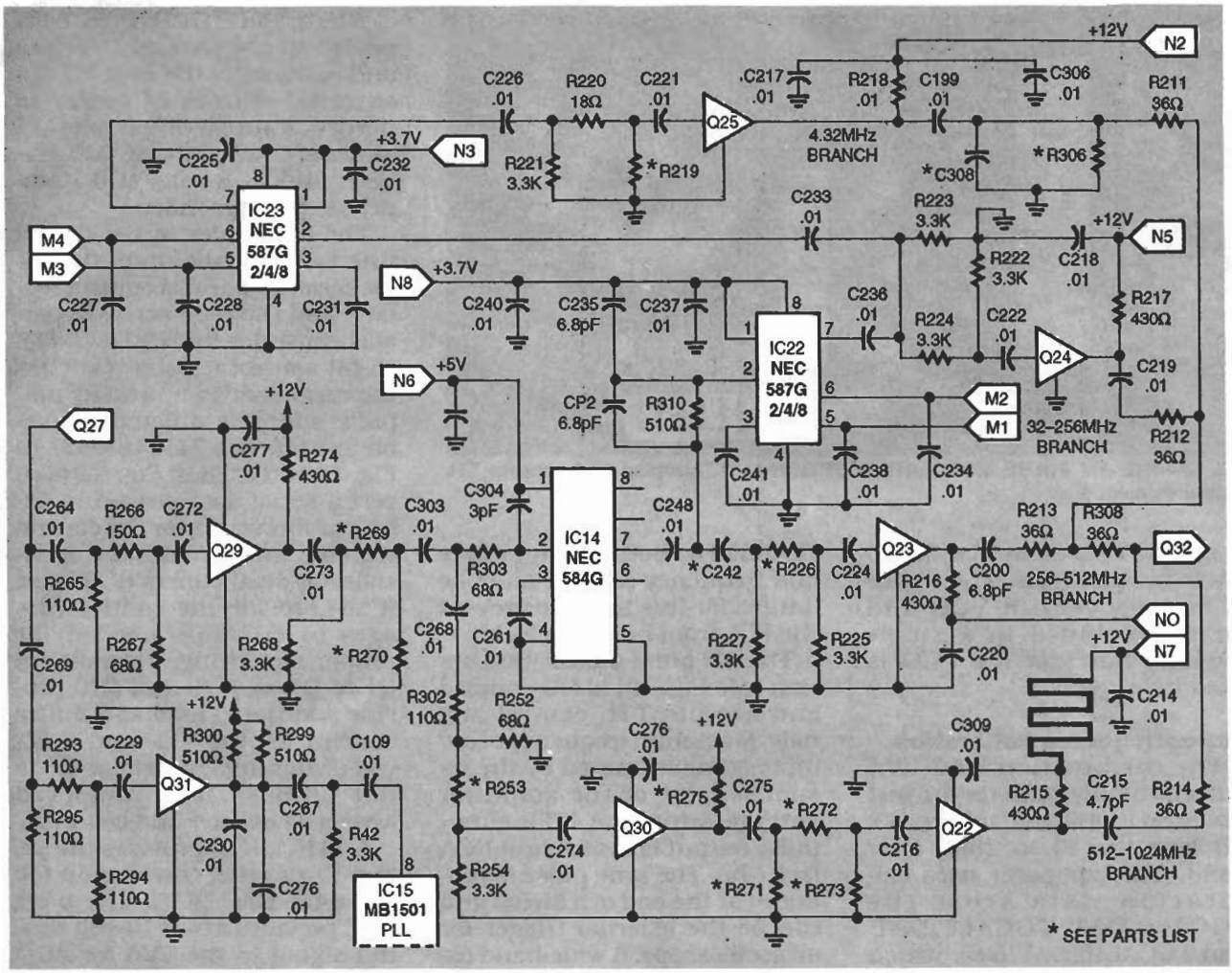


FIG. 10—AFTER THE SIGNAL IS SPLIT, one half is sent to the 512-to-1024 path. Splitting again occurs with half going to the 512 to 1024 amplifier and the other half to the 256 to 512 MHz divider.

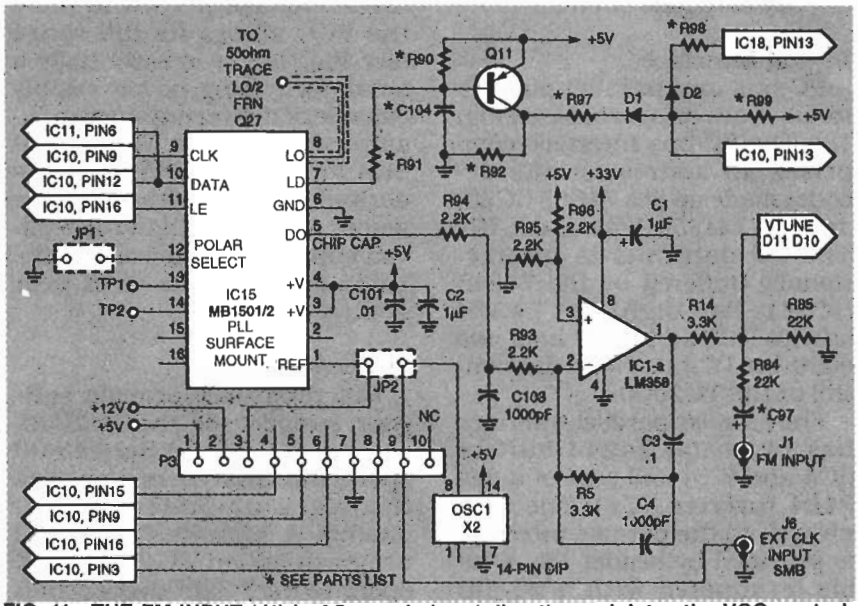


FIG. 11—THE FM INPUT (J1) is AC-coupled and directly modulates the VCO control point.

The dividers

The two divide-by-2 dividers are NEC584Gs, and the two divide-by-2/4/8 dividers are NEC587Gs (see Figs. 9 and 10). The first NEC548G (IC16) acts as a prescaler, reducing the output frequency of the VCO by two. It becomes the 512-to-1024 divider when this band amplifier is switched on. This signal is the split; one half is sent to the PLL and the other half is sent to the 512-to-1024 path. Splitting again occurs with half going to the 512–1024 amplifier and the other half to the 256–512 MHz divider. The output the 256–512 MHz divider is sent to the 256–512 MHz amplifier and the 32–256 MHz 2/4/8 divider. The 4–32 MHz band is handled by the last 2/4/8 divider.

The VCO

Three different voltage-controlled oscillators can be installed in the TG2000. The

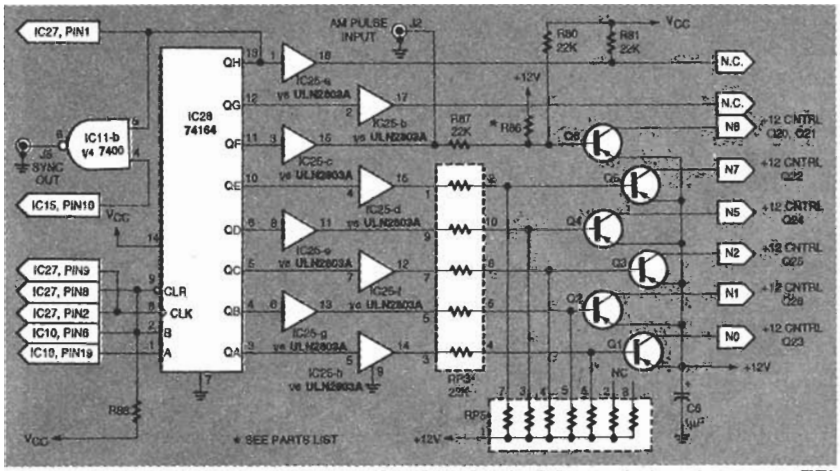


FIG. 12—THE AM PULSE MODULATION OPTION is DC-coupled and accepts TTL control signals.

standard VCO is an ADC20010 made by Anadigics. The device is actually both a VCO and mixer combined in a single module, but just the VCO is used here.

Power/frequency calibration

The combination DAC/VVA automatically adjusts output power so that it's flat within ±2 dB over the 10 to 2000 MHz band. The computer uses calibration data from the TGCAL0.DAT, TGCAL5.DAT, and TGCAL10.DAT files, which are sent to the DAC to linearize power output. Those files represent 0dBm, −5dBm, and −10dBm, respectively.

Readers will not be able to achieve the same calibration accuracy obtained with a factory-assembled product; a slight degradation will be seen because kit builders must depend on generic calibration files.

Frequency accuracy is determined primarily by the 4-MHz crystal TTL oscillator (OSC1 in Fig. 11). The standard oscillator is accurate to ±50 ppm. More accurate frequency references improve the accuracy of the frequency output.

External modulation inputs

FM and optional pulse-AM modulation is obtained with RCA jacks. The AC-coupled FM input (J1 in Fig. 11) modulates the VCO control point. Sensitivity decreases as DC control voltage increases. The maximum sensitivity is about 1V/100MHz. Both the amplitude and frequency content must be limited for this input to prevent the PLL from breaking lock.

The AM pulse modulation option (see Fig. 12) is DC-coupled and accepts TTL control signals. Maximum frequency of on/off toggling is limited by the response time of the amplifier voltage supply. A TTL sync-pulse output is available at RCA jack (J5). The sync pulse is produced at the end of a sweep and can be the external trigger for an oscilloscope. A wide-band oscilloscope (or an RF detector probe and a lower performing scope) can display these frequency response curves.

Digital interface

PC-bus and parallel-port interfaces are supported (see Fig. 13). The PC-bus interface comprises an address/strobe decoder made up of a 74688 (IC20) and two 74138s (IC18 and IC19). The PC data bus is bidirectionally buffered by the 74245 (IC21). Two eight-bit 74374 latches (IC9 and IC10) hold two eight-bit PC-bus bytes for control of the TG2000.

The simpler parallel interface has two octal 74244 buffers (IC4 and IC5) and part of a hex 7404 inverter (IC6). The connection to the parallel interface is provided by header P2. A cable terminated with a 26-pin IDC connector on one end and a DB-25 on the other is all that's needed to complete the interface.

When the TG2000 is connected to the parallel interface and external to the host PC, an external source of power is needed. A supply of +5 volts at 1 ampere, +12 volts at 0.5 ampere, and −12 volts at 0.1 ampere is recommended.

The remainder of the digital interface is made up of the 16-bit serial-to-parallel control register and the 8-bit serial-to-parallel converter for the DAC. The 16-bit control register switches the various dividers and RF amplifiers for the different bands on and off. Two 74164s (IC27 in Fig. 14 and IC28 in Fig. 12) convert a serial data stream to 16-bit parallel words for the control register. Two UNL2803A open-collector octal buffers (IC25 and IC26) provide the control voltages or currents needed for proper switching. Transistors Q1 to Q7 and Q9 and Q10 provide additional level and buffer current for the +5- and +12-volt switching. Transistor Q8 is not used so it is jumpered across its emitter and collector.

A 74164 (IC8) provides the serial-to-parallel conversion for the 8-bit DAC (IC7). The 8-bit DAC provides a 0- to 10-volt control signal to the VVA for AGC purposes, as already discussed.

An MC34063A +12- to 28-volt converter (IC3) provides the higher voltage needed to drive the VCO across its full range (see Fig. 15). It is essentially a small switching power supply capable of delivering a few milliamperes at 28 volts. The −1-volt bias for the LM358A (IC1-a) is derived from a voltage divider across or connected to the −12-volt supply. This bias allows the LM358A to operate at or near ground potential.

Software

Two programs provide software support for the TG2000. Version 4.0 of the Series-800 spectrum analyzers provides the tracking-generator capability. A separate DOS-based program called TG2000.EXE operates the TG2000 as a general-purpose signal generator. Only the TG2000.EXE software will be discussed here. It is

Continued on page 88

continued from page 42

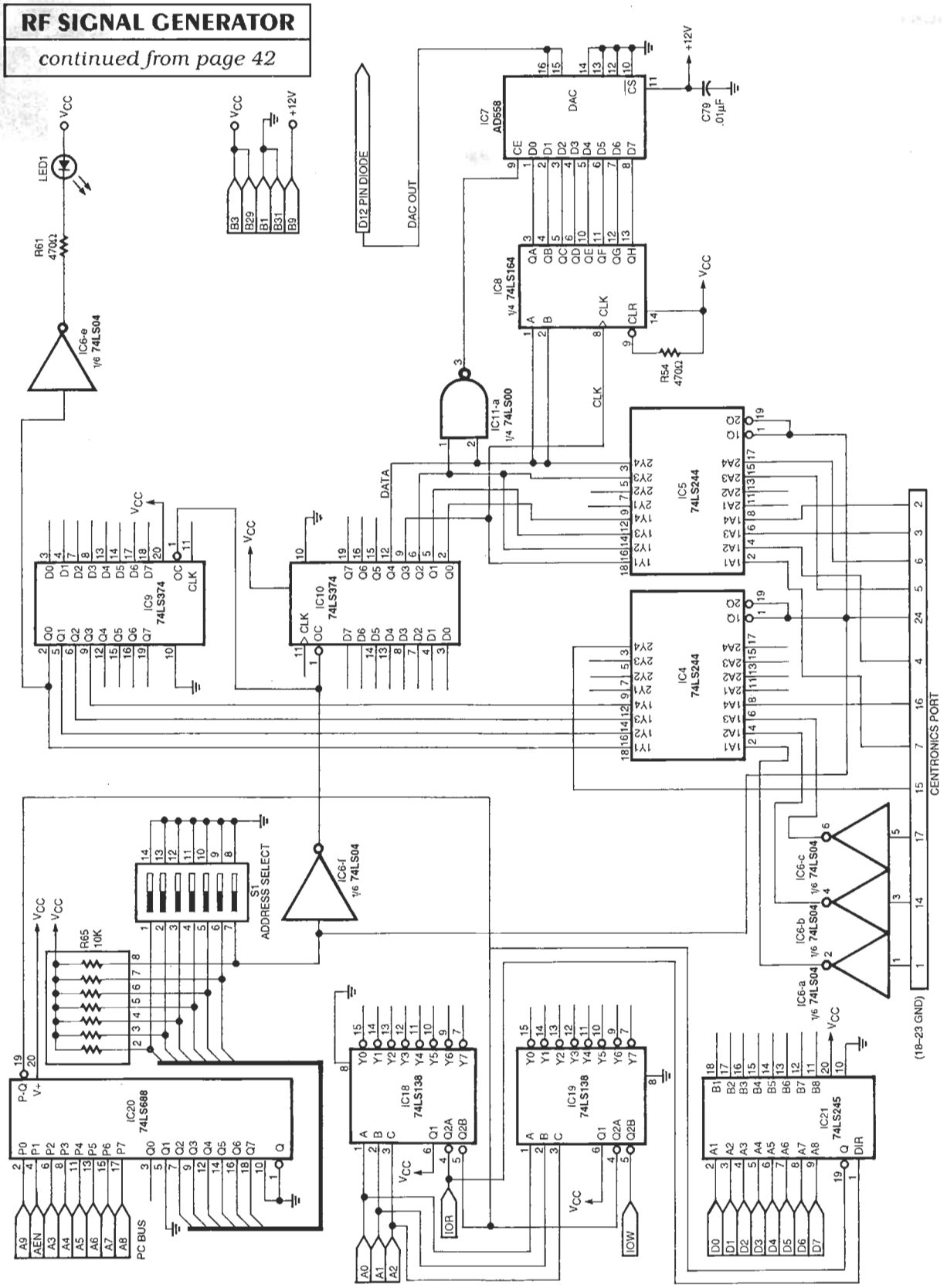


FIG. 13—THE PC-BUS INTERFACE comprises an address/strobe decoder made up of a 74688 (IC20) and two 74138s (IC18 and IC19). The PC data bus is bidirectionally buffered by the 74245 (IC21).

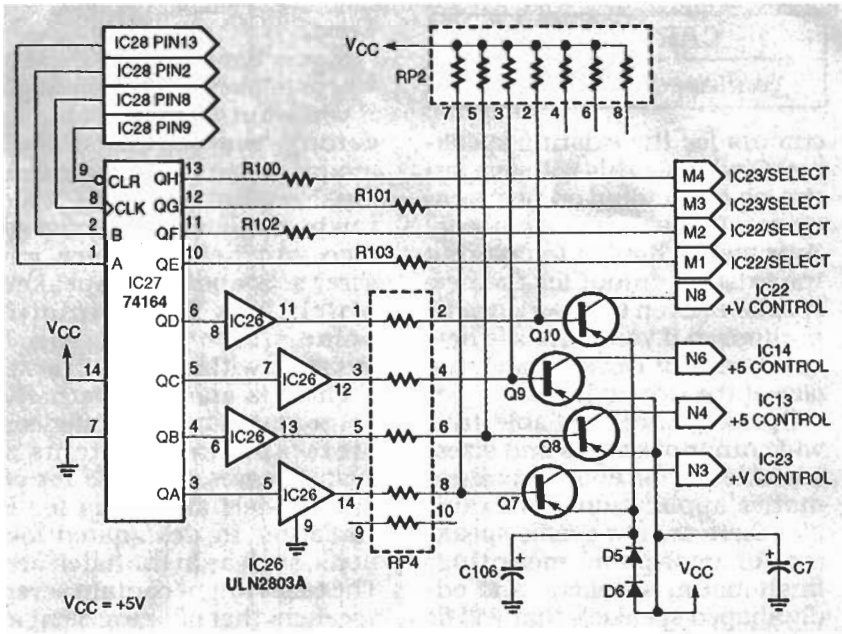


FIG. 14—TWO 74164s (IC27 AND IC28) convert a serial data stream to 16-bit parallel words for the control register.

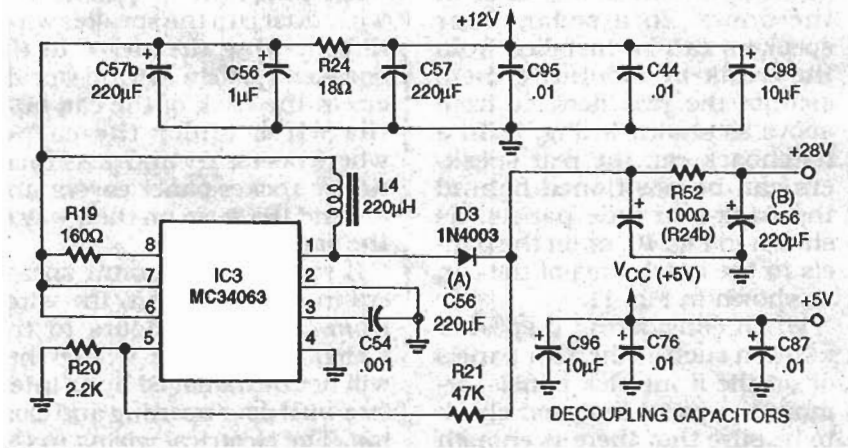


FIG. 15—THE MC34063A +12- TO 28-VOLT CONVERTER provides the higher voltage needed to drive the VCO across its full range.

available on the *Electronics Now BBS*, as part of a ZIP file called TG2000.ZIP.

The TG2000.EXE program contains a menu that allows the user to configure and control the generator. A complete user manual is also contained in the TG2000.ZIP file, so only the highlights will be covered here.

Before using the TG2000 software, you must choose the interface, and possibly the address where the generator will reside on the PC bus. Select the SETUP item from the main menu to configure the software for the chosen address/interface. The setup information is stored in a configuration.

Once the setup operation is complete, you can select either linear or log sweeps and the modulation function. The linear sweep has a constant step size for the entire band of the instrument. The log sweep increases its step size by a factor of two every time it crosses a band boundary. Both sweep functions sweep from a user-defined starting frequency to a user-defined stopping frequency. Sweep rate can be controlled by the DELAY entry.

The other modulation function is a frequency toggle. Two user-defined frequencies are toggled back and forth at a user-defined rate controlled by DELAY. This function can simulate FSK modulation, commonly used for digital data transmission.

Three diagnostic functions are available: Blink, Bitroll, and DAC Ramp. Blink will verify interface operation by toggling all output lines at a 1-Hz rate. Bitroll will debug the 16-bit control register. An alternating pattern of ones and zeros is sent to the 74164s. This results in a square wave at each control bit. DAC Ramp commands the DAC to produce a ramp voltage that will permit any missing codes to be spotted with a scope.

Next month's article will cover the building and and test of the TG2000. Ω

ORDERING INFORMATION

Note: The following items are available from DKD Instruments, 1406 Parkhurst St., Simi Valley, CA 93065. (805) 581-5771:

- **TG2000 kit—$775.00**
- **TG2000 assembled and tested—$1100.00**