IC Tone Burst Generator

Part II: How it works and how to build it

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HAVING DISCUSSED the general theory behind our IC tone burst generator last month, this month we will get down to specifics; namely a working schematic, details of circuit operation, and a parts list. The complete generator with all its options is an extremely flexible instrument. However there are a number of circuit features which can be deleted if you don't need all the performance of the full-blown version. At any rate, here it is in its entirety—you may carry your own version as far as you desire or your electronic larder permits.

Figure 1 is a functional block diagram which illustrates how the unit is laid out, the input/output signals, and the signal flow path. The input signal is first buffered after entering the instrument, then branched into two paths; one via the synchronizer and one via the switch itself. The processed output of the synchronizer gates the switch ON-OFF to establish a tone burst, and an output amplifier buffers this signal to feed the outside world. An internal power supply feeds the various circuits regulated ±12 volts and +5 volts, also unregulated plus and minus potentials of about 20 volts.

The actual circuitry which accomplishes these functions can be segregated into three main areas, the switch and its associated circuits, the synchronizer and its details, and the power supply. Let's look at them now in that order.

The MC1496G Electronic Switch

The heart of the tone burst electronics is the balanced modulator switch, the MC1496G, which we discussed last month. Figure 2 shows how it is used in this application. The details differ slightly from our general model of last month, but the basic idea is still the same.

Beginning at the input of the instrument (JI) the signal is buffered by IC1, an op-amp connected as a unity gain voltage follower. The input impedance of this connection is very high due to the 100% voltage feedback, so the 47K resistor R1 serves as the sole determinant of input impedance. The low impedance buffered signal at IC1's output splits into two paths; the route through the switch itself and the synchronizer path (output AA). For the moment we'll not regard the synchronizer signal and follow the signal flow through the switch.

The signal from IC1 is applied to IC2 by two paths. REa or channel A drives IC2-Q5's emitter on pin 3. Likewise REb or channel B drives IC2-Q6's

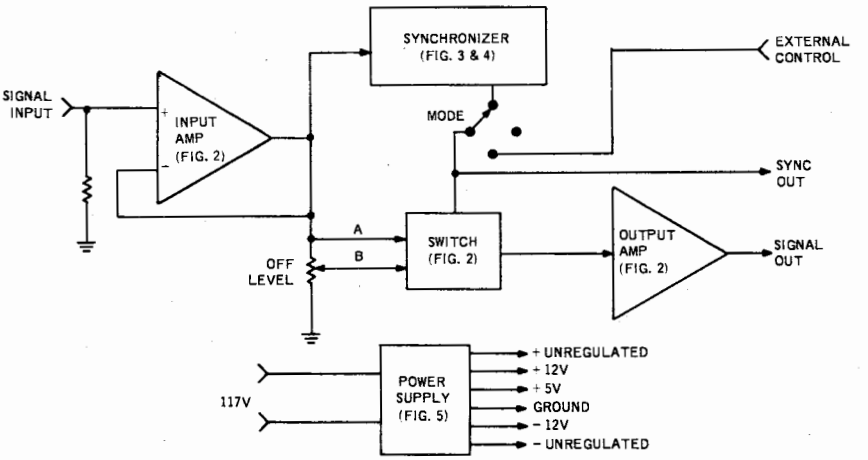

Fig. 1—Block diagram of IC tone burst generator.

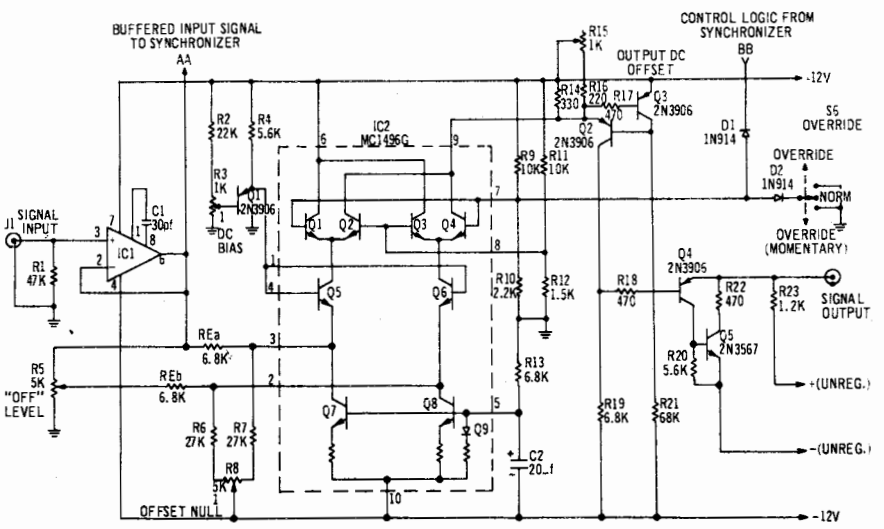

Fig. 2—Schematic diagram of input amp., switch, and output amp.

emitter via pin 2, with the channel B level variable by adjustment of OFF level pot R5. The two switching channels of IC2 operate with IC2-Q5 and Q6 in the common base mode. The connection minimizes crosstalk and maximizes both dynamic range and linearity.

To enable the audio signals to be d.c. coupled through IC2 it is necessary to offset the Vbe of IC2 Q5 and Q6. To accomplish this, a positive d.c. bias is used on their bases (pins 1 and 4) from Q1. This level is variable from R3 and is trimmed so the emitters of IC2-Q5 and Q6 rest at zero volts d.c., thus facilitating d.c. coupling through REa and REb. In addition Q1 provides a very low source impedance, eliminating the common base connection as a possible source of crosstalk.

To eliminate any possible mismatch between the d.c. currents of channels A and B, a differential current balance network is used in the IC2-Q5 and Q6 emitters. This consists of R6, R7 and trimmer R8. R8 is set up initially to adjust the current offset to zero and needs no further adjustments.

The switching of the IC2-Q5 and Q6 collector currents is just as discussed last month. A fixed d.c. bias is applied on pin 8 from R11-R12 and the pin 7 potential switched to control the state of the switch. In the quiescent state the d.c. bias from R9-R10 holds pin 7 slightly higher than pin 8, which in turn connects the output at pin 9 to source B. When a LOW control logic signal from the synchronizer is applied through D1, pin 7 is pulled low with respect to pin 8; this transfers the switch output to source A. Since in this application only a single output from pin 9 is desired, the opposite side of the switch (pin 6) is a.c. grounded by tying it directly to the +12 V. line.

The signal output from pin 9 does not drive a load resistor directly, but is applied to level shift converter Q2-Q3. This stage translates the high d.c. baseline of pin 9 back down to a zero volt average potential at the top of R19. So we can now have a signal d.c. coupled all the way through the instrument, be switched, and then appear at the output with no d.c. offset, and also no interaction between control signal and output due to RC time constants.

A complementary output buffer, Q4 and Q5, buffers the relatively high impedance of R19 and enables the generator to drive ± 5 volts into 500 ohms at the output jack J4. Current limiting is provided by R23 (positive swing) and R22 (negative swing). Since this output stage is a local d.c. feedback loop in itself (and thus immune to ripple and supply variations), it