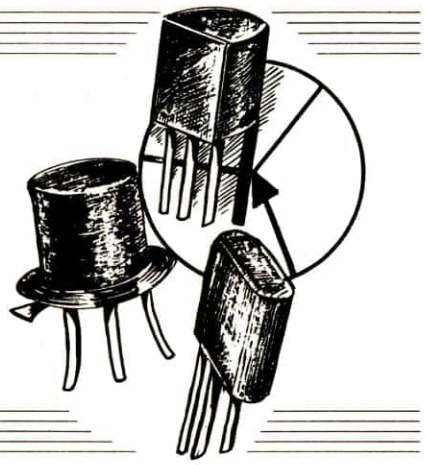
Constructional Project

TRANSISTOR CHECKER



STEVE KNIGHT

Check out your collection of "suspect" and unmarked transistors, including f.e.t.s, with this tester.

TRANSISTORS, both of the bipolar and field-effect varieties, particularly when they have been used over and over again in experimental set-ups, (and schools and colleges are in the forefront of such situations) are apt to find themselves in circuit systems where the operating conditions are not always to their liking. Reversed and excessive applied voltages are old established favourites on the road to ruin, and eventually there arrives the day when a box or a drawer full of assorted devices of dubious antecedence are left for the pupil or the student to take his or her pick, and (when the experiment doesn't do what it should) ruminate on whether the trouble is due to their incompetence, the circuit design or the bits they are using.

Some transistors pack up completely and it doesn't take too long to spot the cause of the trouble. However the main problem usually arises from those transistors that give the appearance of working but have in fact poor gain or excessive leakage, so that things half function and the circuit designer (if he is being followed) gets a lot of unwarranted stick.

But dubious devices apart, it is frequently necessary to select transistors from perfectly good collections for, perhaps, high gain, or to pick out pairs having close gain and current figures for matching purposes, and so on. A transistor checker is then a useful piece of test equipment.

REQUIREMENTS

What is needed is not a complicated box of tricks which will provide us with every parameter a transistor possesses, most of which the amateur experimenter would have no use for, anyway, but a simple checker that will provide, in a few seconds flat, those reassuring functional checks on diodes and transistors before they are incorporated into equipment.

There have been a number of simple testers published in magazines over the years since the transistor put in an appearance, but I have not seen any which cater for field-effect devices (f.e.t.s) as well as the "ordinary" bipolar types. The circuit to be described will cater for all diodes and both sorts of small-signal transistors as well as, of course, differentiating between *npn* and *pnp* bipolars and *n*- and *p*-channel f.e.t.s.

BASIC PRINCIPLES

The bipolar transistor can usually be summed up for acceptance or rejection by the basic measurements of its *leakage* (saturation) current and its current *gain*. In the case of the f.e.t. the parameters of importance are the *pinch-off* voltage (V_p), the value of the drain current (I_{DSS}) with the gate voltage (V_g) set to zero, and the mutual transconductance (g_m). Diodes, of course, can be checked simply by noting the effectual forward and reverse resistance.

COMMON EMITTER

Starting with bipolar transistors, the effect of leakage becomes most important when the transistor is used in the common-emitter configuration. Suppose in Fig. 1 that an *npn* transistor is connected to collector and base supplies but has its emitter (e) left open-circuited.

A meter included in the collector circuit might be expected to record zero collector current, but actually a small leakage current will flow across the collector-base junction even though it is reverse biased. This leakage is composed of minority carriers (holes in this case) which move across the junction in the direction collector-to-base. But such a movement of holes from collector to base *inside* the device is equivalent to a movement of electrons (as recorded, *outside* the device) in the direction base-to-collector.

This current therefore shows itself in the external circuit as an *addition* to the collector current I_c which will flow normally when the emitter is reconnected. This unwanted part of I_c is designated I_{CBO}, and is temperature dependent. In a silicon transistor it amounts to only a few nanoamps under normal conditions, but can be considerably higher in a germanium device.

If a transistor is now connected as shown in Fig. 2, this time with the base (b) left open, the leakage current I_{CBO} which still

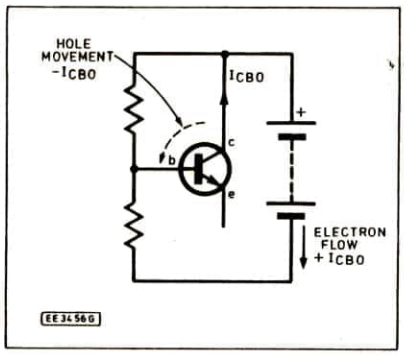


Fig. 1. The effect of leakage current.

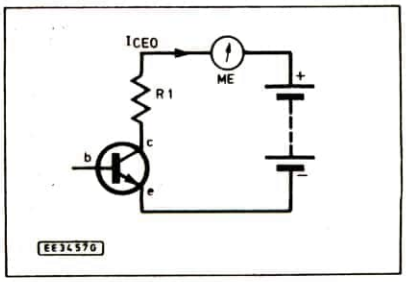


Fig. 2. How leakage is amplified by transistor action.

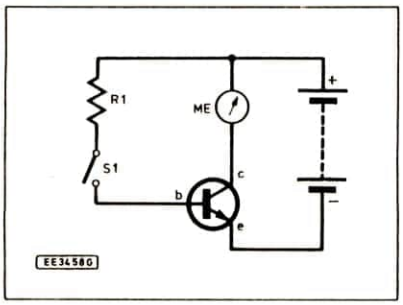


Fig. 3. Method of measuring static current gain.

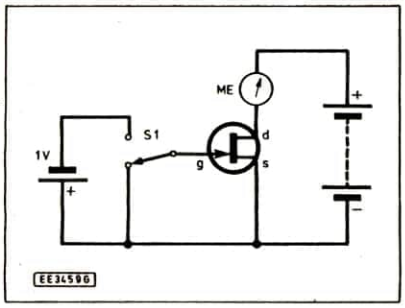


Fig. 4. Method of measuring transconductance.

flows, will be treated as a base input signal and will be amplified by the transistor to give a collector current expressed as I_{CEO}. This current may well be several hundred times the value of I_{CBO} and hence may be significant in determining the thermal stability of an amplifier when it becomes an unwanted part of the main collector current.

The checker will measure I_{CBO} and the effect of its amplification in the common-emitter configuration, that is, the value of I_{CEO}. The I_{CEO} is simply measured by using the basic circuit of Fig. 2.

The transistor under test has its base connection left "open circuit" and the amplified leakage is shown on a microammeter ME1 (protected to full scale deflection (f.s.d.) by resistor R1) wired into the collector circuit. In a good silicon device the current, even though amplified, will normally be negligible but in a poor example it may run to several microamps.

Germanium transistors have relatively high I_{CBO}'s even when perfectly good, and I_{CEO}'s up to 100μA are not uncommon, particularly in some of the older types. Anything over this figure should certainly be rejected.

CURRENT GAIN

Turning now to the measurement of current gain, the d.c. gain of a transistor (or its static common-emitter amplification factor h_{FE}) is a figure indicating how many times the base current is effectually contained in the collector current. In other words, how well is it amplifying?

This is determined by measuring the change in collector current resulting from a known change in base current. Fig. 3 shows a common method (there are others); here resistor R1 is selected so that when switch S1 is operated, the current flowing through R1 into the base is some precise figure, say, 10μA.

By suitable scaling, the collector current as measured on the meter ME1 will indicate a direct value for the current gain. This gain figure is for purely *d.c. conditions:* the a.c. gain or dynamic gain figure (h_{FE}) when a load resistor is used in the collector circuit, is always less than the static gain, in general about 10 per cent smaller.

CHECKING F.E.T.s

For the f.e.t., the diagram of Fig. 4 shows the basic circuit arrangement for the measurement of I_{DSS} and g_m. With switch S1 in the position shown, the gate (g) of the f.e.t. is "earthed" and the milliammeter ME1 gives a direct reading of I_{DSS}. When the switch is changed over, the gate (g) is biased by −1V and the drain current falls.

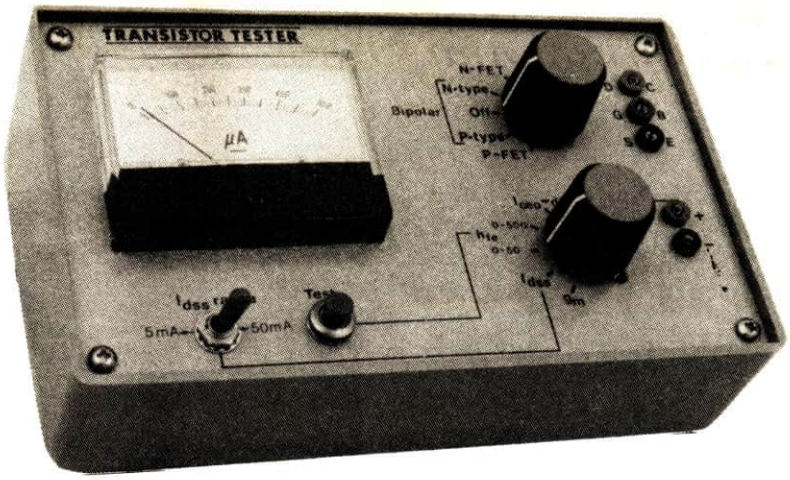
The mutual transconducante g_m is a measure of the change in drain current divided by the change in gate voltage. Since the gate change is one volt, the change in the meter current gives a direct indication of g_m, that is, so many milliamps-per-volt or, as it is usually expressed, so many milli-siemen.

A close approximation to the pinch-off voltage is obtained from a simple relationship between I_{DSS} and g_m which will be given later.

The above descriptions have been made assuming *npn* transistors and *n*-channel f.e.t.s. For *pnp* transistors and *p*-channel f.e.t.s, all supply voltage polarities are simply reversed. We are now ready to combine these basic systems into the complete checker.

CIRCUIT DETAILS

The complete circuit diagram of the Transistor Checker is shown in Fig. 5, and this



contains all the forms of the basic systems discussed earlier under Fig.2, Fig.3 and Fig.4.

The amount of switching might seem off-putting at first sight, but provided the work is approached in a logical way, things are not so fraught as they might appear. There are two main switch assemblies involved; S1 having three wafers each of 2-pole, 5-way; and S2 made up of two wafers, each also 2-pole, 5-way.

One of the poles on S2 is not used. For both these switches, 2-pole, 6-way wafers are used but the mechanism is stopped off at the 5-way position.

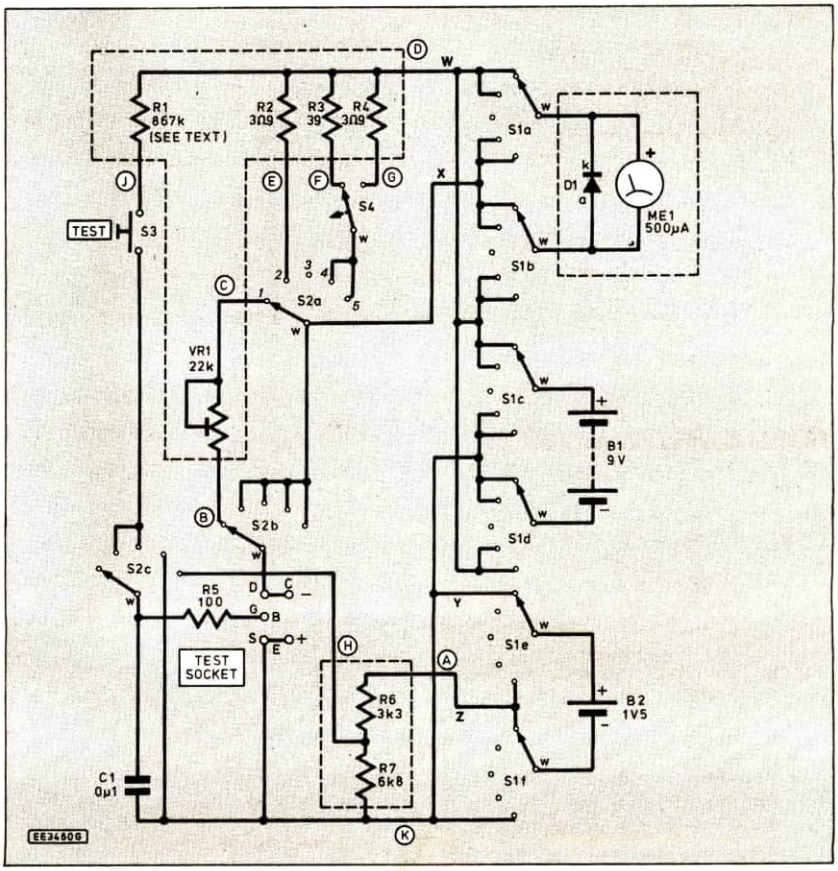
The only other components are seven resistors, a preset potentiometer, a capacitor, a 500μA moving coil meter ME1, diode D1, a biassed toggle switch and a push-to-make push button switch S3, plus coloured terminals and knobs. Most of the resistors go on to a simple circuit board for convenience and this is fitted directly to the terminals of the meter.

The whole assembly is consequently built on to a single aluminium panel which fits into a small "console" type ABS plastic case measuring 159mm by 91mm by 61mm. Any alternative style of case may of course be used provided it has adequate space.

POLARITY SWITCHING

The first wafer of switch S1, that is, S1a and S1b, are simply reversing switches for the meter ME1. The meter terminals are changed over to suit the polarity when either *npn* or *pnp* (or *n*- or *p*-channel f.e.t.s) are being tested.

Fig. 5. Complete circuit diagram for the Transistor Checker. Switch S1 is shown in the N-FET position and S2 in the I_{CEO} – Diode position. Components enclosed in dotted lines are mounted on the p.c.b. Circled letters refer to connections on the circuit board.



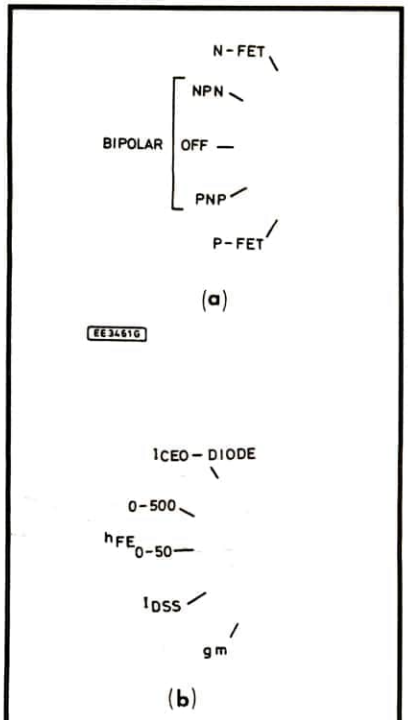


Fig. 6. Front panel legends (full size) required at 30 degrees indexing for Polarity switch (top) and Function switch (above).

COMPONENTS

Resistors

R1	867k (820k + 47k, (see text)	
R2, R4	3Ω9 (2 off)	
R3	39	
R5	100	
R6	3k3	
R7	6k8	

See SHOP TALK Page

All 0.25W 5% carbon or better

Potentiometer

VR1	22k min. skeleton preset

Capacitors

C1	0μ1 ceramic disc

Miscellaneous

ME1	500μA Altai type T23
S1	6-pole 5-way, three wafers each 2-pole 5-way
S2	3-pole 5-way, two wafers each 2-pole 5-way
S3	Push-to-make pushbutton switch
S4	Min. changeover toggle, biased one side

Plastic ABS console type case, 161mm x 96mm x 61mm/39mm; 1mm wander plug and socket, 1 green, 2 red and 2 black; miniature crocodile clips (3 off); 9V battery, type PP3; 1.5V cell; 19mm (¾in.) collet knobs, 2 off; various colours of connecting wire; solder pins (12 off); solder etc.

Printed circuit board available from *EE PCB Service*, code EE781.

Approx cost guidance only **£35** *excl. batts.*

Similarly, the second wafer, S1c and S1d, reverses the polarity of the 9V supply (battery B1) for the same reason. Wafer S1e and S1f also reverses the polarity of the f.e.t. gate supply battery B2 when f.e.t.s are being checked.

The relevant functions of the switch positions are indicated in Fig. 6(a). Use this as your lettering guide on the front panel.

FUNCTION SWITCH

Switch S2 selects the various measuring modes after S1 has been set to suit the type of device being tested. Looking at the circuit diagram, in the position shown (I_{CEO}-Diode), the meter is connected in series with preset potentiometer VR1 (wired as variable resistor) and the transistor (or diode) under test.

For a transistor, the base connection is an open-circuit and hence the meter will read the leakage current I_{CBO}. For a diode, the forward conduction will be indicated.

The second and third positions of S2 give an indication of current gain, h_{FE}, after the manner shown earlier in Fig. 3. On the second position resistor R2 shunts the meter and converts it to read 5000μA (5mA) f.s.d.; in the third position the meter is left unshunted.

When the pushbutton switch S3 is pressed, 10μA flows through resistor R1 into the base (b) of the test transistor, hence the meter indicates either a maximum h_{FE} of 500 (position 2) or 50 (position 3). This last sensitive position should only be used for cases of h_{FE} which fall below 50 on the 500 range.

The fourth and fifth positions of the switch are reserved for f.e.t. testing; on the fourth position I_{DSS} is shown on the meter (now shunted by resistor R3 to read 50mA f.s.d.). If the reading is very small, an auxiliary switch S4 converts the f.s.d. to 5mA; this switch is normally biassed to the least sensitive position.

The fifth switch position (as per Fig. 4. earlier) puts a 1V potential of appropriate polarity, derived from the 1.5V cell B2 via the resistor divider chain R6, R7, on to the gate of the f.e.t. and hence, by the change noted in I_{DSS}, provides an indication of g_m. The legends required on the front panel for this switch are given in Fig. 6(b)

CONSTRUCTION

The front panel drilling measurements are given in Fig. 7. These measurements suit the original panel which is 155mm by 90mm. The hole size for the meter also suits the specified meter; the holes for this can be marked out using the packing piece as a guide.

All the front panel lettering should be added after drilling but *before* any of the components are mounted. The switch positions are indexed out at 30 degrees intervals on a radius from the fixing hole which suits the knobs you are going to use. Collet, 19mm (¾in.), type knobs were found to be best as there is then no problem with the alignment of the pointer-mark when they are fitted and no precise orientation of the switches on the panel is necessary.

SWITCH WIRING

It is best to wire up the wafers of switches S1 and S2 before fixing them to the front panel. If each wafer is wired up systematically and interconnections made where necessary between the wafers, there is no real problem about the job; all that is needed is a logical progression from each wafer to the next.

If you look again at the main circuit diagram Fig. 5, there are connections from the wipers (w) of each of the three wafers of S1 which go to: (i) the meter, (ii) the 9V battery, (iii) the 1.5V cell. Solder distinctive coloured wires on the switch wipers for easy identification.

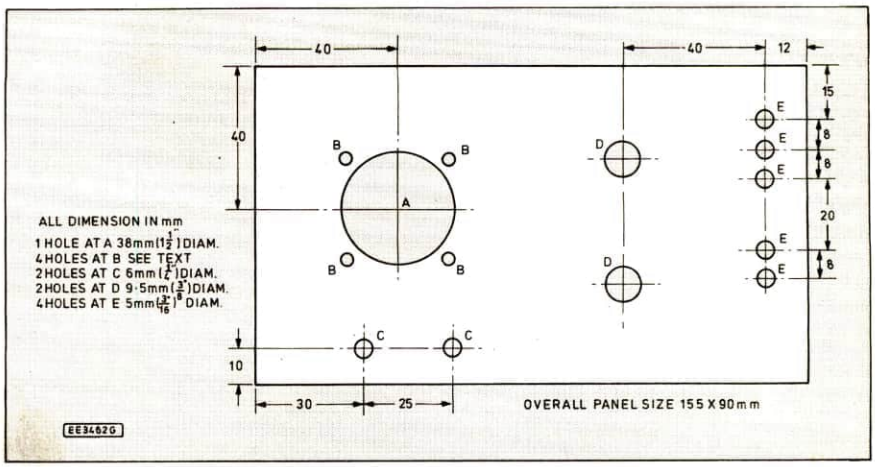
Again looking at the diagram, notice that there are only *four* leads which actually come from these wafers to connect with the remainder of the circuit; these are indicated by the letters *W*, *X*, *Y*, *Z*. Once the interconnections between wafers have been made, the switch can be mounted on the front panel.

The same procedure applies to switch S2; most of the outgoing wires (in this case shown as circled letters on the circuit diagram) go off to a small printed circuit board (p.c.b.) which will be described in a moment. Again, the use of coloured leads will avoid confusion.

The pushbutton switch S3 and the biassed changeover switch S4 are mounted immediately below the meter, while the input test sockets are fitted on the right of the panel as the photographs show. The group of three sockets are for bipolar and field-effect transistors and are marked D-C, G-B and S-E, representing either drain, gate, source or collector, base, emitter inputs respectively. The two lower sockets are for diode testing and are marked + and − (plus and minus) respectively.

The terminals used are 1mm type coloured sockets which are bought together with matching 1mm plugs. You can use spring

Fig. 7. Front panel drilling details. The meter hole drilling depends on unit used.



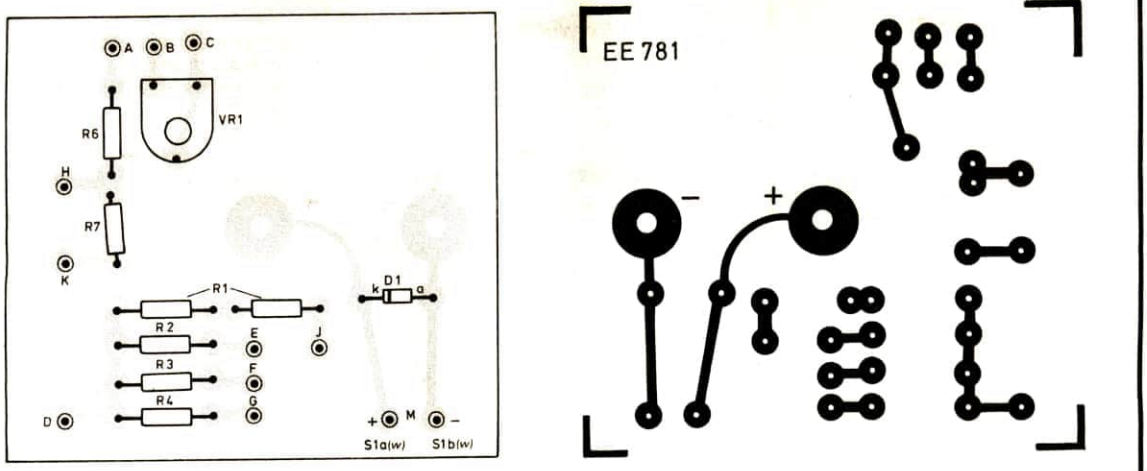


Fig. 8. Printed circuit component layout and full size copper foil master pattern. Resistor R5 and capacitor C1 are wired directly between switch wafer and output sockets.

type terminals as an alternative but watch the available space.

The method of connecting transistors adopted by the author utilises three miniature crocodile clips connected by short flexible leads to the 1mm plugs which then go into the appropriate sockets. Some of the older transistors had leads sufficiently long to plug directly into the sockets but these are now few and far between; using croc' clips will accommodate practically every style of transistor output configuration.

CIRCUIT BOARD

Apart from the switches and sockets, most of the remaining discrete components are mounted on a small printed circuit board; the exception being resistor R5 and capacitor C1. This board is available from the *EE PCB Service*, code EE781.

The p.c.b. is screwed directly on to the meter's rear terminals and carries all the resistors except R5 which, along with capacitor C1, is hard wired directly between switch wafer S2c wiper or pole contact and the appropriate sockets. The full size copper track layout and component dispositions are given in Fig. 8 where the lettering refers to that shown on the circuit diagram; this makes the interwiring from the switch leads and the connections to switches S3 and S4 relatively easy.

Preset potentiometer VR1 should at this point be set to its maximum resistance position, fully anticlockwise. It is important to note in passing that the values of the shunt resistors R2, R3 and R4 apply *only* to the specified meter and will have to be modified if you use an alternative meter.

Resistor R1 is actually made up from an 820k in series with a 47k; we need 10μA to flow into a transistor base when switch S3 is pressed but the base-emitter voltage drop is different for silicon and germanium devices. Assuming the battery p.d. is 9V, then about 8.4V is available for a silicon device and about 8.75V for a germanium one.

Hence, to get 10μA to flow a compromise is necessary in the value of resistor R1. So 867 kilohms seems reasonable, though there is not much point in being pedantic about this, bearing in mind the tolerance of the resistors, and the variation in the potential barrier voltage of different transistors.

The two batteries are located beneath and to either side of the circuit board. They are fixed to the front panel with double-sided sticky pads. The 9V supply battery is positioned nearest the wafer switches, see photographs.

With the simple p.c.b. used here, it is no problem to use either etch-resistant transfers or a Dalo pen to map out the tracks. The only critical spacing is that for the meter fixing holes which must be exactly 25.4mm (1in.) apart. Use solder pins as the connecting points for the incoming wires.

SETTING UP

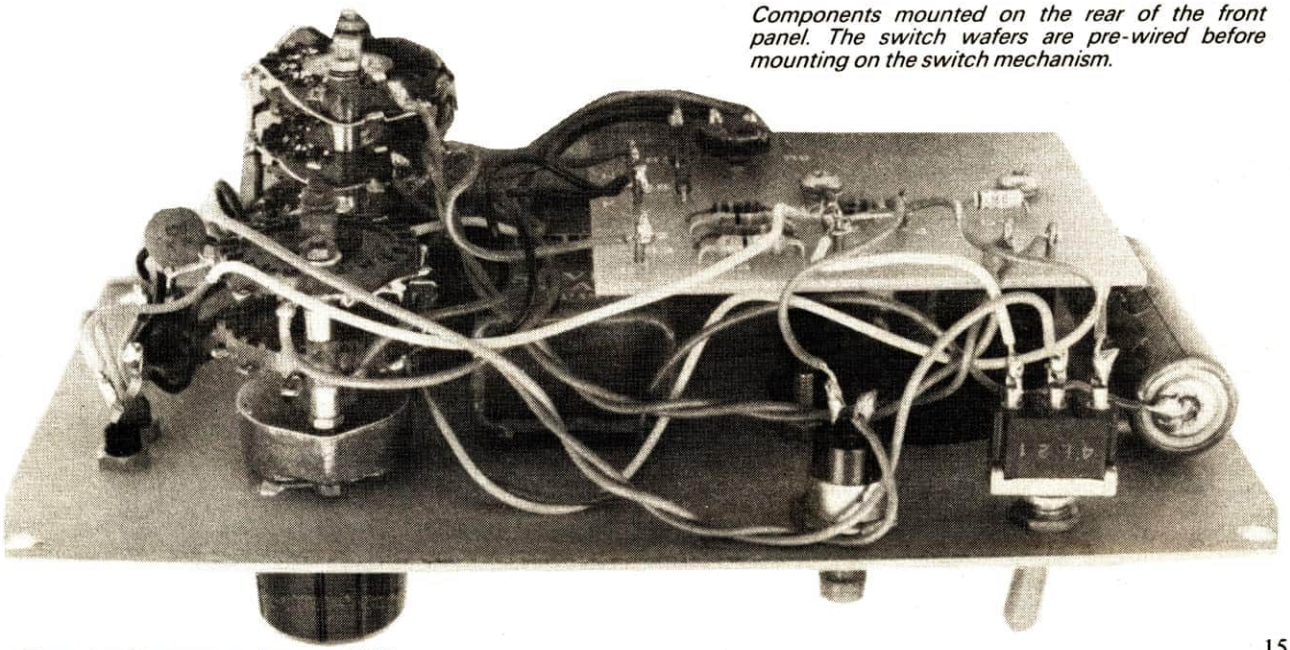
With the project assembled and with the batteries in place, a quick preliminary check can be made. This is quite simple as only preset VR1 needs adjustment to give the meter a full-scale reading on the available battery voltage.

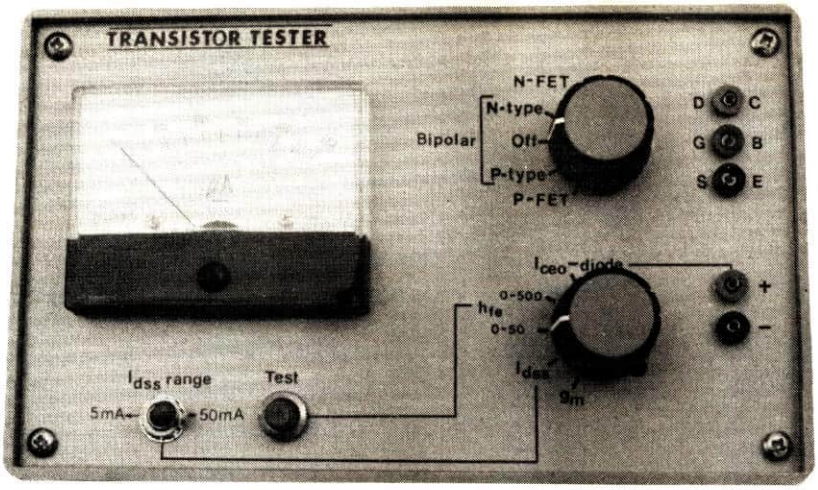
With S1 set to OFF and S2 set to I_{CEO} Diode, short out the input sockets C and E. Then switch S1 to either the *npn* or *pnp* position and adjust VR1 to provide a full-scale reading on the meter.

This completes all that is strictly necessary for the operation of the tester but you can if you wish check on the accuracy of the meter shunting for the h_{FE} ranges. To do this, connect a 47 kilohms (or thereabouts) variable potentiometer, resistance fully in, across the C-E terminals.

Switch S1 to either *npn* or *pnp* and switch S2 to the h_{FE} 0-50 range. Adjust the pot carefully to give f.s.d., then turn switch S2 to

Components mounted on the rear of the front panel. The switch wafers are pre-wired before mounting on the switch mechanism.





Front panel layout and lettering.

the 0-500 range. Check that the meter now reads 50 on this 0-500 range. For any *serious* error, say, a reading outside 45-55, resistor R2 will need adjusting.

OPERATION

Here is a brief summary of the procedures for testing diodes, bipolar and field-effect transistors. Always start with the instrument switched OFF and with the Function switch set to I_{CEO}-Diode.

Diodes

To check a Diode: Connect the marked end of the diode (the cathode (k)) to the negative terminal and the anode (a) to the positive terminal. With S2 on I_{CEO}-Diode, switch S1 to the PNP position; the meter should then indicate the forward conduction of the diode, generally close to a full scale reading.

Switch now to the NPN position on S1. The meter will now indicate the diode reverse leakage which for a good diode should be undetectable.

Transistors

To check a bipolar transistor: Assuming an *npn* device, connect the collector (c), base (b) and emitter (e) leads to the appropriate terminals. Set the function switch to I_{CEO}-Diode and the polarity switch to NPN.

The meter will now indicate the open-base *leakage* current I_{CEO} on a 500µA full-scale deflection. For a good silicon transistor this reading should be negligible but for a germanium transistor a current of 100µA might not be unusual, particularly for some of the older types.

To check the *gain*, switch to the h_{FE} 0-500 position and press the Test button S_3. The meter will indicate the static current gain directly; if the reading is less than 50, switch to the 0-50 position.

In cases where the leakage is appreciable, make a note of the meter reading *before* pressing Test switch S3; *deduct* this reading from that obtained when S3 is pressed to get a true value for h_{FE}. It is the *change* in the current which matters.

To determine whether a transistor is *npn* or *pnp* use can be made of the diode terminals. Put the collector lead into the + socket (plus) and the combined emitter and base leads, *shorted together*, into the – socket (minus). Switch the function switch alternately to PNP and NPN; then the position which produces the full-scale reading (or very close to it) is that which suits the type of transistor under test.

Field Effect Transistors

To check a f.e.t.: Assuming an *n*- channel f.e.t. connect the drain (d), gate (g) and sources (s) leads to the appropriate terminals. Set the Function switch to I_{DSS} and the polarity switch to N-FET.

The meter will now indicate (on a 50mA f.s.d. range) the drain current for zero gate volts. If the reading is below 5mA, operate the biassed switch S4 to give a 5mA f.s.d. range. Note this reading.

Switch now to g_m; the previous I_{DSS} reading will decrease, a bias of 1V now being applied to the gate. The *change* in the current will give an indication of g_m either in mA/V or millisiemen.

To evaluate V_p (the *pinch-off point*) use the simple relationship:

$$V_p = \frac{-2I_{DSS}}{g_m}$$

Thus, for example, if I_{DSS} = 4mA and g_m = 1.5mA/V (or 1.5 millisiemen) then:

$$V_p = \frac{-2 \times 4}{1.5} = -5.3V$$

PRECAUTIONS

At all times, when carrying out tests, make sure that the clips to the "transistor under test" do not short together *before* switching the unit on; failure to do this could lead to the meter "cracking" over and the result could be a bent pointer. *Always* return switch S1 to OFF before connecting or removing a transistor.

Most small-signal type transistors and f.e.t.s can be checked on this instrument, as can most *small* power silicon types: *high* power types *cannot* be tested accurately because of the low collector currents used. □

The completed tester showing the two batteries secured (with double-sided sticky pads) beneath the circuit board. The resistor R5 and capacitor C1 can just be seen on the left.