# MOS TAP

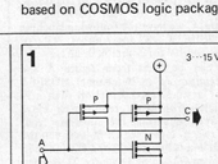
Solid state circuits are increasingly intruding into fields that were once the domain of electromechanical components, but only recently has it become possible economically to replace the simple electromechanical switch by an electronic system with no moving parts — the Touch Activated Programmer (TAP). In last month's issue a TAP was described which utilised TTL IC's. This month we publish a new design based on COSMOS logic packages.

In line with the Elektor policy of continuous development and utilisation of new technologies a TAP has been developed which uses COSMOS IC's. As will be explained later in the text this offers greater circuit simplicity than the TTL TAP but, since COSMOS prices are higher, this circuit is more expensive than the TTL TAP. Readers thus have two designs from which to choose; a TTL TAP using cheap, readily obtainable components, or a MOS TAP using 'state-of-the-art' devices at slightly higher cost. The main advantages offered by the MOS TAP are as follows:

- micropower quiescent operation.
- excellent noise immunity (typically 45% of the supply voltage).
- wide supply voltage tolerance (3–15 V).
- high input impedance (typically $10^{12}\,\Omega$) therefore, unlike the TTL TAP, no input buffers are needed.

The MOS TAP is based on an RCA COSMOS IC, the CD4011AE, which is a quadruple two-input NAND-gate. The circuit of one of the gates is given in figure 1. It consists of two complementary pairs each comprising a P-channel FET and an N-channel FET.

When inputs A and B are both high ($+V_b$) the P-channel FET's are cut off. The two N-channel FET's are turned on and the output is in the low or '0' state, which is a resistance of 400-800 between point C



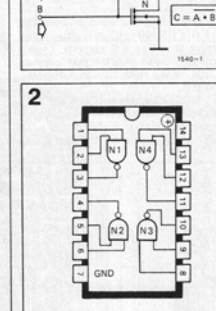




**Figure 1. The circuit of one of the NAND-gates in a CD4011AE. Note the use of complementary pairs of P- and N-channel MOSFET's.**

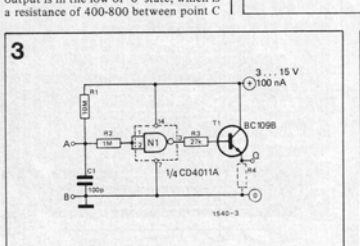
**Figure 2. The pinout of the CD4011AE DIL package. The configuration is different from the 7400 used in the TTL TAP.**

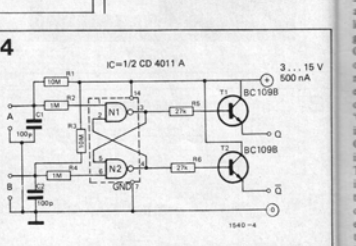
**Figure 3. The 'push-button' is the simplest application of a COSMOS NAND-gate as a touch-switch. If points A and B are bridged by a finger the output of the gate will become '1'. If the contacts are released the output becomes '0' again. $T_1$ is an emitter-follower to increase the output current capability.**

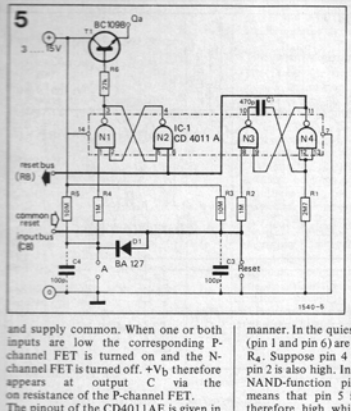
**Figure 4. The basic element of the multi-position switch is a set-reset flip-flop. It is shown here with two sets of touch contacts, but one of these is replaced by the reset bus RB in the final circuit.**

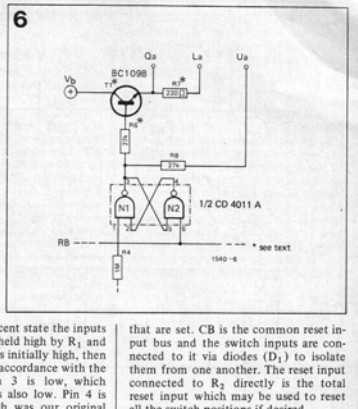
**Figure 5. The basic configuration of the reset circuit. The monostable $N_3/N_4$ produces a reset pulse when input A is touched. This goes out along the RB bus to reset the other switch positions, which, for simplicity are not shown.**

**Figure 6. Detail of the output circuitry for one switch position. The functions of the three outputs are detailed in the text.**






and supply common. When one or both inputs are low the corresponding P-channel FET is turned on and the N-channel FET is turned off. $+V_b$ therefore appears at output C via the on resistance of the P-channel FET.

The pinout of the CD4011AE is given in figure 2. Note that it is not the same as the pinout of the 7400 which was used in the TTL TAP. The IC is also available in a (more expensive) ceramic package as the CD4011AD. This has the same pinout as the plastic-packaged CD4011AE. For those who are unfamiliar with MOS devices it is worth noting that since the devices are of insulated-gate construction they should be handled with care as static charges can easily destroy the device. In particular it is recommended that an IC socket be used, neither should the device be plugged into nor removed from the circuit with power applied.

## The NAND-gate as a 'push-button'

The basic principle of the MOS TAP is illustrated in figure 3. In the quiescent state the inputs of the gate (which for this example are tied together) are held at $+V_b$ by $R_1$. The output is therefore low. If points A and B are bridged by a finger the input will be held low by the skin resistance, which is a maximum of about 2MΩ for dry skin and considerably less for moist skin. The output of the gate will therefore become high. Since COSMOS can supply only 500μA or so output current an output buffer may be required for some applications. The emitter follower $T_1$ provides this. If the output is required to sink current in the '0' state $R_4$ must be included. $R_2$ is an input protection resistor for the IC and $C_1$ helps improve the transient noise immunity.

This simple circuit is, of course, useless if latching operation is required so, like the TTL TAP, the MOS TAP is based on set-reset flip-flops. One flip-flop is employed for each switch position and the circuit of one such flip-flop is given in figure 4. It operates in the following manner. In the quiescent state the inputs (pin 1 and pin 6) are held high by $R_3$ and $R_4$. Suppose pin 4 is initially high, then pin 2 is also high. In accordance with the NAND-function pin 3 is low, which means that pin 5 is also low. Pin 4 is therefore high which was our original premise. This is one of the two stable states of the flip-flop. Suppose now that input A is touched. This means that pin 1 is held low. Pin 3 therefore becomes high, and since 6 and 5 are high 4 becomes low. This holds pin 2 low so that even when the touch contact is released the circuit remains in this state. If input B is now touched the circuit reverts to its original state. We thus have a two-position switch.

## Extension to multi-position switch

There are various ways of extending the system. One way would be to use NAND-gates with several inputs to make an "n-stable" flip-flop. One NAND-gate would be required for each switch position. In practice this would be very cumbersome since an n-position switch would require NAND-gates with n+1 inputs. It would also be impossible to further extend the system once it had been built, and of course a different design of printed circuit board would be required for each different number of positions required.

The MOS TAP described in this article uses the same system as that described for the TTL TAP. The switch may be extended to any number of positions using the set-reset flip-flop previously described and the latching operates by using a common reset monostable so that when any contact is touched a reset pulse is produced which cancels all the other switch positions.

The principle of operation of the reset circuit is illustrated in figure 5, which shows one switch position plus the reset monostable. When input A is touched the monostable consisting of $N_3$ and $N_4$ is triggered and produces a reset pulse of about 50 mSec. which goes out along the reset bus RB to reset any positions that are set. CB is the common reset input bus and the switch inputs are connected to it via diodes ($D_1$) to isolate them from one another. The reset input connected to $R_2$ directly is the total reset input which may be used to reset all the switch positions if desired.

## The output circuitry

Before describing the circuitry of the complete TAP it is necessary to clarify some points concerning the output circuits. As can be seen from figure 6 only the Q output of the flip-flop is used. $T_1$ is a buffer emitter follower, as described earlier. When the flip-flop is in the reset state $T_1$ is cut off; when the flip-flop is set, however, a voltage of $+V_b-0.7$ V. appears at the $Q_a$ output (0.7 V. is the base emitter voltage drop of $T_1$). The current which $T_1$ can supply is limited by $R_6$ and depending on the gain of $T_1$ can be between 100 and 200 mA; the $Q_a$ output is thus short-circuit proof. The optimum value of $R_6$ is given by:

$$R_6 = 2 \times 10^3 \times V_b$$

where $R_6$ is in ohms and $V_b$ in volts.

The total current which can be supplied by outputs $Q_a$ and $L_a$ together is approximately:

$$I_{Q_a} + I_{L_a} = 5 \times 10^{-1} \times h_{FE_{T_1}}$$

The current is in milliamps. $h_{FE_{T_1}}$ is the common-collector current gain of $T_1$.

Output $L_a$ is intended to drive a LED (or lamp) to indicate when a particular switch position is energised. For a typical LED with a voltage drop of about 1.5 V. at 40 mA. $R_7$ is given by:

$$R_7 = \frac{V_b - 2}{4 \times 10^{-2}}$$

Since the base-emitter voltage of $T_1$ will vary with temperature output $U_a$ is provided for applications requiring a stable output voltage (the output voltage of $U_a$ is equal to $V_b$ so if the supply is stable output $U_a$ will be). Of course this output can only supply about 500 μA.

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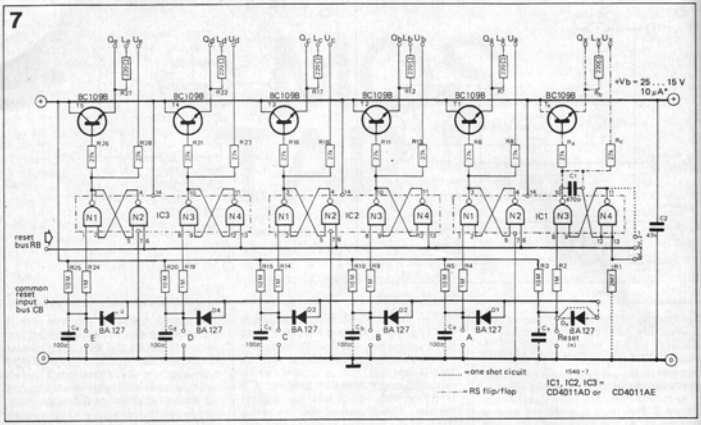


## The complete MOS TAP

The circuit of the complete five-position MOS TAP is given in figure 7. As can be seen from the circuit each input is connected to the common reset input bus CB via a diode ($D_1 - D_5$). These isolate the inputs from one another. $N_3$ and $N_4$ are the reset monostable.

The system may be extended simply by adding extra boards. In this case, since only one reset monostable is required for the entire system, $N_3$ and $N_4$ on the additional boards may be converted to extra switch positions by adding the components shown in the dot-dash lines, i.e. $D_X$, $T_X$, $R_a$, $R_b$, $R_c$. The components shown in dotted lines (i.e. $R_1$, $C_1$ and the links across $D_X$ and between pin 11 of the IC and pins 1 and 2 of the board) are omitted. Note the new link between

**Figure 7. The circuit of the complete MOS TAP. This has five switch positions, but if the system is extended the monostable on additional boards can be converted to a flip-flop, thus providing six extra positions per board.**

**Figure 8. The printed circuit pattern for the MOS TAP.**

**Figure 9. The component layout of the basic MOS TAP.**

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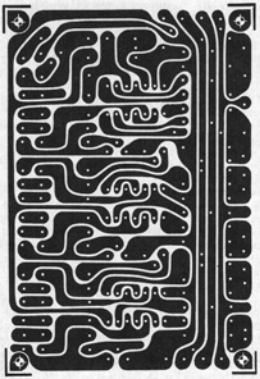

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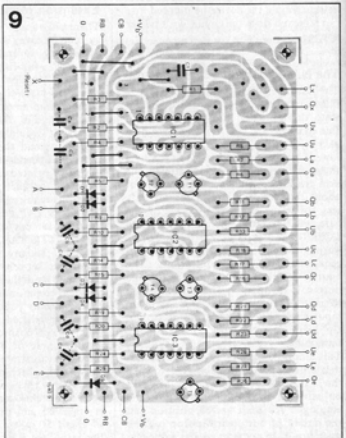


**Parts list for figures 7, 9 and 10.**

Resistors:
$R_1$ = 2M7
$R_2$,$R_4$,$R_9$,$R_{14}$,$R_{19}$,$R_{24}$ = 1M
$R_3$,$R_5$,$R_{10}$,$R_{15}$,$R_{20}$,$R_{25}$ = 10M
$R_6$,$R_8$,$R_{11}$,$R_{13}$,$R_{16}$,$R_{18}$,$R_{21}$,$R_{23}$,$R_{26}$, $R_{28}$ = 27k*
$R_7$,$R_{12}$,$R_{17}$,$R_{22}$,$R_{27}$ = 220Ω*

Capacitors:
$C_1$ = 470p
$C_2$ = 47n
$C_a - C_e$ = 100p*

Semiconductors:
$IC_1$,$IC_2$,$IC_3$ = CD4011AE or CD4011AD (RCA)
$T_1 - T_5$ = BC109b or BC109c
$D_1 - D_5$ = BA127* or equivalent

For the extension board $C_1$ and $R_1$ are not required.
The following additional parts are needed.

$R_a$,$R_c$ = 27k*
$R_b$ = 220Ω*
$D_x$ = BA127
$T_x$ = BC109b or BC109c

* See text.

**Figure 10. The extension board component layout. Note the differences between this board and figure 9.**

**Photo 1. The completed five-position MOS TAP.**

pins 2 and 3 of the board, and the link which replaces $C_1$.

## The printed circuit board

The board for the basic MOS TAP is given in figure 8 and the associated component layout in figure 9. The board layout for extending the system is shown in figure 10. The component differences to the left of $IC_1$ can be clearly seen. It can be seen that the supply tracks $+V_b$, 0 V. and the reset lines RB and CB are available on both edges of the board, so that extending the system is simply a matter of linking across. The capacitors $C_a - C_e$ and $C_x$ are included to improve the transient noise immunity, but they may not be required in every case. If it is desired that the switch should set in a particular position on switching on the supply than all these capacitors should be omitted, except the one connected to that switch position.
Note that diodes $D_1 - D_5$ and $D_x$ must have very low reverse leakage, less than 200 nA., so DUS cannot be used in this circuit. If these diodes are omitted then the CB rail has no effect. In that case any number of switch positions may be on simultaneously and they can only be reset by touching the reset input connected directly to the reset monostable.

## Power Supplies

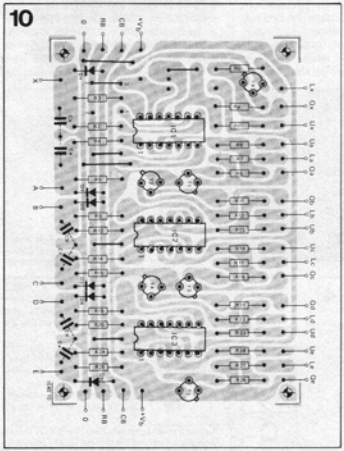
The MOS TAP will operate from any supply between 3 and 15 V. The current consumption is very low, less than 10 μA. at 15 V. but of course any output current the circuit must supply is added to this.

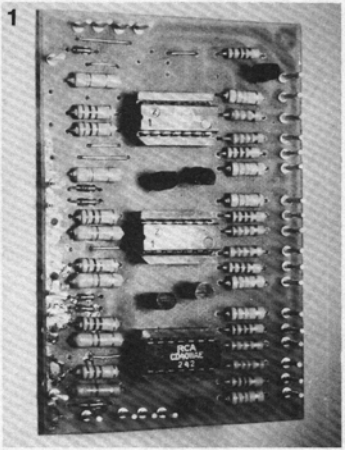
## Precautions

As mentioned earlier COSMOS IC's must be treated with extreme care, and in particular the use of an IC socket is recommended. If the device is soldered directly into the circuit use an earthed soldering iron.

## Touch contacts

The design of the touch contacts is up to the user, but should be such that they cannot be accidentally bridged by dirt, moisture etc. When a supply of less than 10 V. is used it is generally possible to employ single-point touch contacts (no earth return) as the circuit will operate from hum picked up by the body capacitance rather than from the skin resistance. Screened leads should be used in both cases if the input lead length exceeds 5 cm. and the screening should be connected to supply common (0 V.) at one end only.



# COS/MOS digital ICs

COS/MOS is a development of bipolar IC technology and an offspring of the MOS (Metal Oxide Semiconductor).
It started with the MOSFET being developed from the universally known junction FET (Field Effect Transistor). The former distinguish themselves from the latter by their isolated gate. The result of this gate isolation is a particularly high gate resistance. A drawback is that a static charge can build up on such a gate when the transistor is not connected in a circuit. This charge usually causes the immediate destruction of a MOSFET because the extremely thin isolating layer breaks down. So the handling of MOSFETs calls for special precautions. This also applies to COS/MOS ICs in which MOSFETs are integrated.

The integration is such that P+ and N- channel transistors are used alternately. Furthermore the switching circuits are integrated symmetrically. The latter two characteristics form the basis for the term COS (COmplementary Symmetry). Thus COS/MOS can be briefly described as complementary symmetrical MOSFET integration. A simple example of a COS/MOS IC construction is given in figure A. Here the dark-shaded area represents the n- (polarized) substrate. The diagonally-hatched area is the metal oxide film on which the electrical contacts are made. These contacts are drawn in deep black. Below the isolating layer at the electrical contact interruptions are the p- and n- layers. The layers are so integrated that the result is a complementary MOSFET pair as shown in figure B. Corresponding to the labelling of figure A, we have the following labelling in figure B: 'S' for sources, 'G' for gates and 'D' for common drain.

As can be seen from figure A the integration of an N- channel MOSFET is of a simpler construction than a P-channel. The latter requires an extra p- layer separating the substrate from the two n- layers which lie between the drain and G2 (= gate 2) and the junction between G2 and S2 (= source 2), respectively.

Of course, the integration of even the simplest COS/MOS IC is slightly more complex than figure B suggests. Even a common 2-input NAND gate consists of no less than four integrated MOSFETs.
Like MOSFETs, every COS/MOS IC must be handled with due care because the inputs (gates) are isolated with respect to the rest of the integrated circuit. Normally the input impedance of a gate is $10^{12}\ \Omega$. As a result a static charge can easily build up if such an IC is kept in a plastic box, for instance. The human body too, is often statically charged. Touching the inputs with a finger can be sufficient to destroy the COS/MOS IC. Therefore the ICs are packed in a kind of expanded plastic containing a highly conductive substance. The connecting pins of the IC are pressed into the expanded plastic.
To give the inputs some measure of protection, manufacturers often provide COS/MOS IC inputs with an inbuilt protection circuit. These circuits are not shown in the circuit diagrams of the ICs.
Figure C is an example of an input circuit of a COS/MOS inverter. As can be seen in this figure, the circuit consists of a P- and an N- channel MOSFET. In reality the input circuit is as shown in figure D. Here we see that each gate input protection circuit comprises one resistor and three diodes. The diodes $D_4$ to $D_8$ are usually formed in the diffusion process. The gate input protection, however, is added as an extra (a resistor of about 500 Ω plus three diodes).
In figure D the diode $D_3$ has a breakdown voltage of about 25 V. The breakdown voltage of the diodes $D_1$ and $D_2$ is about 50 V.