CMOS QUAD SWITCHES AND MULTIPLEXERS

New Low-Leakage, Low-Dissipation IC's For Analog Circuits

by Roger Van Aken†

Complementary Metal-Oxide Semiconductor (CMOS) monolithic IC technology has been with us for several years and is now widely applied in digital circuitry, ranging from wristwatches to computer mainframes. Its promise is low dissipation, low drive power (allowing greater fanout), and wide voltage swings (hence greater noise immunity). Its uses in analog circuitry, though more limited, are growing; the promise here is near-negligible drive power, low leakage and dissipation, characteristics that happen to be quite interesting for analog switch design.

It has become apparent to Analog Devices that there is a need for high-performance monolithic analog circuitry that takes advantage of the benefits of CMOS. Following a substantial period of development, the products described here represent the first fruits of this technology: the AD7510 quad analog switches, the AD7501 8-channel analog multiplexers, and the AD7502 4-channel dual analog multiplexers.* Additional switches, multiplexers, and other analog-digital interface devices, as well as the possibility of related custom designs, are on the way.

WHAT IS CMOS?

CMOS is the combination and interconnection of p-channel and n-channel MOS field-effect transistors on a single chip to form monolithic integrated circuits. Examples of such circuits are to be seen in Figures 3 and 4, to be discussed shortly.

The structure of a p-channel MOS transistor is shown in cross-section in Figure 1. Starting with an n-substrate, two p^+ areas are diffused in. The portion of the substrate between them will become the channel. Note that two series-opposing P-N junctions are formed, constituting essentially an open circuit. An insulator, a silicon-oxide/nitride sandwich is laid down above the channel, and a metallic contact, the *gate*, is deposited on the insulator, directly above the channel, thus forming a capacitor. When negative voltage is applied to the gate, the channel region becomes positively charged at the interface between the oxide and the silicon substrate, and conduction can take place between the source and drain. The voltage from gate-to-channel at which substantial conduction starts to take place is called the *threshold voltage*.

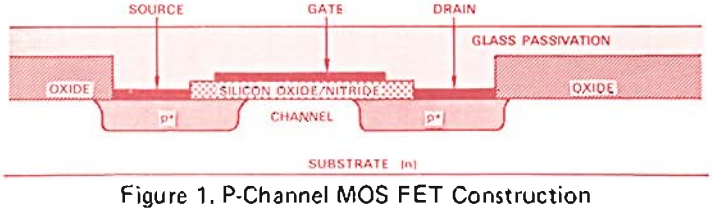

Figure 1. P-Channel MOS FET Construction

The complementary device, an n-channel MOS transistor, is built in essentially the same way, but with a p-substrate and n-diffusions for source and drain. Its channel region conducts when *positive* voltage is applied at the gate.

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*For complete information on these products, use the reply card. Request K2.

Both kinds of device are near-ideal voltage-controlled switches. Since conduction is the result of an applied field, gate current is seen to be virtually non-existent, so drive power is quite low. When non-conducting, the channel is like two diodes back-to-back, so breakdown voltage across the channel can be substantial, and leakage is negligible for most purposes. When conducting, the resistance is a function of applied voltage. (It will be seen that in CMOS switches (Figure 4) resistance is nearly constant, because as one parallel path decreases in conductance, the other increases, and the resistance change is only about 20% over a ±10V range.)

Figure 2 shows a substrate with two complementary devices. Starting with the n-substrate, a p-well is diffused into it; this p-well becomes the substrate for the n-channel transistor. The next step consists of diffusing heavily doped n^+ source and drain regions for the n-channel device, and p^+ source and drain regions for the p-channel device. Then the oxide layers are grown to insulate the gate electrodes.

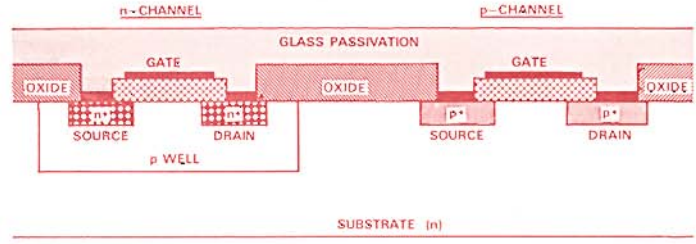


Figure 2. Complementary MOS FET Construction

Figure 3 shows a basic inverter, a complementary pair of p- and n-channel MOS transistors connected in "push-pull" across the supply voltage, with a common gate connection and drain (output) connection. When positive voltage is applied to the gates, the n-channel device conducts and the p-device turns off; the output sinks to a voltage near the negative rail. Only one device conducts at a time, and in the quiescent condition (no load) only leakage current flows (10nW dissipation at ±15V).

Summarizing the advantages of CMOS:

- very low dissipation and leakage current
- extremely high input impedance
- wide power-supply voltage range

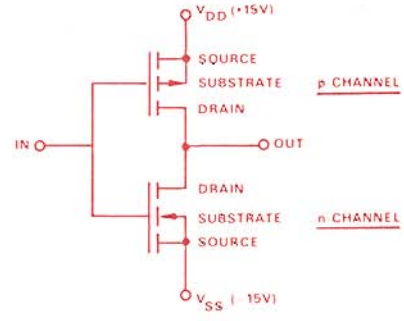


Figure 3. CMOS Inverter

CMOS ANALOG SWITCHES

CMOS devices can be used to form analog voltage-switches having very high resistance in the "open" condition, and less than 100Ω when closed. Figure 4 shows the basic switch configuration.

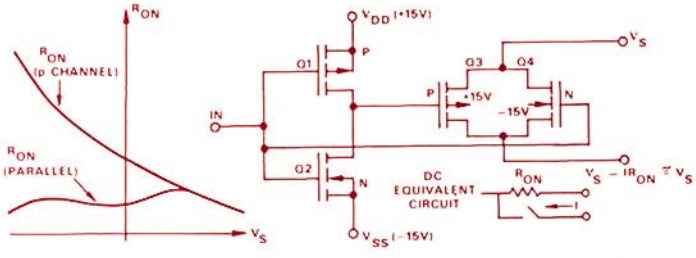


Figure 4. Basic CMOS Switch

Two complementary channels are connected in parallel, with their gates driven in opposite directions by the input and output of an inverter. When the input is *high*, Q1 is off, Q2 is on, and their common drain connection is *low*. The p-channel MOSFET Q3's gate is driven low, so it conducts, and the n-channel Q4 is driven high, so it too conducts, creating a parallel path between points A and B (as long as both terminals are between the extremes of the power supplies and of the input gate drive.

When the input is low, the gates switch polarity, and both Q3 and Q4 are non-conducting.

The curves in Figure 4 show the variation of channel resistance with applied voltage. Although the resistance of the n-channel device increases with positive voltage, and the resistance of the p-channel device increases with negative voltage, their parallel combination changes but little over the whole range, ensuring excellent linearity when loaded by resistance.

THE AD7510 QUAD-SWITCH FAMILY

The AD7510 comprises four independent switches (Figure 5), housed in a hermetically-sealed 16-pin ceramic dual in-line package (TO-116). *On* resistance at +25°C is less than 100Ω (max), with about 20% variation over the ±10V analog signal range. Leakage current of the individual switches is less than 3nA at +25°C (AD7510S) and the total quiescent power requirement (all four switches *off*) is less than 1μA for both (±15V) supplies.

The switches are *on* for high (i.e., positive true) digital input and *off* for low input. The digital control inputs are compatible with DTL/TTL logic, as well as CMOS, with all necessary level-shift circuitry contained on the chip (requiring no additional drive power, except for the "J" version, which requires a 1-2kΩ "pullup" resistor for DTL/TTL compatibility).

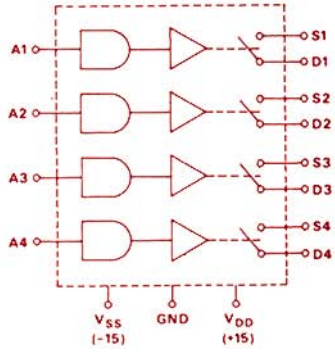


Figure 5. Functional Diagram of AD7510 Quad Switches

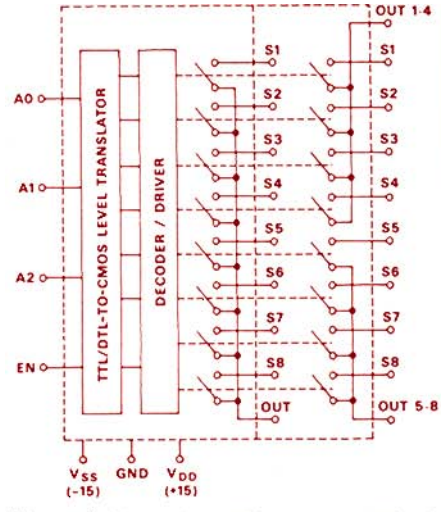
The complete independence of the switches makes possible a wide range of applications, including analog integrators, sample-hold amplifiers, variable-gain amplifiers, D/A and A/D converters, remote-control devices, etc.

The AD7510 is available in three versions: AD7510K, specified for operation from 0 to +75°C, has *off* leakage current less than 5nA at +25°C and 500nA over the temperature range with full-scale analog voltage, and minimum *high* logic level of 2.4V at +25°C; AD7510J has similar temperature range and leakage specifications, but 4.2V minimum *high* logic level; AD7510S is specified for operation from -55°C to +125°C, with 200nA maximum channel leakage, and *high* logic level similar to that of AD7510K. Prices for the J, K, and S versions (1-49) are: $13, $15, and $24.

THE AD7501 AND AD7502 MULTIPLEXER FAMILIES (FIGURE 6)

The AD7501 is an 8-channel multiplexer, housed in a 16-pin ceramic dual in-line package (TO-116), with 3-bit binary addressing and an *enable* line. The AD7502, structurally similar, is a dual 4-channel multiplexer with 2-bit binary addressing and *enable;* it is useful for routing *differential* analog signals. Applications of these devices include multiplexing, digitally-controlled filters, and signal distribution. The *on* resistance for both types is guaranteed to be less than 300Ω at +25°C, with typical variation of 20% over the entire ±10V analog range. The leakage per switch at +25°C is less than ½nA, (S version) and power-supply current is less than 1μA with all digital inputs *low*. The output (i.e., switch common) current leakage is less than 5nA for the AD7501S and 3nA for the AD7502S.

Both the AD7501 and AD7502 are available in a choice of three options, J, K, and S. J and K are for the "commercial" (0 to +75°C) temperature range, and S is for the extended "military" range (-55°C to +125°C). As is the case with the AD7510, the J differs from the K only in requiring an external "pullup" resistor for DTL/TTL compatibility. Prices of both the AD7501J, K, and S, and the AD7502J, K, and S are: (1-49) $28 (J), $30 (K), $44 (S). ▶▶▶



AD7501				
A_2	A_1	A_0	EN	ON
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8
X	X	X	L	NONE

AD7502			
A_1	A_0	EN	ON
L	L	H	1&5
L	H	H	2&6
H	L	H	3&7
H	H	H	4&8
X	X	L	NONE

Figure 6. Functional Diagram and Truth Tables for AD7501 and AD7502 Multiplexers