Ask The Applications Engineer—26

by Mary McCarthy & Anthony Collins*

SWITCHES AND MULTIPLEXERS

Q. *Analog Devices doesn't specify the bandwidth of its ADG series switches and multiplexers. Is there a reason?*

A. The ADG series switches and multiplexers have very high input bandwidths, in the hundreds of megahertz. However, the bandwidth specification by itself is not very meaningful, because at these high frequencies, the off-isolation and crosstalk will be significantly degraded. For example, at 1 MHz, a switch typically has off-isolation of 70 dB and crosstalk of –85 dB. Both off-isolation and crosstalk degrade by 20 dB per decade. This means that at 10 MHz, the off-isolation is reduced to 50 dB and the crosstalk increases to –65 dB. At 100 MHz, the off-isolation will be down to 30 dB while the crosstalk will have increased to –45 dB. So it is not sufficient to consider bandwidth alone—the off-isolation and crosstalk must be considered to determine if the application can tolerate the degradation of these specifications at the required high frequency.

Q. *Which switches and multiplexers can be operated with power supplies less than those specified in the data sheet?*

A. All of the ADG series switches and multiplexers operate with power supplies down to +5 V or ±5 V. The specifications affected by power-supply voltage are timing, on resistance, supply current and leakage current. Lowering power supply voltage reduces power supply current and leakage current. For example, the ADG411's $I_{S(OFF)}$ and $I_{D(OFF)}$ are ±20 nA, and $I_{D(ON)}$ is ±40 nA, at +125°C with a ±15-V power supply. When the supply voltage is reduced to ±5 V, $I_{S(OFF)}$ and $I_{D(OFF)}$ drop to ±2.5 nA, while $I_{D(ON)}$ is reduced to ±5 nA at +125°C. The supply currents, I_{DD}, I_{SS} and I_L, are 5 µA maximum at +125°C with a ±15-V power supply. When a ±5-V power supply is used, the supply currents are reduced to 1 µA maximum. The on-resistance and timing increase as the power supply is reduced. The Figures below show how the timing and on-resistance of the ADG408 vary as a function of power supply voltage.

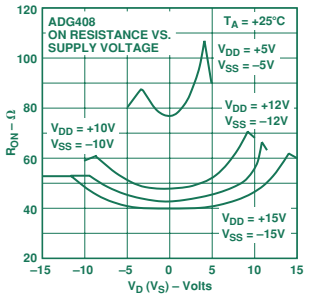

Figure 1. On-Resistance vs Power Supply.

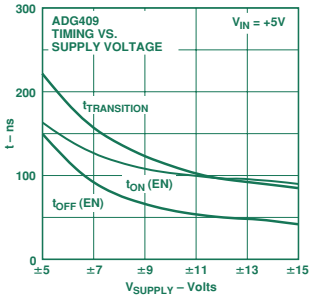

Figure 2. Timing vs Power Supply.

Q. *Some of the ADG series switches are fabricated on the DI process. What is it?*

A. DI is short for dielectric isolation. On the DI process, an insulating layer (trench) is placed between the NMOS and PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in standard switches, are eliminated, resulting in a completely latchup-proof switch. In junction isolation (no trench used), the N and P wells of the PMOS and NMOS transistors form a diode which is reverse-biased in normal operation. However, during overvoltage or power-off conditions, when the analog input exceeds the power supplies, the diode is forward biased, forming a silicon controlled rectifier (SCR)-like circuit with the two transistors, causing the current to be amplified significantly, leading eventually to latch up. This diode doesn't exist in dielectrically isolated switches, making the part latchup proof.

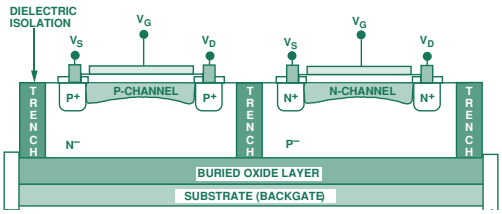

Figure 3. Dielectric Isolation.

Q. *How do the fault-protected multiplexers and channel protectors work?*

A. A channel of a fault-protected multiplexer or channel protector consists of two NMOS and two PMOS transistors. One of the PMOS transistors does not lie in the direct signal path but, is used to connect the source of the second PMOS to its backgate. This has the effect of lowering the threshold voltage, which increases the input signal range for normal operation. The source and backgate of the NMOS devices are connected for the same reason. During normal operation, the fault-protected parts operate as a standard multiplexer. When a fault condition occurs on the input to a channel, this means that the input has exceeded some threshold voltage which is set by the supply rail voltages. The threshold voltages are related to the supply rails as follows: for a positive overvoltage, the threshold voltage is given by $V_{DD} - V_{TN}$ where V_{TN} is the threshold voltage of the NMOS transistor (typically 1.5 V). For a negative overvoltage, the threshold voltage is given by $V_{SS} - V_{TP}$, where V_{TP} is the threshold voltage of the PMOS device (typically 2 V). When the input voltage exceeds these threshold voltages, with no load on the channel, the output of the channel is clamped at the threshold voltage.

Q. *How do the parts operate when an overvoltage exists?*

A. The next two figures show the operating conditions of the signal path transistors during overvoltage conditions. This one demonstrates how the series N, P and N transistors operate when a *positive* overvoltage is applied to the channel. The first NMOS transistor goes into saturation mode as the voltage on its drain exceeds $(V_{DD} - V_{TN})$. The potential at the source of the NMOS device is equal to $(V_{DD} - V_{TN})$. The other MOS devices are in a non-saturated mode of operation.

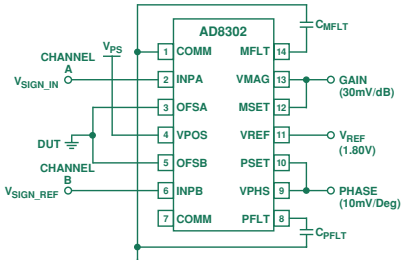

Figure 4. Positive Overvoltage on the Channel.

*Their biographies, and a photo of Mary McCarthy, appear in Analog Dialogue 31-3, page 23.

When a *negative* overvoltage is applied to a channel, the PMOS transistor enters a saturated mode of operation as the drain voltage exceeds ($V_{SS} - V_{TP}$). As with a positive overvoltage, the other MOS devices are non-saturated.

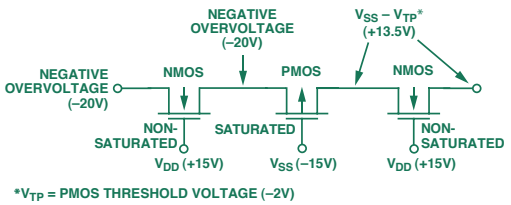

Figure 5. Negative Overvoltage on the Channel.

Q. *How does loading affect the clamping voltage?*

A. When the channel is loaded, the channel output will clamp at a value of voltage between the thresholds. For example, with a load of 1 kΩ, V_{DD} = 15 V, and a positive overvoltage, the output will clamp at $V_{DD} - V_{TN} - \Delta V$, where ΔV is due to the IR voltage drop across the channels of the non-saturated MOS devices. In the example shown below the voltage at the output of the clamped NMOS is 13.5 V. The on-resistance of the two remaining MOS devices is typically 100 Ω. Therefore, the current is 13.5 V/(1 kΩ + 100 Ω) = 12.27 mA. This produces a voltage drop of 1.2 V across the NMOS and PMOS resulting in a clamp voltage of 12.3 V. The current during a fault condition is determined by the load on the output, i.e., V_{CLAMP}/R_L.

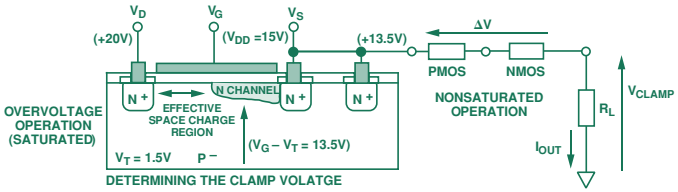

Figure 6. Determining the clamping point.

Q. *Do the fault-protected multiplexers and channel protectors function when the power supply is absent.*

A. Yes. These devices remain functional when the supply rails are down or momentarily disconnected. When V_{DD} and V_{SS} equal 0 V, all the transistors are off, as shown, and the current is limited to sub nanoampere levels.

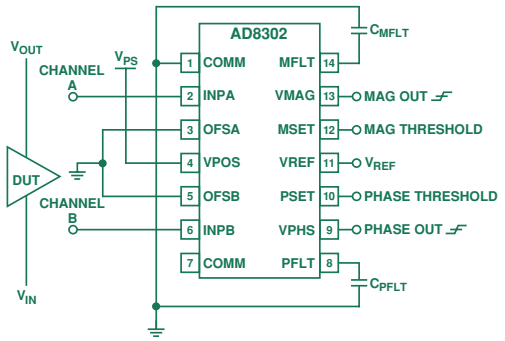

Figure 7. Power Supplies Absent.

Q. *What is "charge injection"?*

A. Charge injection in analog switches and multiplexers is a level change caused by stray capacitance associated with the NMOS and PMOS transistors that make up the analog switch. The Figure below models the structure of an analog switch and the stray capacitance associated with such an implementation. The structure basically consists of an NMOS and PMOS device in parallel. This arrangement produces the familiar "bathtub" resistance profile for bipolar input signals. The equivalent circuit shows the main parasitic capacitances that contribute to the charge injection effect, C_{GDN} (NMOS gate to drain) and C_{GDP} (PMOS gate to drain). The gate-drain capacitance associated with the PMOS device is about twice that of the NMOS device, because for both devices to have the same *on*-resistance, the PMOS device has about twice the area of the NMOS. Hence the associated stray capacitance is approximately twice that of the NMOS device for typical switches found in the marketplace.

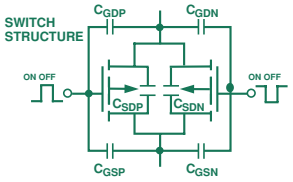

Figure 8

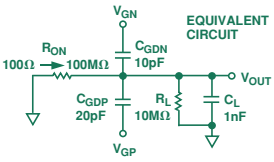

Figure 9

Figure 8. CMOS Switch Structure showing parasitic capacitance.
Figure 9. Equivalent circuit showing the main parasitics which contribute to charge injection.

When the switch is turned on, a positive voltage is applied to the gate of the NMOS and a negative voltage is applied to the gate of the PMOS. Because the stray gate-to-drain capacitances are mismatched, unequal amounts of positive and negative charge are injected onto the drain. The result is a removal of charge from the output of the switch, manifested as a negative-going voltage spike. Because the analog switch is now turned on this negative charge is quickly discharged through the on resistance of the switch (100 Ω). This can be seen in the simulation plot at 5 μs. Then when the switch is turned off, a negative voltage is applied to the gate of the NMOS and a positive voltage is applied to the gate of the PMOS. The result is charge added to the output of the switch. Because the analog switch is now off, the discharge path for this injected positive charge is a high impedance (100 MΩ). The result is that the load capacitance stores this charge until the switch is turned on again. The simulation plot clearly shows this with the voltage on C_L (as a result of charge injection) remaining constant at 170 mV until the switch is again turned on at 25 μs. At this point an equivalent amount of negative charge is injected onto the output, reducing the voltage on C_L to 0 V. At 35 μs the switch is turned on again and the process continues in this cyclic fashion.

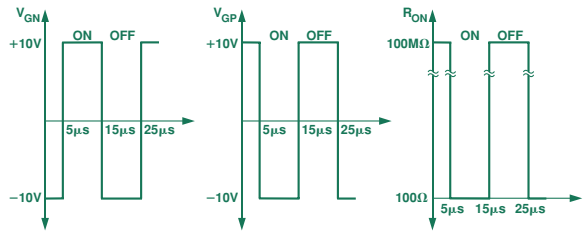

Figure 10. Timing used for simulation in Figure 11.

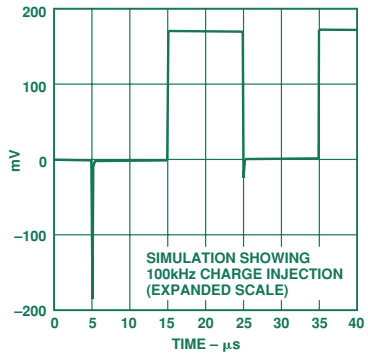

Figure 11. Output of simulation to show the effect of charge injection switching at 100 kHz.

At lower switching frequencies and load resistance, the switch output would contain both positive and negative glitches as the injected charge leaks away before the next switch transition.

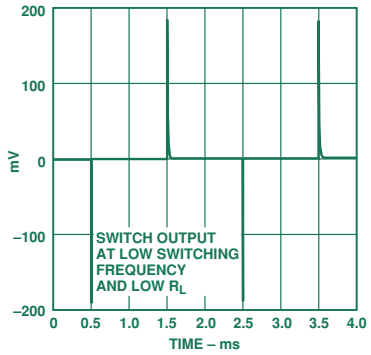

Figure 12. Switch output at low switching frequencies and low resistive loads.

Q. *What can be done to improve the charge injection performance of an analog switch?*

A. As noted above, the charge injection effect is caused by a mismatch in the parasitic gate-to-drain capacitance of the NMOS and PMOS devices. So if these parasitics can be matched there will be little if any charge injection effect. This is precisely what is done in Analog Devices CMOS switches and multiplexers. The matching is accomplished by introducing a dummy capacitor between the gate and drain of the NMOS device.

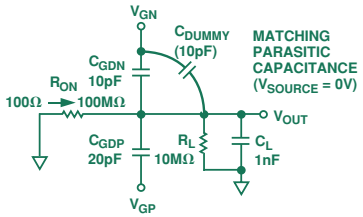

Figure 13. Matching parasitics at V_{SOURCE} = 0 V (ground).

Unfortunately the matching is only accomplished under a specific set of conditions, i.e., when the voltage on the Source of both devices is 0 V. The reason for this is that the parasitic capacitances, C_{GDN} and C_{GDP}, are not constant; they vary with the Source voltage. When the Source voltage of the NMOS and PMOS is varied, their channel depths vary, and with them, C_{GDN} and C_{GDP}. As a consequence of this matching at V_{SOURCE} = 0 V the charge injection effect will be noticeable for other values of V_{SOURCE}.

NOTE: Charge injection is usually specified on the data sheet under these matched conditions, i.e., V_{SOURCE} = 0 V. Under these conditions, the charge injection of most switches is usually quite good in the order of 2 to 3 pC max. However the charge injection will increase for other values of V_{SOURCE}, to an extent depending on the individual switch. Many data sheets will show a graph of charge injection as a function of Source voltage.

Q. *How do I minimize these effects in my application?*

A. The effect of charge injection is a voltage glitch on the output of the switch due to the injection of a fixed amount of charge. The glitch amplitude is a function of the load capacitance on the switch output and also the turn on and turn off times of the switch. The larger the load capacitance, the smaller will be the voltage glitch on the output, i.e., $Q = C \times V$, or $V = Q/C$, and Q is fixed. Naturally, it may not always be possible to increase the load capacitance, because it would reduce the bandwidth of the channel. However, for audio applications, increasing the load capacitance is an effective means of reducing those unwanted "pops" and "clicks".

Choosing a switch with a slow turn on and turn off time is also an effective means of reducing the glitch amplitude on the switch output. The same fixed amount of charge is injected over a longer time period and hence has a longer time period in which to leak away. The result is a wider glitch but much reduced in amplitude. This technique is used quite effectively in some of the audio switch products, such as the SSM-2402/SSM-2412, where the turn on time is designed to be of the order of 10 ms.

Another point worth mentioning is that the charge injection performance is directly related to the *on*-resistance of the switch. In general the lower the R_{ON}, the poorer the charge injection performance. The reason for this is purely due to the associated geometry, because R_{ON} is decreased by increasing the area of the NMOS and PMOS devices, thus increasing C_{GDN} and C_{GDP}. So trading off R_{ON} for reduced charge injection may also be an option in many applications.

Q. *How can I evaluate the charge injection performance of an analog switch or multiplexer?*

A. The most efficient way to evaluate a switch's charge injection performance is to use a setup similar to the one shown below. By turning the switch on and off at a relatively high frequency (>10 kHz) and observing the switch output on an oscilloscope (using a high impedance probe), a trace similar to that shown in Figure 11 will be observed. The amount of charge injected into the load is given by $\Delta V_{OUT} \times C_L$. Where ΔV_{OUT} is the output pulse amplitude.

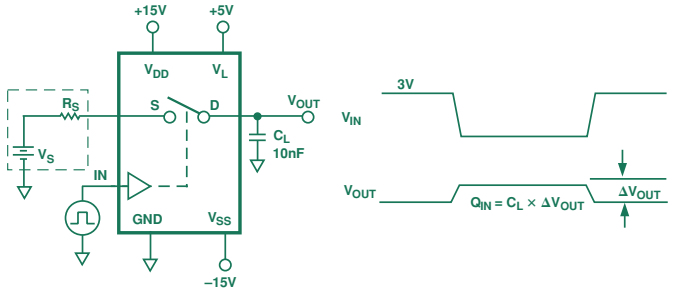

Figure 14. Evaluating the charge injection performance of an analog Switch or Multiplexer.