Bus Switches for Speed, Safety, and Efficiency: What They Are and What You Should Know about Them

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Bus switches—often called *digital switches*—are products designed for connecting to high speed digital buses. Characterized by sub-nanosecond propagation delay and fast switching—and introducing no additional noise or dc power dissipation—they are ideally suited for voltage translation, hot swapping, hot plug, bus or capacitance isolation, and many other applications. In addition, their design makes them useful in many analog applications. The key features that make them suitable for so many different applications include low *on*-resistance, low capacitance, and low propagation delay. This discussion will consider the architecture and characteristics of bus switches—and explain many of their uses.

What is a bus switch?

The basic element of a bus switch is an N-Channel FET whose condition is controlled by CMOS logic. As a *bilateral* switch, either the *source* terminal (A) or the *drain* terminal (B) can be the signal input (Figure 1). When disabled, the gate is held at zero volts and there is an open circuit between the source and the drain.

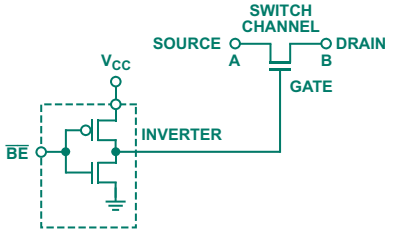

Figure 1. Bus switch channel.

When the switch is enabled ($\overline{BE}$ at 0), its gate is driven to V_{CC}. If V_{GS} (or V_{GD})—i.e., $V_{CC} - V_{IN}$, is greater than the transistor threshold voltage (usually about 1 V) the channel will switch to the low-resistance *on* condition (a few ohms). However, as V_{GS} approaches the threshold voltage, the device approaches its saturation region and becomes highly resistive; Figure 2 shows a typical plot of *on*-resistance versus input voltage as a function of V_{CC} (ADG3257). When in saturation, the output voltage will be limited to $V_{CC} - V_{TH}$.

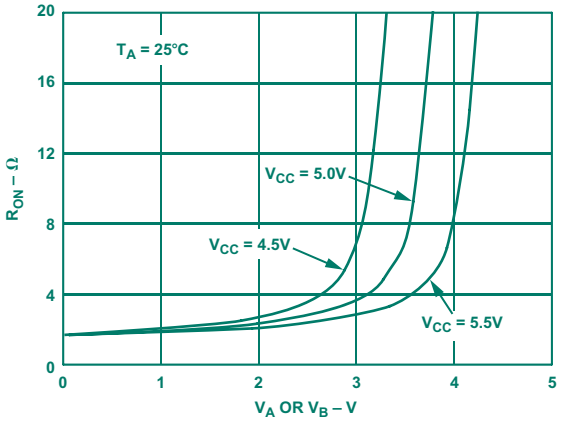

Figure 2. On-resistance of ADG3257 bus switch vs. input voltage (V_A or V_B).

Figure 3 is a plot of output voltage versus input voltage for a typical bus switch with inputs and supply voltages in the 5-V range. When V_{GS} becomes less than about 1 V, the switch channel begins to saturate and the voltage clamps to $V_{CC} - V_{TH}$. So, in this example, for V_{CC} = 5 V, the output follows the input up to about 4 V. Beyond this input voltage, V_{OUT} is held at $V_{CC} - V_{TH}$. This clamping tendency turns out to be a very useful feature of a bus switch; its advantages and use will be discussed in more detail later.

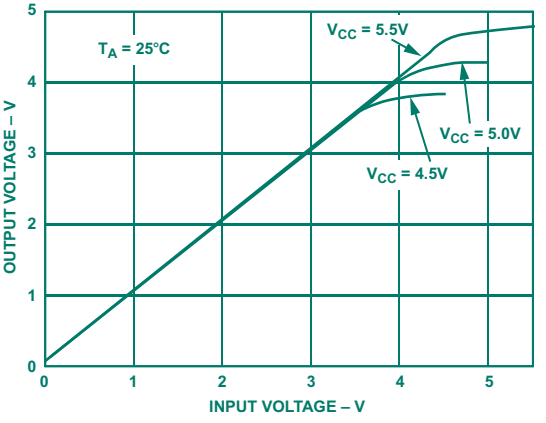

Figure 3. V_{OUT} vs. V_{IN} for the ADG3257 bus switch with V_{CC} in the 5-V range.

Key features affecting applications of bus switch devices are: *on-resistance*, *capacitance* associated with the channel, and *propagation delay. On*-resistance of such devices is usually very low—typically a few ohms. The capacitance, which needs to be kept as low as possible, is typically less than 10 pF in the *on* condition. Both capacitance and *on*-resistance parameters affect the propagation delay through the switch channel.

Practically all of the propagation delay of a bus switch in the *on* condition, driven by a low impedance voltage source, comes from the RC delay of the R_{ON} of the switch and the load capacitance—typically it is in the sub-nanosecond region and is much smaller than the rise/fall times of the driving signals. In a system, propagation delay of the digital switch is determined by the circuit impedance on the driving side of the switch and its interaction with the load on the driven side.

Where would we use a bus switch?

Bus switches are used to increase speed and reduce noise by isolating functions that do not need to drive the bus—or be driven by it—at one moment, but may need to be connected later. Additionally, bus switches can be used in PC *docking stations*, PC-*card* or *power management* applications to break current paths and prevent circuit leakage. By nature, bus switches dissipate very low quiescent power—bus switch members of the ADG324x/ADG325x families, when not switching, typically consume 1 nA (1 μA max)—making them excellent for use in low-power applications such as *notebook* PCs. Bus isolation also makes these devices suitable for *hot swapping* and *hot plugging*, where they can help prevent undesired behavior when additional cards or modules are plugged in. Bus switches are also useful in applications that require systems operating at two different supply voltages to be connected. Each of these applications will be described in more detail below.

Using a digital bus switch for *bus isolation*

A common requirement of bus architectures is low capacitance loading of the bus. Such systems require bus-bridging devices that allow the number of available loads to be increased without exceeding the specs. Ideally, any load on a bus that is not currently in use should be disconnected to reduce overall capacitive loading and avoid exceeding the bus capacitance specification.

Bus switches are designed specifically for this purpose: to isolate functions that do not need to drive or be driven at this moment but may need to be connected later, thus minimizing the total capacitive load connected at any given moment.

If a bus switch is placed between each load on the bus and the bus itself, then the load is isolated from the bus when the switch is disabled. Because the bus switch can pass significant amounts of current *in either direction* when enabled, without adding significant propagation delay for signals that pass through it, it is a viable solution to the bus isolation problem. Figure 4 shows a generalized situation, and Figure 5 shows a specific solution to a memory bank drive problem with a quad 2:1-multiplexer bus switch.

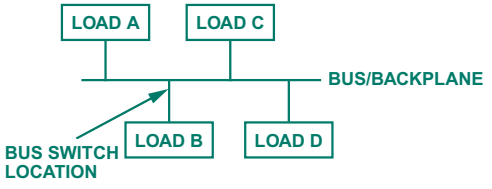

Figure 4. A bus switch can isolate Load B from the rest of the bus.

Multiplexing

Problems faced by a designer of a system with a large number of common bus signals include noise in the system due to simultaneous switching of the address and data bus signals—and large delays in the system caused by capacitive loading of the bus.

Figure 5a shows an array of memory banks in which each address and data signal is loaded by the sum of the individual loads. Now, if a bus switch is used (the ADG3257 quad 2:1 multiplexer/demultiplexer in this example) as shown in Figure 5b, then the output load on the memory address and data bits is halved. This isolation can provide a near-doubling of the speed at which the selected bank's data can flow, because the capacitance loading is halved and the switches introduce negligible propagation delay. Bus noise is also markedly reduced.

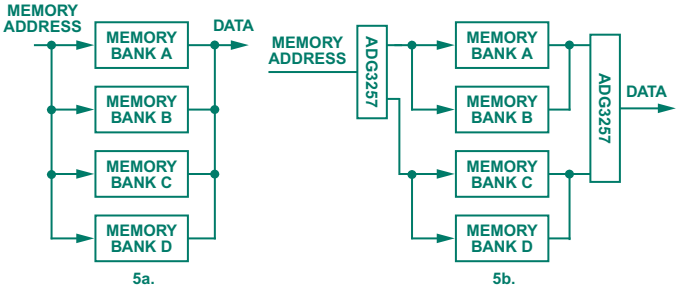

Figure 5. Reducing memory bank loading.

a. The address and data lines are heavily loaded when all memory banks are permanently connected to the bus.
b. When the ADG3257 is used to switch between different memory bank pairs, access time and noise are both reduced.

Voltage-level translation

When interfacing between two devices operating at different supply voltages, digital signals coming from the higher voltage device need to be safely interfaced to the lower voltage device. In order not to exceed *maximum* ratings specified for the device operating at the lower voltage level, the voltage output coming from the higher voltage device must be reduced. This can be readily accomplished by inserting a bus switch in series with the signal in question (Figure 6).

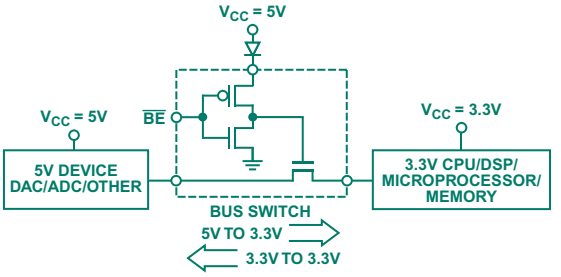

Figure 6. Using the ADG3257 to switch and level translate between a 3.3-V controller and 5-V data converter.

As discussed above, if the V_{GS} voltage is reduced to less than 1 V, the switch channel begins to saturate and the output voltage clamps to $V_{CC} - V_{TH}$. That is, the output follows the input up to the vicinity of this voltage and, for higher input voltages, V_{OUT} is held at $V_{CC} - V_{TH}$. Figure 7 shows an output-input plot of the same switch as in Figure 3, but focused on V_{CC} in the 3.3-V region. This behavior makes bus switch devices suitable for interfacing applications calling for level translation.

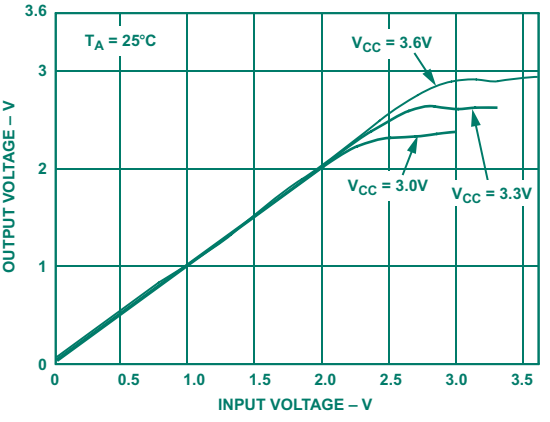

Figure 7. V_{OUT} vs. V_{IN} for the ADG3257 bus switch with V_{CC} in the 3-V range.

In the example of Figure 6, the user may wish to apply a 3.3-V DSP or microcontroller as a control device in an application for which reasonable analog performance requires that the ADC or DAC or other device operate from, say, a 5-V supply. Unless the microcontroller has inputs that can tolerate the 5-V device's output levels, the circuits will not be able to communicate properly. With the bus switch of Figures 3 and 7 connected between the devices, as a voltage translator, bidirectional communication is possible without risk of damaging the lower-supply device. The combination of the diode, connected in series with the 5-V supply, and the bus switch's clamp voltage provides a drop fairly close to the required 5-V-to-3.3-V (left to right) without impeding 3.3-V communication (right to left).

Similarly, the device could be used to level-translate between 3.3-V and 2.5-V systems. A LVTTL VOH level for a 2.5-V output is 2 V, while the LVTTL VIH level required by the 2.5-V device is 1.7 V, so a 5-V bus switch operating at a lower supply voltage can easily meet these requirements.

Because a bus switch is a simple FET, the signal path is bidirectional; i.e., the inputs and outputs are interchangeable. However, *information* cannot always be communicated bidirectionally; it is dependent on supply. Table 1 shows that translations between 5 V↔3.3 V and 3.3 V↔2.5 V may be used to communicate bidirectionally between devices operating from different supplies, but the other two options (2.5V→1.8V, 3.3V→1.8V) cannot be employed for both directions. For further details, see the ADG3247 data sheet.

Table 1. Bus Switch Devices and Their Level-Translation Capabilities.

Part No.	Function	Level Translation			
		5↔3.3	3.3↔2.5	2.5→1.8	3.3→1.8[1]
ADG3245	8-Bit Bus Switch	X	✓	✓	✓
ADG3246	10-Bit Bus Switch	X	✓	✓	✓
ADG3247	16-(2x8) Bit Bus Switch	X	✓	✓	✓
ADG3257	Quad 2-1 (4 Bit, 1 of 2)	✓[2]	✓	X	X

[1]SEL pin tied to logic low. For more information on SEL pin, see ADG3245/6/7 data sheets.

[2]Requires external diode.

As explained earlier, the threshold voltage, V_{TH}, is approximately 1 V, so with 2.5-V supply, the maximum output of the bus switch will be 1.5 V, which is insufficient to meet the 1.7-V V_{IH} input requirement of a 2.5-V device (Figure 8). Similarly, when translating between 3.3 V and 1.8 V, the maximum output of the bus switch will be 1.5 V, so again the voltage level is not sufficiently high for a 3.3-V device to recognize it as *logic high*. Therefore, the signal path can be relied on only for unidirectional communication in these cases.

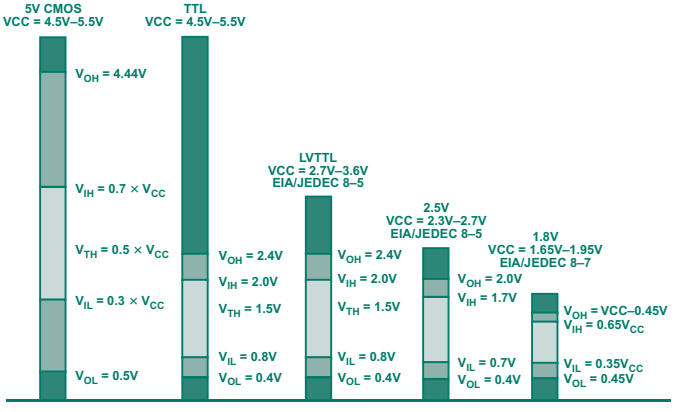

Figure 8. Logic levels compared for different supply voltages.

How many "bits"?

In the terminology of bus switches, *bits* refers to the number of channels associated with the device. For example, a 16-bit device (ADG3247) has 16 individual channels. Bus switches can be made available in a variety of bit widths. Current offerings are 8-, 10-, 16-bit and quad 2-1 (4-bit, 2-port) devices (ADG3245, ADG3246, ADG3247, ADG3257, respectively), with more in the offing.

Can a bus switch be used to switch analog signals?

A bus switch channel is a simple N-channel *field-effect transistor* (FET); standard analog switch designs include a P channel in parallel in order to make rail-to-rail analog switching possible. The design of the bus switch provides lower *on*-resistance, smaller *on* and *off* channel capacitance, and thus improved frequency performance, compared to its analog counterpart. Smaller associated capacitances benefit device performance by reducing charge injection (Figure 9) to significantly lower values than are found in the standard analog switch.

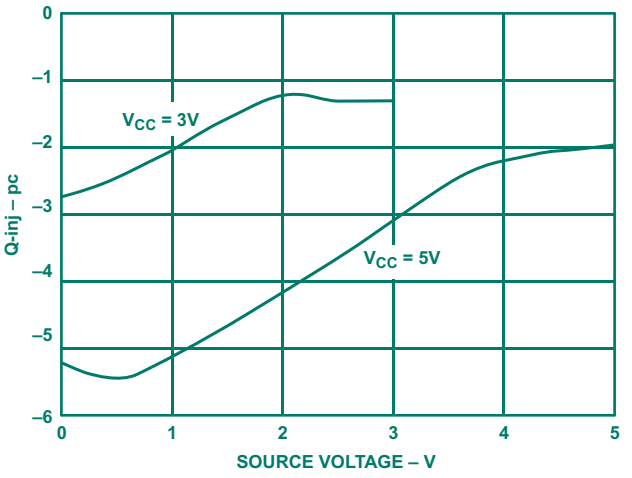

Figure 9. Charge injection for a typical bus switch (ADG3257).

Thus, bus switches need not be confined to bus switching applications or used solely for switching digital signals. They can also find many uses in switching analog signals, within the limitations of $V_{CC} - V_{TH}$ (which, in many cases, is not an important issue).

How are bus switches useful in hot swap applications?

Hot swapping is adding and/or removing plug-in circuitry in a system with the power *on*. Examples of applications that require the ability to hot swap are docking stations for laptops and line cards for telecommunications switches. During a hot swap event, the connectors on the back plane are "live"; the add-on card must be able to cope with this condition. If the bus can be isolated prior to insertion, one has more control over the hot-swap event. Isolation can be achieved using a digital switch, ideally positioned on the add-on card between the connector and the device (Figure 10). However, it is important that the ground pin of the add-on card must connect to the ground pin of the back plane before any other signal or power pins, and it must be the last to disconnect when a card is removed.

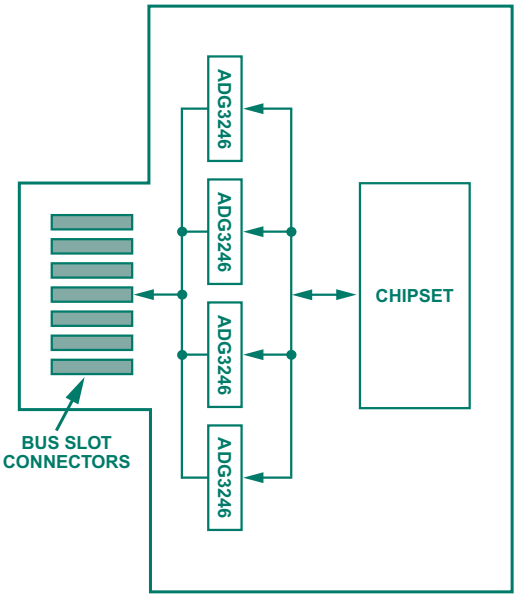

Figure 10. Hot swapping with the ADG3246 bus switch.

And how about hot plug?

Critical systems, such as ADSL (Asynchronous Digital Subscriber Line), manufacturing controls, servers, and airline reservations must not be shut down. If new hardware, such as a plug-in modem, needs to be added to the system, it has to be done while the system is up and running. This process of adding hardware during mandatory continuous operation is known as *hot plug*. To ensure smooth execution of the process, a digital switch can be wired between the connector and the internal bus (Figure 11). During the hot-plug event, the switch is turned off to provide isolation of the specific circuit location.

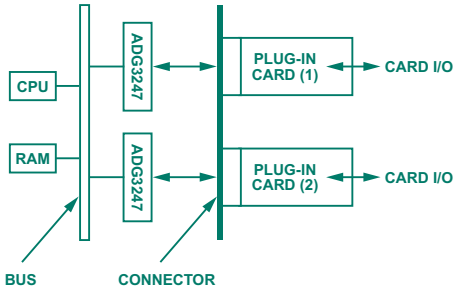

Figure 11. Using the ADG3247 in a hot-plug application.

The benefits of a flow-through pinout architecture

A useful feature of many of these digital switches from Analog Devices is the logical "flow-through" pin arrangement, in which each input and its corresponding output are on opposite sides of the chip without crossovers or interruptions of the pattern (Figure 12). This makes routing of the input and output signals much easier to deal with in printed circuit board layouts. In addition, propagation delays can be more readily matched with a flow-through pin arrangement.

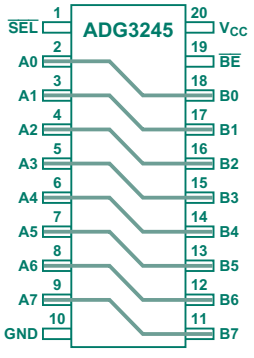

Figure 12. Flow-through pin arrangement.

CONCLUSION

Bus switch devices are extremely versatile; they may be used in many different applications in today's high performance systems. In this brief introduction, we have shown how bus switches are utilized in areas such as bus isolation, voltage translation, analog signal switching, and hot-insertion applications. We have also made it evident that they are suitable for many other applications. We have introduced key specifications of bus switches, discussed their operation, and sought to answer some frequently asked questions about them.

ACKNOWLEDGEMENTS

We wish to thank the Bus Switch Team of Analog Devices for their valuable contributions.

REFERENCES

ADG3245, ADG3246, ADG3247, and ADG3257 data sheets

EIA/JEDEC for power supply voltages and interface standards

Compact PCI Hot Swap Specification R1.0

PCI Hot-Plug Specification R1.0

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