Program analyzes all-resistive dc circuits

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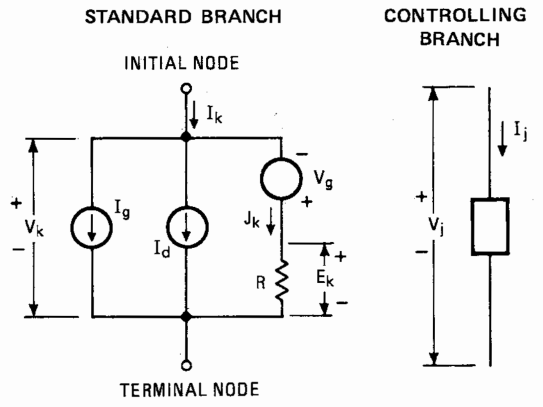
Networks that are strictly resistive can be analyzed easily and quickly for dc conditions with a brief but effective computer program written in Basic. The circuit to be analyzed can also contain active devices, provided those devices can be represented by only resistive elements and voltage-dependent sources.

The standard circuit branch allowed by the program is shown in Fig. 1, along with the program listing. Nodes may be numbered in any order with consecutive integers beginning with zero. (The program always assumes that node 0 is the reference node.) Branches may also be numbered in any order with consecutive integers, but this set of numbers must begin with the number one.

The program first asks to know the number of nodes minus one, and then it requests the number of branches. (A question mark is typed after each request.) The user responds by typing in the data requested each time, and pressing the RETURN key on his terminal.

After this preliminary input data is obtained, the program asks for the branch data by typing a question mark each time for each branch. In response, the user types in the data for each branch in a specific order and



V_k, V_j = BRANCH VOLTAGES
I_k, I_j = BRANCH CURRENTS
E_k = ELEMENT VOLTAGE
J_k = ELEMENT CURRENT
V_g, I_g = INDEPENDENT SOURCES
$I_d = g_m \cdot V_j$ (VOLTAGE-CONTROLLED CURRENT SOURCE)

1. Dc circuit analysis. Computer program, which is written in Basic, is useful for a speedy dc analysis of small resistive networks. The definitions for a standard circuit branch and the program listing itself are given here. Dependent sources must be voltage-controlled.

```
100  DIM A[7,15],Y[15,15],E[15],I[15],
     J[15],V[15],S[15],W[15,7],U[15,7]
110  PRINT "NUMBER OF NODES - 1 =";
111  INPUT N
120  PRINT "NUMBER OF BRANCHES =";
121  INPUT B
130  MAT A=ZER[N,B]
140  MAT Y=ZER[B,B]
150  MAT E=ZER[B]
160  MAT I=ZER[B]
170  FOR K=1 TO B
180  INPUT B1,F1,T1,R,E[B1],I[B1],Y1,C1
190  IF F1=0 THEN 210
200  LET A[F1,B1]=1
210  IF T1=0 THEN 230
220  LET A[T1,B1]=-1
230  LET Y[B1,B1]=1/R
240  IF C1=0 THEN 260
250  LET Y[B1,C1]=Y1
260  NEXT K
270  MAT S=ZER[B]
275  MAT J=ZER[B]
280  FOR K=1 TO B
281  LET S[K]=Y[K,K]*E[K]
282  NEXT K
290  MAT S=I+S
295  MAT S=J-S
300  MAT W=ZER[B,N]
310  MAT W=TRN(A)
320  MAT U=ZER[B,N]
330  MAT U=Y*W
340  MAT V=ZER[N,N]
350  MAT W=A*U
360  MAT U=ZER[N,N]
370  MAT U=INV(W)
380  MAT V=ZER[N]
390  MAT V=A*S
400  MAT J=ZER[N]
410  MAT J=U*V
420  PRINT
430  PRINT "NODE"," VOLTAGE"
440  FOR K=1 TO N
450  PRINT K,J[K]
460  NEXT K
470  MAT V=ZER[B]
480  MAT W=ZER[B,N]
490  MAT W=TRN(A)
500  MAT V=W*J
510  MAT J=ZER[B]
520  MAT J=Y*V
530  MAT J=J-S
540  PRINT
550  PRINT "BRANCH"," VOLTAGE"," CURRENT"," POWER"
560  FOR K=1 TO B
570  PRINT K,V[K],J[K],V[K]*J[K]
580  NEXT K
590  MAT V=V+E
600  PRINT
610  PRINT "ELEMENT"," VOLTAGE"," CURRENT"," POWER"
620  FOR K=1 TO B
630  LET J[K]=Y[K,K]*V[K]
640  PRINT K,V[K],J[K],V[K]*J[K]
650  NEXT K
660  END
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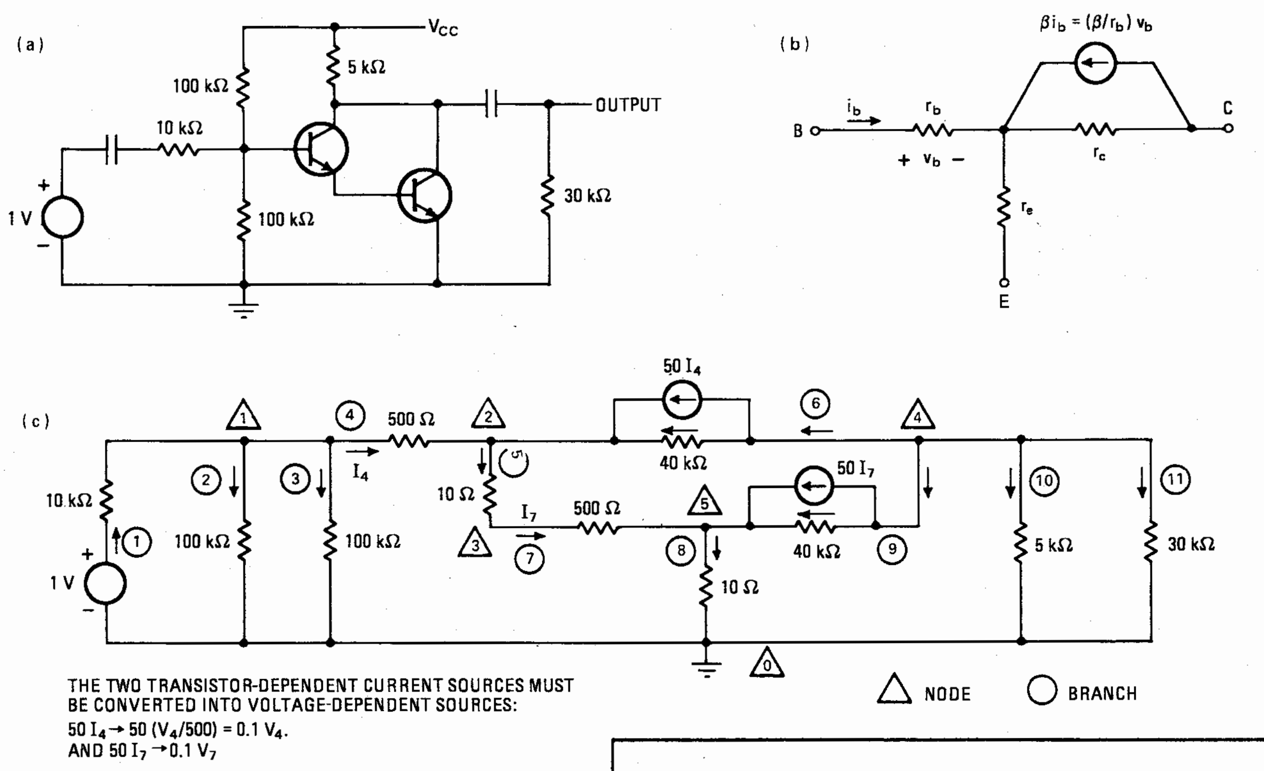

(d)

```
FEADY
RUN
NUMBER OF NODES - 1 =?5
NUMBER OF BRANCHES =?11
?1,Ø,1,10000,1,0,0,0
?2,1,Ø,100000,0,0,Ø,0
?3,1,Ø,100000,0,0,0,Ø
?4,1,2,500,Ø,Ø,0,Ø
?5,2,3,10,Ø,Ø,Ø,Ø
?6,4,2,40000,0,0,0.1,4
?7,3,5,500,0,0,0,0
?8,5,Ø,10,0,0,0,0
?9,4,5,40000,0,0,Ø.1,7
?10,4,Ø,5000,0,0,0,Ø
?11,4,0,30000,Ø,Ø,Ø,0

NODE          VOLTAGE
 1            .428572
 2            .4Ø4286
 3            .4ØØ121
 4           -82.Ø2Ø3
 5            .191866

BRANCH        VOLTAGE        CURRENT         POWER
 1           -.428572        5.71428E-Ø5    -2.44898E-Ø5
 2            .428572        4.28572E-Ø6     1.83674E-Ø6
 3            .428572        4.28572E-Ø6     1.83674E-Ø6
 4            2.42857E-Ø2    4.85713E-Ø5     1.17959E-Ø6
 5            4.165Ø5E-Ø3    4.165Ø5E-Ø4     1.73477E-Ø6
 6           -82.4246        3.67952E-Ø4    -3.Ø3283E-Ø2
 7            .2Ø8255        4.165Ø9E-Ø4     8.67399E-Ø5
 8            .191866        1.91866E-Ø2     3.68127E-Ø3
 9           -82.2122        1.877Ø1E-Ø2    -1.54314
 1Ø          -82.Ø2Ø3       -1.64Ø41E-Ø2     1.34547
 11          -82.Ø2Ø3       -2.734Ø1E-Ø3     .224245

ELEMENT       VOLTAGE        CURRENT         POWER
 1            .571428        5.71428E-Ø5     3.2653ØE-Ø5
 2            .428572        4.28572E-Ø6     1.83674E-Ø6
 3            .428572        4.28572E-Ø6     1.83674E-Ø6
 4            2.42857E-Ø2    4.85713E-Ø5     1.17959E-Ø6
 5            4.165Ø5E-Ø3    4.165Ø5E-Ø4     1.73477E-Ø6
 6           -82.4246       -2.Ø6Ø62E-Ø3     .169845
 7            .2Ø8255        4.165Ø9E-Ø4     8.67399E-Ø5
 8            .191866        1.91866E-Ø2     3.68127E-Ø3
 9           -82.2122       -2.Ø5531E-Ø3     .168971
 1Ø          -82.Ø2Ø3       -1.64Ø41E-Ø2     1.34547
 11          -82.Ø2Ø3       -2.734Ø1E-Ø3     .224245

READY
```

2. Program at work. The transistor amplifier in (a) is analyzed for dc conditions. The T-model equivalent circuit (b) can be used for the transistors, provided that all dependent current sources are converted into voltage-dependent sources. In the complete amplifier equivalent circuit (c), all nodes and branches are numbered consecutively. The program printout is shown in (d).

on the same line. He gives the branch number, the initial node number, the terminal node number, the resistance value, the value of the independent voltage source, the value of the independent current source, the transconductance of the dependent current source, and the number of the branch that is controlling the dependent current source, finally pressing the RETURN key.

The polarity signs allotted to the voltage and current sources must agree with the sign conventions defined by the standard branch of Fig. 1. The various data inputs must be separated by commas.

Once the program has all of the input data, it will compute the circuit's output node voltages, as well as all the branch and element voltages, currents, and power. The element of a branch is the resistance of that branch. When there is no current source associated with a branch, the branch current is the same as the element current. And when a branch does not have a voltage source, branch and element voltages are the same.

Figure 2 shows an example analysis of a two-transistor amplifier (Fig. 2a). The simple T-model equivalent circuit (Fig. 2b) is used to represent each transistor. In the complete amplifier equivalent circuit (Fig. 2c), the node numbers are enclosed by triangles, and the branch numbers are encircled. The program printout (Fig. 2d) conveniently tabulates the input data, the output node voltages, the branch data, and then the element data.

On a 16-bit minicomputer with an 8,000-word memory, the program can handle a circuit having up to seven nodes and 15 branches. If a machine with more storage capacity is used, the dimensions of the arrays set up by statement 100 in the program listing can be increased to accommodate larger circuits. □

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