Probing system lets you test digital ICs

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This Design Idea describes a simple yet powerful handheld probe that you can use as both a logic probe and a pulse generator either individually or simultaneously. This feature makes the probe useful for testing DIP digital ICs, such as gates, flip-flops, and counters, using a socketed fixture with three-post jumpers to connect each pin to logic high or logic low or to 5V or ground.

Three pushbutton switches, two dual-color LEDs, and two probe tips are built into a plastic cylinder, such as an empty, 20g or larger glue-stick tube. The generator's probe tip hooks to fit onto the test fixture's jumper pins and mounts onto a spring—such as those in retractable ball-point pens—for flexibility, and it allows the logic-probe tip to move to the output under test. Two of the pushbutton switches set the generator's quiescent state for a high or low output. The third switch briefly single-pulses the output to the opposite state. If the switch is pressed for longer than 2 seconds, the output produces a pulse train.

IC_{1A}, an NE556, is a 2-sec monostable circuit, which triggers a 1-msec-pulse generator circuit employing gate G_1, resistor R_1, and capacitor C_1 (**Figure 1a**). G_4 buffers the circuit. The output of the monostable circuit also passes through G_2 and G_3 to mask the output of the astable component, IC_{1B}, an NE556 that provides the pulse train. To prevent any spurious pulse from reaching output Probe A when switch S_1 is not depressed, keep IC_{1B} deactivated by applying a low voltage to its reset pin 4 through transistor Q_1, whose biasing is further guarded by a 0.68-µF capacitor.

When you press switch S_1 for a short

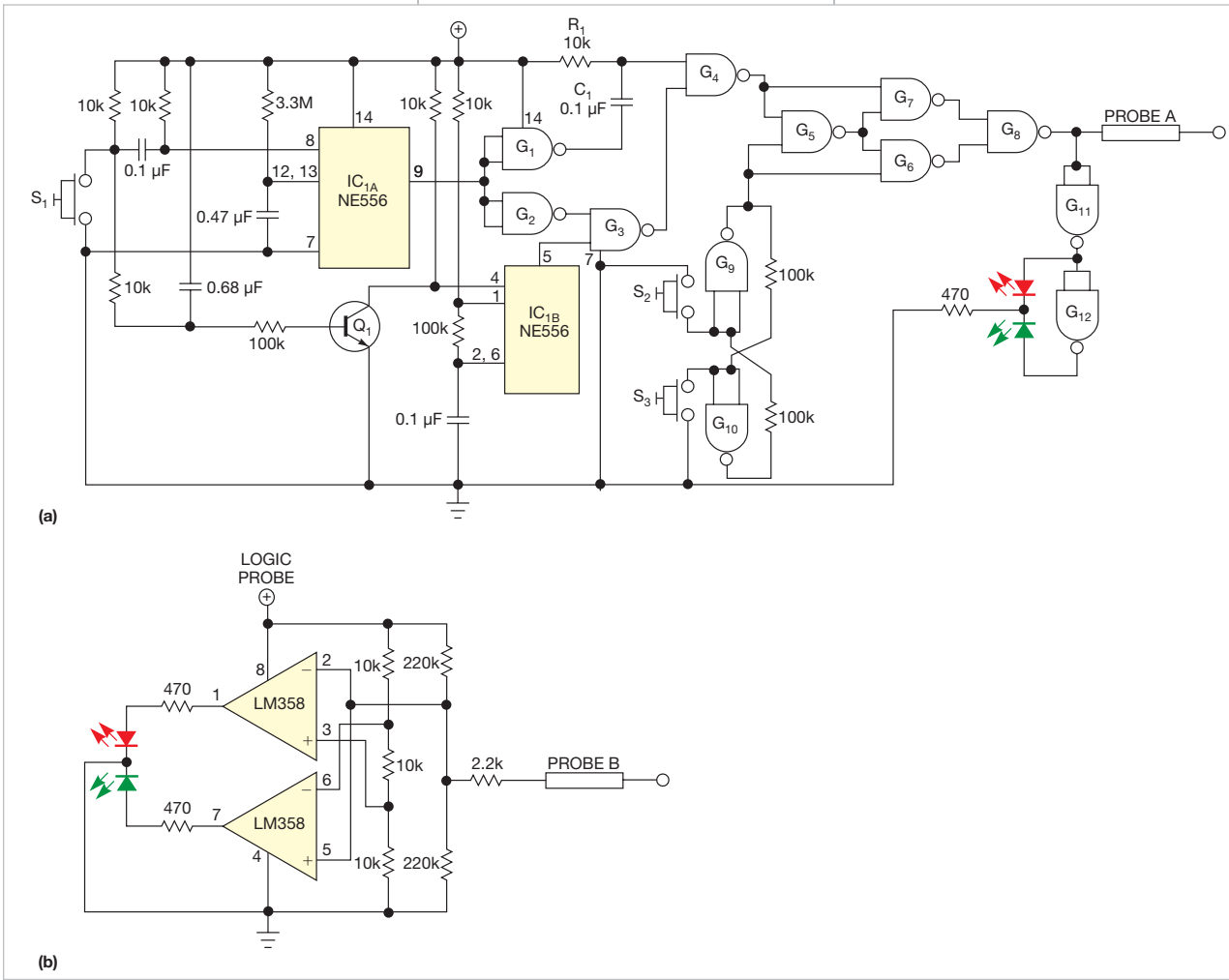

Figure 1 This circuit combines analog and digital functions. Probe A is the pulse-generator probe, and Probe B is the logic probe (a). Although not shown, a 100-µF capacitor should be connected between the supply and ground. Red LEDs indicate logic zero, and green LEDs display logic one (b).

time, IC_{1A} fires and produces a high output for approximately 2 sec. The 1-msec pulse from G_1, R_1, C_1, and G_4 reaches the pulse Probe A through the XOR function comprising G_5 through G_8, and the output of the astable IC_{1B} is masked at G_3 from reaching the XOR. If you depress switch S_1 for longer than 2 sec, the monostable IC_{1A} times out. This action unmasks G_3 and allows the 70-Hz oscillation from IC_{1B} to reach the XOR.

G_9 and G_{10} form a bistable circuit, which "remembers" the most recently pressed S_2 or S_3 switch and controls the inverting and noninverting operation of the XOR function. G_{11} and G_{12} together drive the dual-color LED to indicate the pulse generator's polarity. Red indicates that Probe A's output is mainly logic zero, with the single 1-msec pulse a logic high. Green indicates the opposite.

The LM358 acts as a window-detector logic probe (**Figure 1b**). With the values in the **figure**, the red LED lights at Probe B voltages of less than 35% of the supply voltage, and the green LED lights at voltages greater than 65% of the supply voltage. Neither LED lights between these voltages. You may wish to adjust the resistor network to reduce the lower threshold to include the transistor-transistor-logic zero of less than 0.8V.

If you use CD4011 quad NAND gates, you can externally power the probe at 4.5 to 15V. Using a CD4093 Schmitt-trigger quad NAND for G_1 through G_4 ensures no spurious oscillations as a result of the slow voltage rise at timing capacitor C_1. If your design requires a higher-current generator drive, you can add a pair of NPN and PNP boost transistors to the output.

Figure 2 shows a jig for testing the digital ICs. Configure the 16-pin DIP socket for the device under test with an array of triple-post headers and push-on jumpers. You can connect any pin directly or through a resistor to power or ground to configure power or logic levels. The resistors can be any suitable value; approximately 2 kΩ is appropriate.

To set a TTL low, the pin must connect directly to ground. To inject a signal, hook the flexible spring-mounted generator, Probe A (**Figure 3**), onto the appropriate input post and move logic Probe B to the corresponding output post or pin. See a suggested perf-board layout at www.edn.com/4374947.EDN

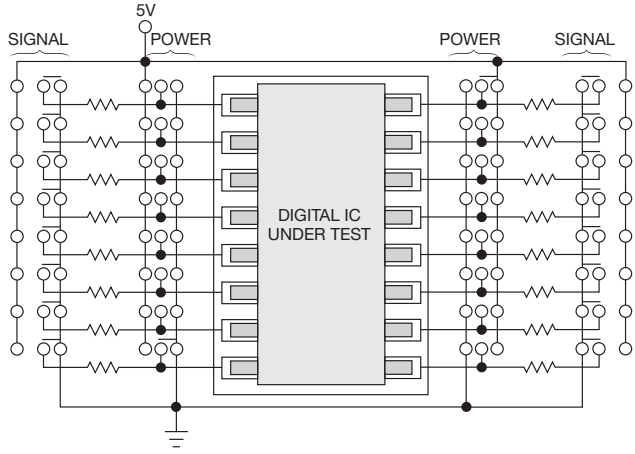

Figure 2 Program this test jig with header posts and jumpers for the IC under test.

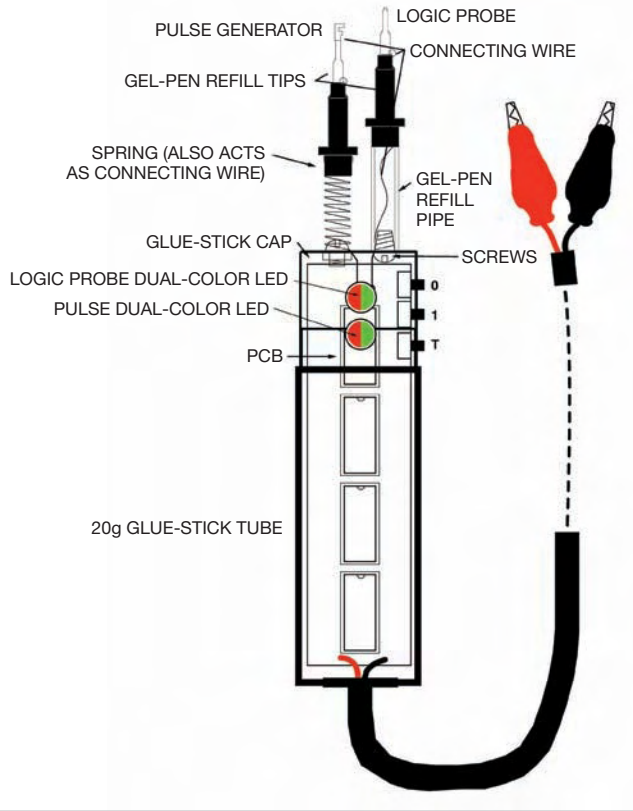

Figure 3 To inject a signal, hook the flexible spring-mounted generator, Probe A, onto the appropriate input post and then move logic Probe B to the corresponding output post or pin.

REFERENCES

1 Baddi, Raju, "Logic probe uses six transistors," *EDN*, Dec 15, 2010, pg 46, http://bit.ly/n24oau.

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