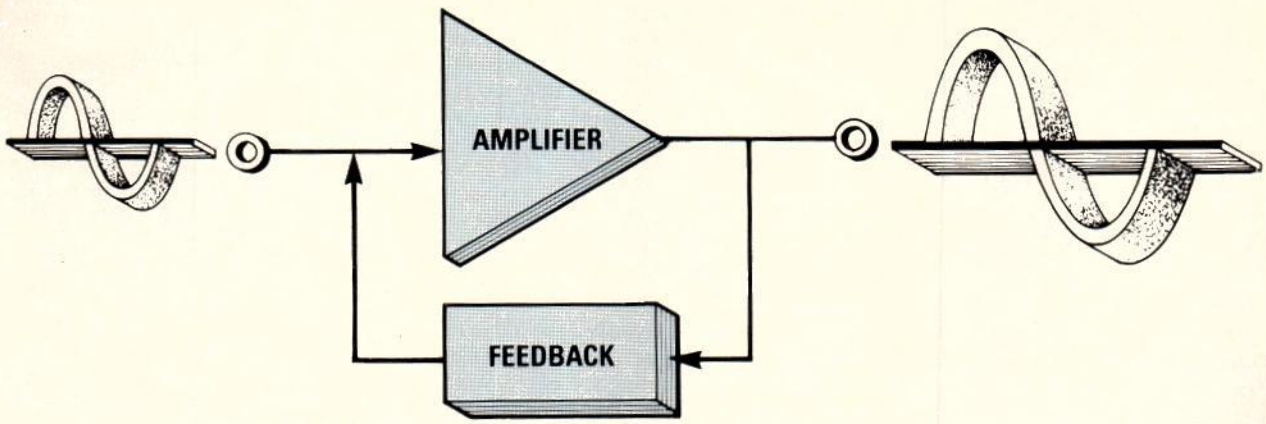
How to Design OSCILLATOR Circuits



JOSEPH J. CARR

Our oscillator series concludes with a discussion of CMOS oscillators.

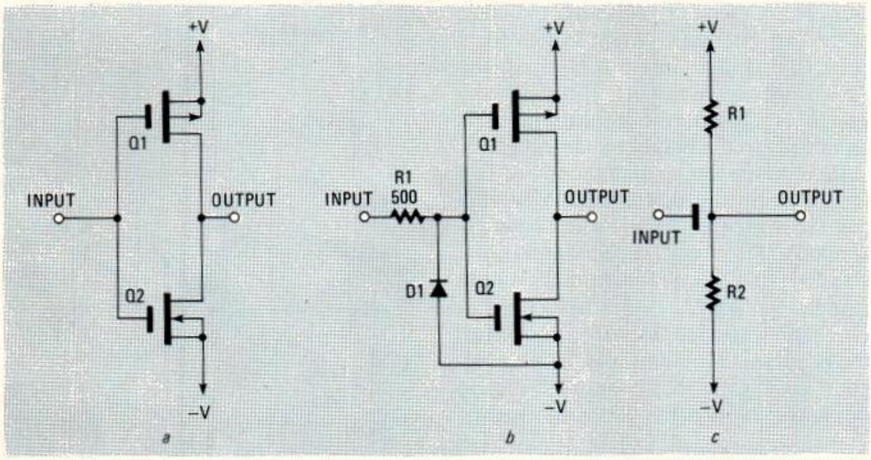


FIG. 1—TYPICAL A-SERIES CMOS INVERTER uses complementary MOSFET transistors (*a*); the B-series adds diode and resistor input protection (*b*). The equivalent circuit may be thought of as two gated resistors (*c*).

Part 7

FOR OUR FINAL INSTALLMENT, we'll discuss the digital CMOS oscillator. Like its TTL counterpart, the CMOS oscillator is often used as a clock in digital circuits. There are several significant differences between TTL and CMOS devices, however.

Perhaps the biggest difference is that CMOS devices are made from *M*etal *O*xide *S*emiconductor *F*ield *E*ffect *T*ransistors (MOSFET's) rather than the the bipolar types used in TTL devices. MOSFET's draw considerably less current than TTL devices (microamperes rather than milliamperes). However, a standard CMOS device has a lower maximum operating frequency than a functionally equivalent TTL device.

Figure 1-*a* shows the CMOS inverter that is the basis of many gates and larger logic elements. The inverter shown there consists of a pair of MOSFET transistors; that type of inverter is the core of the older A-series CMOS devices.

Transistor Q1 is a p-channel MOSFET, and Q2 is an n-channel MOSFET. Those devices operate as follows: A high applied to the common input terminal causes Q2 to turn on and Q1 to turn off. Therefore, the output is low. Likewise, a low input causes Q1 to turn on and Q2 to turn off, so the output is high.

The newer B-series type of CMOS gate is shown in Fig. 1-*b*. It contains several components that protect the device from *E*lectro*S*tatic *D*ischarge (ESD). A-series devices have a gate breakdown voltage of less than 100 volts. Since static build-up on clothing and tools can reach several kilovolts easily, you can damage an A-series CMOS device just by touching it. The resistor (R1) and the diode (D1) in a B-series gate protect against damage by ESD.

There are other differences between A- and B-series CMOS devices. The B series offers faster rise and fall times, and they will drive larger loads than most A-series counterparts. And, although there may be some applications where the characteristics of the A-series are advantageous, in general the B-series device is preferred.

The first CMOS devices had part numbers in the 4000 series. Later, designers wanted pin-compatible substitutes for 74-series TTL devices, so the 74C series came into being. However, although the pinouts of 74 and 74C devices are identical, the electrical characteristics of TTL and CMOS are very different. So, for example, you can't plug a 74C04 package into a circuit designed for use with a 7404. However, a new series of CMOS devices, the 74HCT series, is plug-compatible with LS-type TTL devices.

CMOS devices operate from two power supplies, +V and −V. The difference between the two must generally be less than 18 volts. For example, +12 volts and −6 volts, or ±9 volts, etc. Of course, +V is often set at +5 volts and −V at 0 volts (i. e., ground). The operating characteristics of CMOS devices vary with supply voltage; for that reason, manufacturers often specify operating characteristics at 5, 10, and 15 volts.

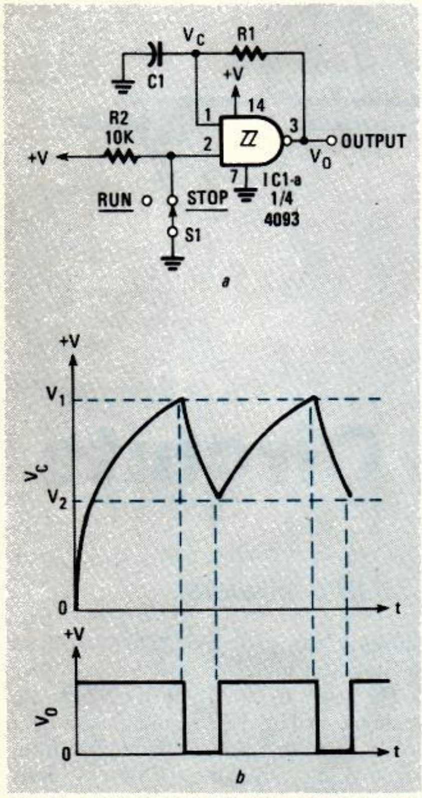


FIG. 2—AN ASTABLE MULTIVIBRATOR may be built from a 4093 Schmitt trigger (*a*); the circuit's timing is shown in *b*.

Circuit model

The transistors in the CMOS device can be modeled as gated resistors, as shown in Fig. 1-*c*. In that circuit the channel resistance of the n-channel device is represented by R1, and the channel resistance of the p-channel device is represented by R2. The output is at the junction of the two resistances.

Let's look at what happens when a signal is applied to the circuit. Assume that +V is 5.0 and that −V is 0.0 volts. When the input is low, the output is high. In that case, resistor R1 has a low value (less than 2K) and R2 has a high value (1 megohm). But when the input is high, the resistances reverse: R1 has high resistance and R2 has low resistance, so the output is effectively at ground.

CMOS current drain is so low because, whenever the circuit is in a stable state (high or low), the output circuit is effectively composed of a high resistance in series with a low resistance. The only time that both resistances are moderately low is when the output is in transition from high to low or from low to high.

Practical circuits

Our first CMOS clock circuit is shown in Fig. 2-*a*; its timing diagram is shown in Fig. 2-*b*. The gate used in that circuit is one gate of a 4093 quad NAND Schmitt trigger. A Schmitt trigger is a special device that changes state only on specific input voltages. Assuming use of a 5-volt power supply, the inputs are affected only by positive-going signals that surpass 2.9 volts, and by negative-going signals that go below 2.3 volts. The *hysteresis* provided thereby allows you to obtain a squarewave output from a slowly changing input signal.

The gate we use has two inputs, so we could tie both together, effectively forming an inverter, or we could use one input as a control element. We chose the latter in the Fig. 2 circuit. When switch S1 is open, the control input is high, so the device operates normally. But when the switch is closed, the control input is grounded, so the output remains high.

Refer to the timing diagram in Fig. 2-*b* for the following discussion. Assuming that the switch is closed, when power is applied to the circuit, capacitor C1 is discharged, so V_C is 0. Therefore the output is high. Voltage V_C begins to increase as C1 charges through R1. When V_C passes the positive-going threshold V_1, the output goes low. At that point C1 begins to discharge through R1. When the voltage decreases to V_2, the output again snaps high, and the cycle repeats.

A CMOS oscillator built from a pair of inverters is shown in Fig. 3. The operating frequency of the circuit is approximately:

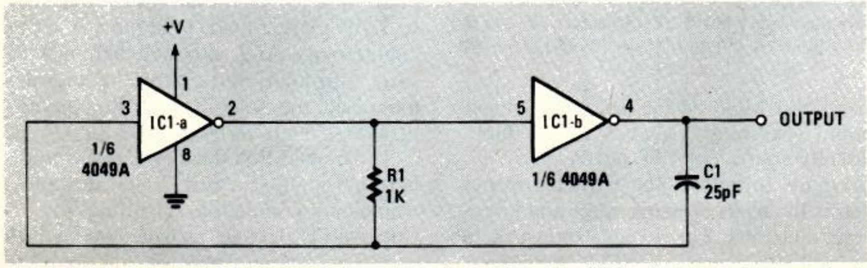


FIG. 3—A PAIR OF CMOS INVERTERS form a simple oscillator. Oscillating frequency is approximately 1/(2.2 · R1 · C1).

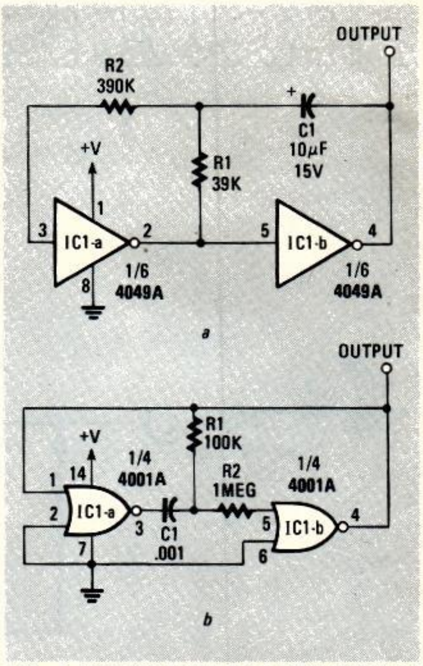


FIG. 4—IMPROVE OUTPUT SYMMETRY by adding an isolation resistor (R2 in both *a* and *a*).

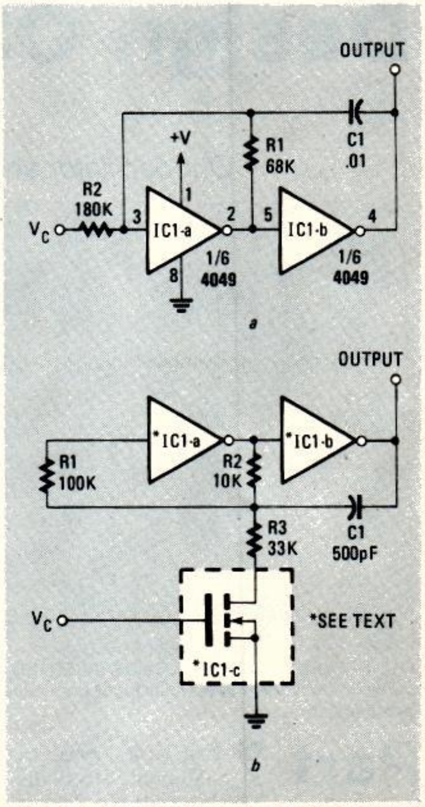


FIG. 5—A CMOS VCO can be built from several standard gates (*a*) or from a 4007 (*b*).

$$f = 1/(2.2 \cdot R1 \cdot C1).$$

The value of R1 can range from the value shown to several megohms; the value of C1 can be as high as 10 μF.

The output waveform of that circuit is slightly asymmetrical, especially when B-series devices are used. The problem with the B-series device is that the internal

continued on page 70