

# Direct Digital Synthesis (DDS) Controls Waveforms in Test, Measurement, and Communications

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In many kinds of equipment, it is important to produce and readily control accurate waveforms of various frequencies and profiles. Examples include agile frequency sources with low phase noise and low spurious signal content for communications, and simply generated frequency stimuli for industrial and biomedical applications. In such applications, the ability to generate an adjustable waveform conveniently and cost effectively is a key design consideration.

Various approaches have been used, but the most flexible one is *direct digital synthesis*<sup>1</sup> (DDS). A DDS chip<sup>2</sup>, or *direct digital synthesizer*, produces an analog waveform—usually a sine wave, but triangular and square waves are inherent—by generating a time-varying signal in digital form and then performing a digital-to-analog (D/A) conversion. DDS devices are primarily digital, so they can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies.

With advances in design and process technology, today's DDS devices are very compact and draw little power. Currently available DDS devices<sup>3</sup> can generate frequencies from well below 1 Hz up to 400 MHz (based on a 1-GHz clock), with time resolution to 48 bits. The low cost of devices using new process technologies—combined with DDS's inherently excellent performance and the ability to digitally (re)program the output waveform—make the DDS approach extremely attractive compared to more discrete and less flexible traditional solutions. Multichannel DDS devices, such as the 2-channel AD9958<sup>4</sup> and the 4-channel AD9959,<sup>5</sup> allow independent programming of up to four inherently synchronized outputs in space-constrained systems (e.g., phased-array radar/sonar, ATE, medical imaging, and optical communications).

Our objective here is to provide the reader with an understanding of a few important uses of DDS in existing applications, and to provide an insight into the key benefits the DDS device brings to these—and other potential applications. At present, the two principal forms of applications using DDS are waveform generation in *communications*—and signal analysis in *industry* and *biomedicine*. Typical other uses include electronic article surveillance (EAS) and maritime applications in sonobuoy systems.

Important applications exist in communications systems that require agile frequency sources with low phase noise and spurs, combining—as DDS does—excellent frequency-tuning resolution and spectral performance. Other typical DDS uses in communications include generating pilot signals for WDM optical-channel identification, enhanced-tunability reference frequencies for phase-locked loops (PLLs), as local oscillators, or even for direct transmission.

In the signal analysis category, many industrial and biomedical designs use DDS to digitally generate programmable waveforms with easily adjustable frequency and phase—without the need to change any external components, as is often the case with traditional waveform generators. Simple frequency adjustments can be used to locate resonances or compensate for temperature drifts. A DDS can be used as a flexible frequency stimulus in measuring sensor impedance, or to generate pulse-width-modulated signals for microactuators, or to examine attenuation in LANs or telephone cables.

## Applications in Industry and Medicine

**Signal-generator network analysis:** Many applications in electronics today involve gathering and decoding data for digital signal processing, analog measurements, fiber optics, and high-frequency communications.

This class of application involves stimulating a circuit or system with frequencies of known amplitude and phase, and analyzing the characteristics of the response to provide key system information. The *network under analysis* (Figure 1) can be anything from a length of cable to a measurement/sensor system. The typical requirement is to compare the response signal(s) to the input signal in phase, frequency, and amplitude.

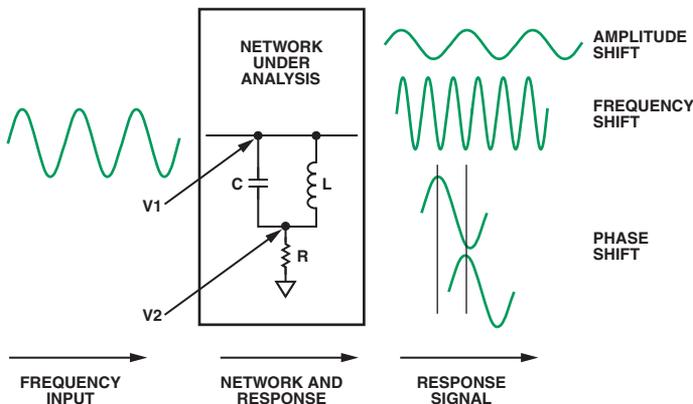


Figure 1. Response testing.

Where a train of frequencies is needed for excitation, a DDS chip is just right, since the stimulus frequency, phase, and amplitude can be software controlled with very tight resolution.

The system works by applying a signal having known frequency, amplitude, and phase to point V1 of the network (shown as a passive circuit for the sake of simplicity) in Figure 2. The amplitude and phase of the signal at point V2 will vary depending on the characteristics of the network. The time difference between the signals, V2 and V1, allows the user to calculate the phase shift, and the change in magnitude will give the relative amplitude shift. Differences in their frequency spectra can provide a measure of distortion. Knowing both the phase- and amplitude response of the system under test, it is possible to calculate its transfer function.

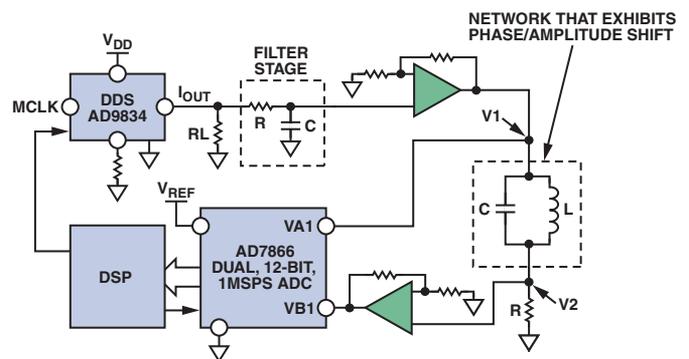


Figure 2. System block diagram.

Typical frequencies used in these applications tend to be from 0 kHz to 200 kHz, at the low end of the DDS frequency-handling range. For some applications a burst of one known frequency provides sufficient information; but for most it is required to sweep a range of known frequencies across the network and analyze the phase/amplitude data for multiple frequencies. A single DDS chip provides the entire frequency generation function, giving the user great flexibility in digitally controlling the frequencies required

for network control. With no external components required, the user just needs the ability to write to the DDS through its SPI interface. The output phase of the DDS is typically controllable with 10-bit-to-14-bit resolution, giving programmable phase resolution to <0.1 degrees.

In the system of Figure 2, the AD9834 DDS chip is used as the analog stimulus for the system. It is driven with a 50-MHz crystal oscillator. The frequency resolution of the AD9834 is 28 bits, which allows the frequency to be controlled to about 0.2 Hz. The DDS output amplitude is controlled by an external resistance to ground; and an external gain stage drives the network.

The output, loaded by resistor, RL, drives a low-pass RC filter, which band-limits the signal and filters out clock frequency, images, and higher frequencies. A buffer amplifier drives the network, represented here by an LRC circuit. The reference signal is connected to Channel 1 of a 2-channel, simultaneous-sampling ADC (such as the AD7866<sup>6</sup> 12-bit, 1-MSPS, dual ADC); and the response signal is applied to Channel 2 of the ADC.

A digital signal processor, used as a system controller, controls the DDS and the ADC sampling. The DSP handles the processing requirements of the system with simple arithmetic, or by FFT, DFT, or proprietary algorithms, and may also control any necessary amplitude- and phase calibration of the system.

### Other Applications

A similar approach may be used in many other applications, with variations that depend on the physics and circuitry employed. Examples include providing frequency sweeps for use in testing LVDTs (linear variable differential transformers); proximity sensing using a capacitive sensor; metal detection using balanced coils; blood measurement using a chemical sensor; flow measurement using ultrasonic sensors; and electronic article surveillance (EAS)—to prevent shoplifting—using RF-responding tags.

### DDS in Communications

Classically, when considering the design of a new frequency synthesizer, two basic approaches have been common: *phase-locked loops* (PLL) and *direct digital synthesis*. The choice is not always clear-cut; often the designer must make trade-offs or design additional circuitry to compensate for the weaknesses of the chosen technique.

However, now that both PLL and DDS circuits are available as low-cost components, it is becoming practical to consider designing a hybrid circuit combining both techniques, thus eliminating the trade-offs. The designer can take advantage of both methods to obtain an overall solution that outperforms individual PLL or DDS designs. We will discuss approaches with the benefits of:

- fine frequency resolution
- fast switching action
- fast settling time
- wide bandwidth
- very low power
- low phase noise and spurious noise

Two different PLL/DDS hybrid frequency synthesizers will be discussed here—a DDS providing a fine-tunable reference for a PLL, and a PLL with the internal offset from the local-oscillator (LO) frequency generated by a DDS.

**Fine-tunable reference for a PLL:** Figure 3 shows a phase-locked-loop frequency synthesizer with the reference frequency generated by the filtered output of a DDS. By using a hybrid solution, the tuning resolution of the DDS can enhance the tunability of the overall system to a level not possible with a PLL alone.

In this example, the PLL consists of an integer-N ADF4106<sup>7</sup> frequency synthesizer, plus an external loop filter and VCO. This configuration allows the designer to choose a VCO to meet the frequency conditions and a loop filter to fit the needs of the application. The reference is generated by an AD9834<sup>8</sup> DDS, followed by a filter and optional matched divider, for reducing noise and spurs.

The DDS, with its 28-bit tuning word, allows the reference frequency to be very narrowly tuned, resulting in fine adjustment of the output frequency much more conveniently than through the use of a fractional-N PLL.

For example, if the VCO has a frequency range of 100 MHz to 500 MHz, and the DDS output is in the neighborhood of 5 MHz, the range of N is from 20 to 100. Each step of N results in a 5-MHz step of output frequency (100 MHz, 105 MHz, 110 MHz, etc.) However, the AD9834's output can be set in small increments by simply adjusting the hexadecimal number written to the frequency register. The AD9834 can be tuned in increments as small as 0.2 Hz with a 50-MHz clock rate. This results in very fine tuning of the hybrid PLL/DDS.

Ideally, the reference would have low phase noise and spurious tones. The DDS output does indeed have low phase noise, but its spurious content may need to be addressed at some frequencies. The spurs are due to a truncation after the phase accumulator, which results in increased spurious content at particular sampling/output frequency combinations. These spurs may be minimized with additional filtering and a careful choice of sampling plan.

If switching speed is unimportant, the PLL bandwidth can be made extremely narrow to exclude reference spurs; then the phase noise and spurs are limited to those of the VCO. If the VCO is clean, this may be the simplest way to obtain a synthesizer with a wide bandwidth, fine resolution, good spurious noise, small size, and extremely low power, albeit with slow switching between frequencies.

To take advantage of the DDS's fast switching ability, as well as its high resolution, a wider PLL loop-bandwidth is needed—making the filter and the optional divider important for low noise and spurs. Note that the PLL increases the amplitude of the spurious tones, but not their frequency offset from the reference. Thus the filter in Figure 3 is necessary to confine the DDS-generated spurious tones and noise to a narrow bandwidth. After frequency multiplication by N, the noise and spurious tones will be increased by  $20 \log(N)$ , but only within the filter bandwidth. Ultimately, the selection of

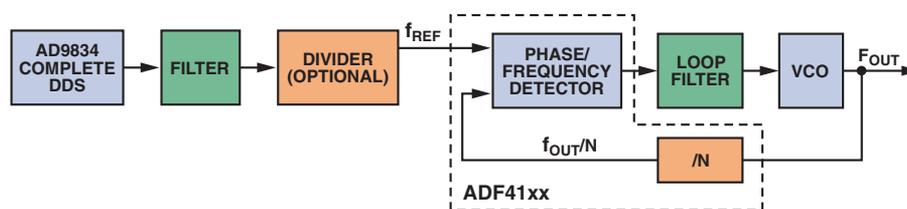


Figure 3. DDS as reference-frequency generator for a PLL.

the filter bandwidth and center frequency is a trade-off between switching speed, noise performance, and the need for continuous frequency coverage.

**PLL with the internal offset frequency generated by a DDS:**

Figure 4 shows a phase-locked-loop synthesizer with the internal offset frequency generated by a DDS.

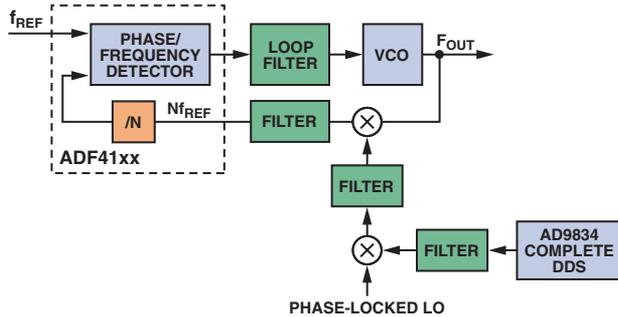


Figure 4. The AD9834 DDS generates the frequency offset for the ADF41xx PLL.

This circuit uses a finely set DDS frequency to modulate a local oscillator frequency, producing a sum/difference frequency which, when filtered, modulates the reference frequency, producing an output frequency,

$$f_{OUT} = Nf_{REF} \pm (f_{LO} \pm f_{OFFSET})$$

This is similar to multiloop synthesizer design, except that the fine-frequency-step PLLs are replaced by a single DDS. The fine frequency resolution of the DDS in this hybrid synthesizer can provide better frequency resolution than a PLL with many loops.

The PLL provides the coarse steps and, as before, the PLL output frequency (with the local oscillator) has the same basic resolution as the input reference frequency,  $f_{REF}$ . The DDS provides fine steps between each of the coarse steps, so that the ultimate output step size is that of the DDS. Using an AD9834 with a 50-MHz master clock, a step size of 0.2 Hz is possible.

**DDS in Data Encoding**

Because DDS devices make adjustment of frequency and phase an easy matter, they are especially useful in encoding data for phase- and frequency modulation onto a carrier. Here are two related applications harking back to the early days of radiotelegraphy.

**FSK encoding:** Binary frequency-shift keying (FSK) is one of the simplest forms of data encoding. The data is transmitted by shifting the frequency of a continuous carrier to one or the other of two discrete frequencies (a binary operation). One frequency ( $f_1$ ) is designated as the “mark” frequency (binary one) and the other ( $f_0$ ) as the “space” frequency (binary zero). Figure 5 shows the relationship between the data and the transmitted signal.

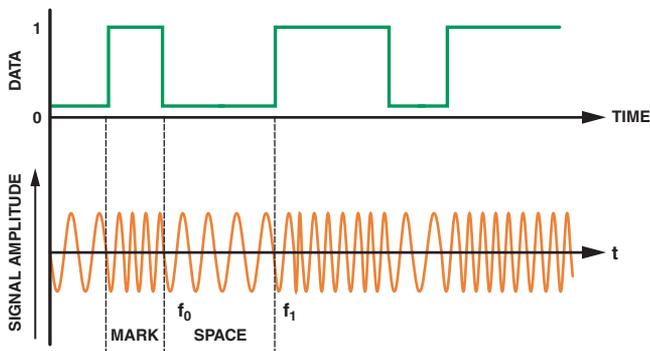


Figure 5. FSK modulation.

This encoding scheme is easily implemented using a DDS. The DDS frequency tuning word representing the output frequencies changes in order to generate  $f_0$  and  $f_1$  in synchronism with the pattern of 1s and 0s to be transmitted. The user programs the tuning words corresponding to the chosen frequencies into the device before transmission. In the case of the AD9834, two frequency registers are conveniently available for FSK encoding. A dedicated pin on the device (FSELECT) is used to select the frequency register corresponding to the appropriate tuning word. The block diagram in Figure 6 demonstrates the implementation of FSK encoding.

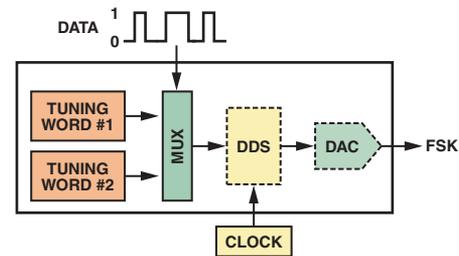


Figure 6. A DDS-based FSK encoder.

**PSK encoding:** Phase-shift keying (PSK) is another simple form of data encoding. In PSK, while the frequency of the carrier remains constant, the phase of the transmitted signal is varied to convey the information.

There are various schemes that can be used to accomplish PSK. The simplest method, using only two signal phases— $0^\circ$  and  $180^\circ$ —is commonly known as *binary PSK* (BPSK).  $0^\circ$  corresponds to Logic 1, and  $180^\circ$  corresponds to Logic 0. The state of each bit received is determined according to the state of the preceding bit. If the phase of the wave does not change, the signal state stays the same (low or high). If the phase of the wave reverses, i.e., changes by  $180^\circ$ , the signal state changes (from low to high, or from high to low).

PSK encoding is easily implemented with DDS products. Most of the devices have a separate input register (a *phase register*) that can be loaded with a phase value. This value is directly added to the phase of the carrier without changing its frequency. Changing the contents of this register modulates the phase of the carrier (thus generating a PSK output signal). For applications that require high-speed modulation, the AD9834 allows the preloaded phase registers to be selected using a dedicated input pin (PSELECT); toggling this pin modulates the carrier as required.

Other phase angles may be used. More complex forms of PSK employ four or eight different phases. This allows binary data to be transmitted at a faster rate per phase change than is possible with BPSK modulation. For example, in four-phase modulation, *quadrature PSK* (QPSK), the possible phase angles are  $0^\circ$ ,  $+90^\circ$ ,  $-90^\circ$ , and  $180^\circ$ ; each phase shift can represent two data bits. The AD9830,<sup>9</sup> AD9831,<sup>10</sup> AD9832,<sup>11</sup> and AD9835<sup>12</sup> provide four phase registers to allow complex phase-modulation schemes to be implemented by continuously updating different phase offsets to the registers.

**Sonobuoy applications:** DDS is useful in *sonobuoy* communications. A sonobuoy is a device that lies in the water and captures ambient sounds in the ocean. Common applications for sonobuoys are in the detection, localization, identification, and tracking of seismic events and underwater targets such as submarines and whales. Arrays of sonobuoys can be used to determine target position, velocity, and direction.

There are four main components to a sonobuoy: a float, a radio transceiver, a battery, and a hydrophone. The hydrophone is an underwater sensor that converts sound pressure waves into electrical voltages that get amplified and sent up to the surface

float. The radio signal is picked up by an antenna and a radio receiver, usually on an aircraft or a ship.

Active sonobuoys transmit sound waves, which bounce off objects. The distance and direction to the object can be determined from the reflected signal. A transducer is used to introduce the acoustic wave into the water and to manipulate the return echoes, which are then amplified for VHF radio transmission. Passive sonobuoys do not emit any sound; they just sit and listen for incoming sounds. In both cases the data is transmitted back to a ship or aircraft, often using spread-spectrum communications, in which the frequencies are rapidly hopped about so as to resemble random noise. A DDS is often used to provide the frequency hopping in the *transmit* and *receive* sections.

The AD9834 is ideal as an agile frequency source in the transmitter section of the sonobuoy (Figure 7). Typical frequencies transmitted are from 136 MHz to 174 MHz.

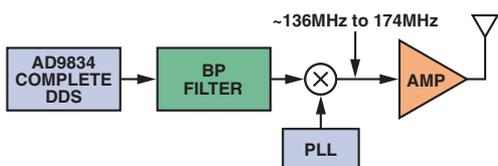


Figure 7. DDS in *transmit* section of sonobuoy.

A block diagram of a typical receiver, for GPS position location, is shown in Figure 8.

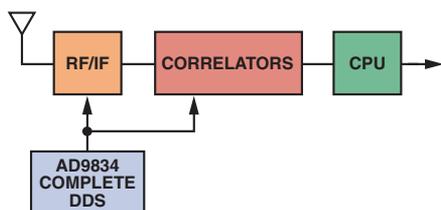


Figure 8. DDS in *receive* section of sonobuoy.

The receive portion of the sonobuoy consists of a GPS antenna, low-noise amplifier, and downconversion front-end stage. The downconversion is driven by the DDS. The signal from the front end is sampled and digitized, and the resulting data stream (which contains the spread-spectrum data of all GPS satellites in range of the antenna) is passed to correlators for spread-spectrum processing. The output of the correlation process is converted by the CPU to provide the sonobuoy's coordinates.

The DDS offers advantages for both the transmitter and receiver, because of its fine-tuning capabilities. The low power (25 mW) and low cost of the AD9833/AD9834 make them an ideal solution for battery-powered, disposable applications, such as in sonobuoys.

**Fiber optic channel identification:** Communication using light waves over fiber optic cables has greatly increased bandwidth and capacity over that available with copper-core technology. Capacity is increased further by using the multiple channels that *wavelength division multiplexing* (WDM) can make available at relatively low cost.

WDM involves combining separate light wavelengths (colors) from the various simultaneous input data streams, and transmitting the sum of these channels ("white" light) through a single optical

fiber. Different protocols can be mixed within the same link. At the receiving end, the light is separated into its components, and demodulated.

Although all of the signals are transmitted at the same time, it is desirable to identify from which channel a signal originated. One way to distinguish between channels is to add a pilot signal with identifiable parameters (e.g., amplitude, frequency, phase, etc.) to each channel's digital data. In optical transmitters the pilot signal is added by varying the current flowing through the laser diode. Figure 9 shows how this is done.

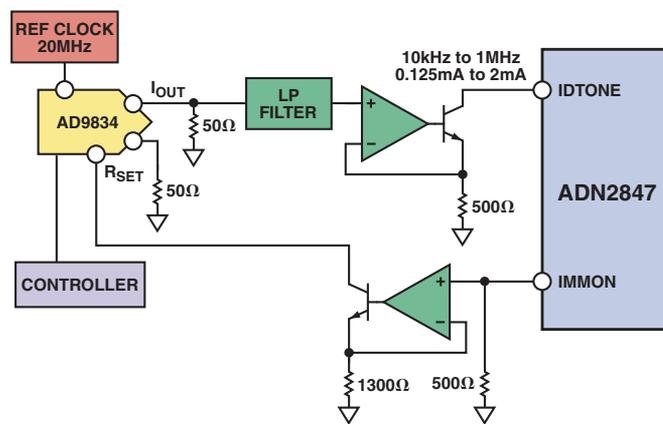


Figure 9. DDS in an optical-fiber communications application.

The ADN2847 laser-diode driver operates at any rate between 50 Mbps and 3.3 Gbps. An external sink current at IDTONE, supplied for fiber identification in WDM, modulates the *optical 1* level over a possible range of 2% of minimum  $I_{mod}$  to 10% of maximum  $I_{mod}$ . The AD9834 generates the modulation waveform and controls the current sinking out of IDTONE by controlling the voltage across a 500  $\Omega$  resistor. A dc current on IMMON, reflecting the modulation current, is used in a feedback loop to control the AD9834 output level via its  $R_{SET}$  pin.

## CONCLUSION

Direct digital synthesis, which generates analog waveforms with digitally adjustable high-resolution phase and frequency, is useful in a wide variety of applications in test, measurement, and communications. Integrated-circuit DDS devices are compact, require little power and space, are low in cost, and easy to apply. ▶

## REFERENCES—VALID AS OF NOVEMBER 2005

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