Frequency synthesizers — 2

The generation of wanted frequencies from other frequencies

by R. Thompson, M.I.E.E.

Part 1 of this article described circuits which generate wanted frequencies from other frequencies using frequency addition and multiplication. This second part describes circuits for a third method, that of frequency division. It also introduces prescalers and explains how they can be used to extend the frequency range of frequency division circuits.

FREQUENCY DIVISION, even at frequencies up to 1GHz, is now almost exclusively carried out by circuits based on the digital binary counter. Alternative methods such as synchronising subharmonic oscillators or tuned regenerative loops have been outdated by the low cost of digital integrated circuits.

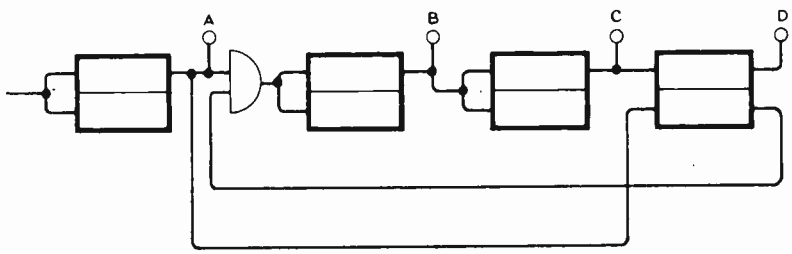
Simple cascading of binary counting elements provide division ratios of 2^N, where N is the number of elements. Generally, however, the division ratios required in synthesizers will not be a 2^N number, in which case the binary counters must be modified. The modifications normally involve the use of feedback loops which either cause binary elements to change state or inhibit clocking pulses. For instance, a divide-by-10 function is obtained with four binary circuits. These would count from 0 to 15, resetting to 0 on the 16th clock input if connected in simple cascade. After 8 counts, however, the last stage changes from 0 to 1 and this change in state can be used to bypass stages 2 and 3. Only two pulses are therefore required to return the counter to all zeros. The arrangement and logic table for this circuit are shown in Fig. 10.

A very common requirement in synthesizers is for a divider which can be readily varied by switches or control logic. Normally the approach to this requirement is to use standard counting blocks, 2^N or 10, in conjunction with either recognition or presetting logic. These arrangements are shown in Fig. 11. In (a), the setting switches programme the recognition circuits to the required division number. The counter then starts at zero and counts up to the required number, the recognition circuits produce an output pulse and this is used to reset the counter to zero. In (b), the required number is preset into the counter, which then counts down to zero. This produces an output pulse which again presets the counter. Alternatively, the "nines complement" of the number may be preset and the counter counted up to all nines.

A problem of frequent concern with dividers is the time delay introduced by the logic elements. These can accumulate to very significant times when many elements are cascaded. Synchronous counters avoid this accumulation by clocking all stages with the same pulse, as shown in Fig. 12. Arrangement (a) is a ripple-through counter where clocking is effected by the change of state of the previous stage. In arrangement (b) all stages are clocked in parallel with the clock pulses, the pulses being gated by the state of all "previous" stages. This achieves the same counting action as (b) but with almost synchronous output changes.

When operating in the synchronous mode, differential delays throughout a logic circuit are reduced. This makes the logic processing easier because the changes occur at defined times. It does not, however, increase counting speed, on the contrary it slows it down since time must be allowed for gates to be set between clock pulses.

Variable divider circuits are typically three times slower than straightforward counters because terminal states have to be detected and the counter reset once every count cycle. This resetting action must be completed between input clock pulses in order that no input pulse is missed. One method of exten-



Count	0	1	2	3	4	5	6	7	8	9	10
A	0	1	0	1	0	1	0	1	0	1	0
B	0	0	1	1	0	0	1	1	0	0	0
C	0	0	0	0	1	1	1	1	0	0	0
D	0	0	0	0	0	0	0	0	1	1	0

Fig. 10. *Circuit and logic table for a digital binary counter which can be used to provide frequency division. See text.*

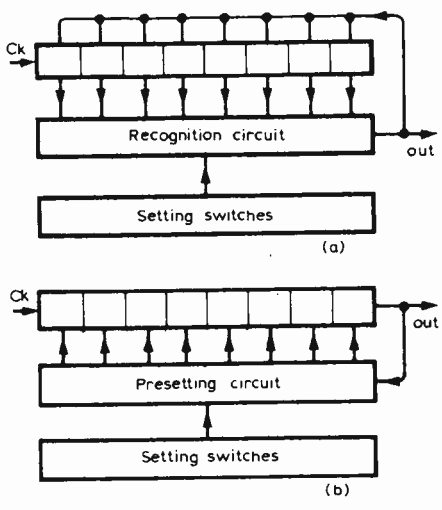


Fig. 11. *Dividers whose division ratios can be varied by switches or control logic. In (a) the setting switches programme the recognition circuits to the required division number and the counter starts at zero and counts up to the required number. In (b) the required number is preset into the counter, which then counts down to zero. This produces an output which presets the counter.*

ding the frequency range of the variable divider is to use an "early decode" circuit, as in Fig. 13(a). The counter is preset and commences counting, in this case downwards, in the normal manner. The most significant stage reaches zero first, followed by the next most significant and so on until all but the least significant are at zero. All of these zeros are gated together with a signal from the least significant stage whose signal is taken not from the zero but from some higher state such as 2. The early decode gate therefore produces an output two clock pulses before the counter would have reached all zeros. The next clock pulse can now trigger the early decode bistable whose output resets all counter stages and the final clock pulse of the counting cycle resets the bistable releasing the reset from the counter. At this stage the counter is ready to start counting from the reset state at the next clock pulse. This particular arrangement allows a full clock cycle for the counters to reset; obviously the decoding could be made even earlier to provide longer resetting times. Earlier decoding would require further bi-stables in the decoder circuit to count off the clock pulses missed while the main counter was resetting.

Another method of extending the frequency range is to use a higher speed divider ahead of the main variable divider. This "prescaler" could be a fixed divider as shown in Fig. 13(b). Since the maximum frequency to be handled by the variable divider is reduced by a factor P, say, the arrangement has the disadvantage that changing the variable division ratio by one now changes the overall division ratio by P. This can be overcome by using a prescaler providing two alternative division ratios.

Figure 13(c) shows the arrangement for such a variable modulus prescaler. If the A and the N counters were connected in cascade, we would have a counter with a least significant digit (l.s.d.) equal to that of the l.s.d. of A and, with the clock input applied to A, the maximum input frequency would be set by the speed of the A counter. With a variable modulus prescaler the output of the prescaler is tapped up the variable counter, splitting it into A and N as shown.

With a prescaler division ratio of P, the l.s.d. of N represents division increments of P. The purpose of having an alternative prescaler ratio greater than P, that is (P + M), is to count off the digits in the required division ratio which are less significant than P. These digits are of course those in A whose l.s.d. will represent increments in M.

The count cycle starts with A-plus-N set to the required division number and the prescaler set to divide-by-(P + M) such that the prescaler produces an output after every (P + M) input pulse. This decrements the N counter by one, registering P pulses, and also decrements the A counter, registering M pulses. The total change in A and N therefore directly indicates the total input count. When the A counter reaches zero, that is after trhe required number of M decrements, it switches the prescaler to a division ratio of P. Although the A counter stops, the N counter continues to decrement until it too reaches zero. When this occurs an output pulse is generated which is also used to reset the A and N counters.

It can be seen that the significance of the l.s.d. of the variable divider is set by the difference of two division ratios. The maximum input frequency, however, is increased by the smaller of the two prescaler division ratios. For instance, if the prescaler ratios are 10 and 11, a ten times extension of frequency can be obtained with no alteration to the l.s.d. significance.

The prescaler will only work when the number set in A is less than that in N. Since the A count can only be decremented by (P + M) input pulses the N counter must always be able to correctly register the P portion as part of the total count.

We can derive the ratio of input and output frequencies for the variable modulus divider quite easily, as follows:

Input pulses to decrement A to zero = (P + M)A

Count in N when A reaches zero = N – A

Number of further inputs for N to reach zero = (N – A)P

Therefore the total count in one cycle = (P + M)A + (N – A)P

= MA + NP

and $f_{out} = f_{in}(MA + NP)$

Where very-high-speed working is required it may be necessary to use the "early decode" technique described earlier to provide time for the A and N counters to be reset.

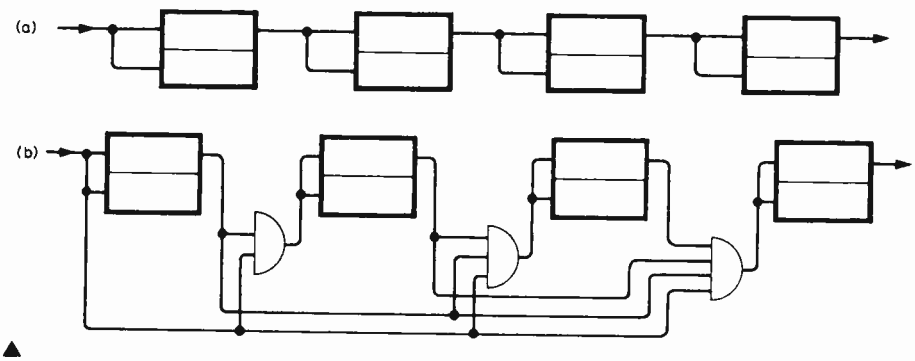


Fig. 12. *Synchronous counters avoid the accumulation of time delays by clocking each stage with the same pulse. (a) is a non-synchronous ripple-through counter where clocking is effected by the change of state of the previous stage. In (b), which is synchronous, all stages are clocked in parallel with the clock pulses, which are gated by the state of all previous stages.*

Fig. 13. *Arrangements for extending the frequency range of variable dividers. (a) uses an 'early decode' circuit, and (b) employs a prescaler. See text. Arrangement (c) is a variable-modulus prescaler which provides two alternative division ratios.*