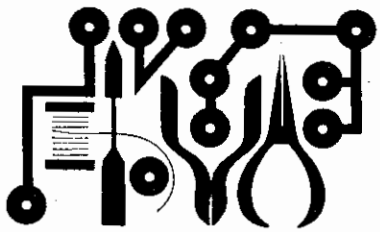
Experimenter's Corner



By Forrest M. Mims

The Digital Phase-Locked Loop (Part 1)

RECENTLY, I was talking to the parts buyer for an electronics supplier about sales volumes of various integrated circuits. The most surprising thing I learned was that sales of the 4046 digital CMOS phase-locked loop (PLL) are only a trickle compared to those of other ICs.

This is puzzling, because the 4046 is is one of the most versatile CMOS chips. It is also unfortunate—the 4046 is very handy if you know how to use it. Among the many applications of the 4046 are those in frequency modulation and demodulation, voltage-to-frequency conversion, frequency synthesis, tone decoding, FSK demodulation, and frequency multiplication.

One possible reason for the low sales volume of the 4046 is that little descriptive or applications information about this chip has appeared in electronics magazines and books. To rectify this situation, we will unravel some of the mysteries surrounding the digital PLL and present some basic circuits. By the time you finish experimenting with some of the more advanced application circuits, you'll be well acquainted with the operating principles of the digital PLL, an exceptionally versatile CMOS chip.

Phase-Locked Loop Basics. The simplest PLL consists of a phase comparator, a voltage-controlled oscillator (vco), and a low-pass loop filter, all arranged as shown in Fig. 1. In operation, the vco oscillates at a frequency determined by an external *RC* network. This frequency is applied to one input of the phase comparator. An external signal applied to the second input of the phase comparator causes it to generate an *error voltage* whose magnitude is proportional to the difference between the external source and vco frequencies.

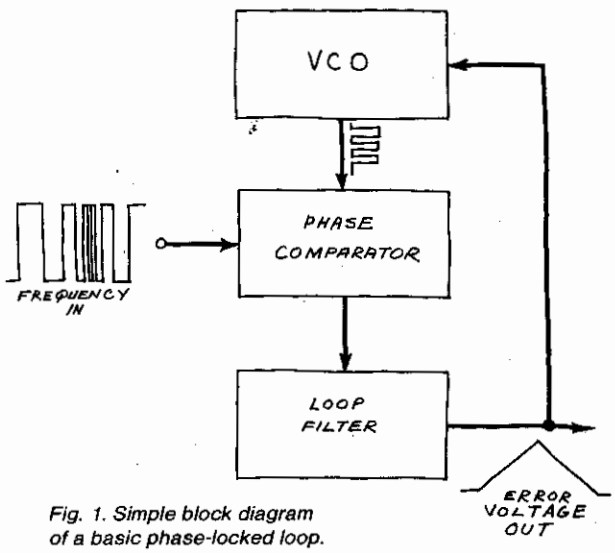


Fig. 1. Simple block diagram of a basic phase-locked loop.

The low-pass loop filter smooths the pulsating error voltage into a dc level which is applied to the control input of the vco. The vco responds to the error voltage by moving its frequency of oscillation toward that of the input signal. This *capture* process continues until the vco frequency equals the input frequency. When this occurs, the PLL is said to be *locked* or *phase-locked* to the input signal.

When the PLL is locked to the input frequency, the vco automatically tracks any changes in the input frequency that fall within a window called the *lock range*. The lock range is always greater than the *capture range*, the band of frequencies over which the PLL can hunt for and "capture" an incoming signal.

It is important to understand that, although the loop filter is essential for proper operation of the PLL, its time constant limits the speed with which the system can track changes in the input frequency. It also limits the capture range. On the other hand, the loop filter helps prevent noise voltages from adversely affecting loop operation. The charge stored in the loop filter's capacitor helps the quick recapture of a signal temporarily lost because of a noise spike or other transient.

In short, the loop filter is a necessary part of the PLL, but it imposes certain operating restraints and tradeoffs. Be sure to keep this in mind when you experiment with PLL circuits, because optimizing PLL performance often requires experimentation with loop-filter component values.

Inside the 4046 PLL. Figure 2 is a block diagram of the 4046 CMOS micropower PLL. One of the most obvious features of this chip is that it includes *two* phase comparators. Phase Comparator I is an exclusive-OR gate that provides a high degree of noise immunity. Unfortunately, this comparator has a tendency to lock onto input signals having frequencies close to harmonics of the vco frequency. Also, it requires a square-wave input with a 50% duty cycle.

Phase Comparator II is a relatively complex network of four edge-triggered flip-flops with control gates and a 3-state output stage. While this detector is less susceptible to the harmonic problem that plagues Phase Comparator I, it is much more sensitive to noise.

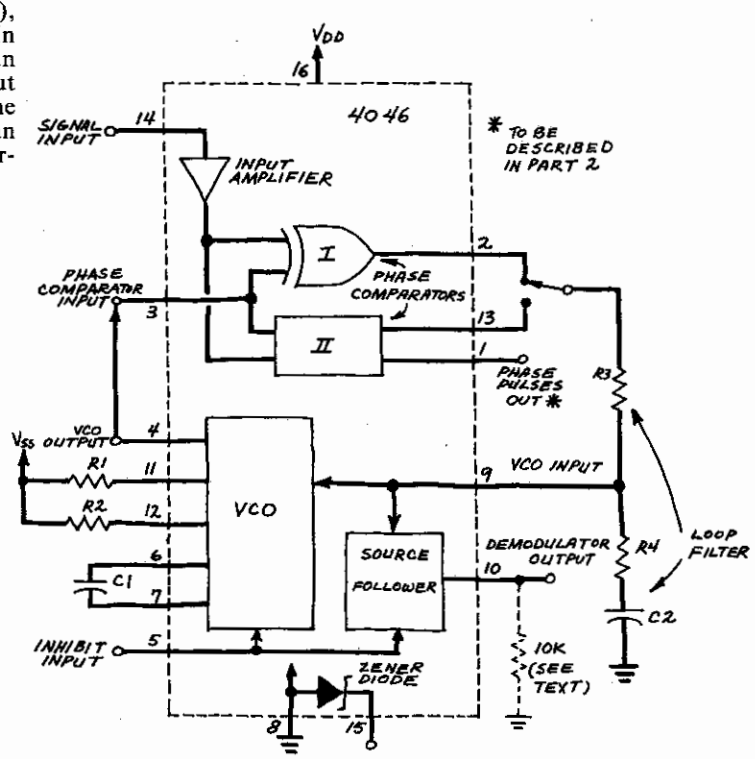


Fig. 2. Block diagram of the 4046 CMOS micropower phase-locked loop.

Both phase comparators are simultaneously driven by an input amplifier which will be described later. Their outputs, however, are brought out to separate pins (2 and 13). This means that the user can select either comparator for a specific application by simply connecting its output pin to the vco through the loop filter.

Because the flip-flop comparator has a frequency-tracking range of more than 1000:1, it is often a better choice than the exclusive-OR comparator which tracks over a range of only ±30 percent. Another advantage of the flip-flop comparator is that it can accept input pulses of any duty cycle (for example, very narrow pulses).

The vco incorporates an NMOS input stage that provides an input impedance of 10^{12} ohms. Its linearity ranges from 0.1 percent (V_{DD} = +5 V) to 0.8 percent (V_{DD} = +15 V). The oscillator's maximum operating frequency typically ranges from 0.7 MHz (V_{DD} = +5 V) to 1.9 MHz (V_{DD} = +15 V).

Figure 2 shows a source follower connected to the vco input. This buffer stage is intended specifically for frequency-demodulation applications. It allows an external amplifier or other circuit to be driven by the output signal from the loop filter (the filtered error voltage) without loading down the filter. When the DEMODULATOR output (pin 10) of the source follower is used, a load resistor of at least 10,000 ohms must be connected between pin 10 and ground (V_{SS}). Otherwise pin 10 should be left floating.

Both the vco and source follower are provided with a common INHIBIT terminal (pin 5) to reduce standby power consumption. A logic 0 (V_{SS}) at pin 5 enables the vco and follower, and a logic 1 (V_{DD}) inhibits them.

The final component in the 4046 is a 5.2-volt zener diode. This zener is intended for voltage-regulation applications, and its use is optional.

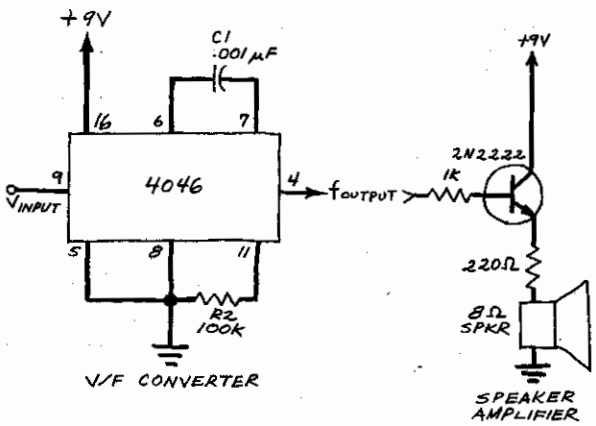


Fig. 3. A basic 4046 vco circuit used as a V/F converter with a speaker amplifier.

Using the 4046. The 4046 requires a power supply that can furnish from 3 to 18 volts at modest current levels. Power consumption depends upon both the vco frequency and what percentage of time the vco is enabled. For example, at a frequency of 10 kHz, the 4046 consumes only 600 microwatts—about 1/160th the power required by a typical analog bipolar PLL such as the 565. Suffice it to say that the 4046 is ideally suited for battery-powered operation!

A minimum number of external components is required to use the 4046. The center frequency of the vco is determined by one capacitor (*C1*) and one or two resistors (*R1* and *R2*) as shown in Fig. 2. When only *R1* is used, the vco frequency can be varied from 0 Hz when the control voltage at pin 9 is V_{SS} to a maximum frequency given by the equation: $f_{max} = 1/R1(C1 + 32\ pF)$ when the control voltage is V_{DD}. For proper

operation, the resistance of *R1* should be between 10,000 ohms and 10 megohms.

Resistor *R2* is included when it is desirable to move the minimum vco frequency to some point above 0 Hz. For this reason, it is called the *offset resistor*. The minimum frequency resulting from the inclusion of *R2* is determined by solving the equation: $f_{min} = 1/ R2 (C1 + 32\ pF)$ when the control voltage at pin 9 is V_{SS}. When *R2* is used, the maximum vco frequency when the control voltage is V_{CC} is found by adding f_{min} to the f_{max} obtained from the previous equation.

These vco design equations are extracted from Motorola's MC14046B specifications sheet. They apply only when the values of *R1* and *R2* are between 10,000 ohms and one megohm and when that of *C1* is between 100 pF and 0.01 μF. Nevertheless, the manufacturer's specifications sheet observes that experimentation is in order to determine the exact component values required for a particular application because, ". . . calculated component values may be in error by as much as a factor of 4." This poses no problem because it's a simple matter to use trimmer potentiometers for *R1* and *R2* and to adjust them to get the desired frequency range.

The loop filter, like the vco, also requires a capacitor (*C2*) and one or two resistors (*R3* and optional *R4*). The best explanation of this rather touchy circuit that I have found is in Don Lancaster's *CMOS Cookbook* (Howard W. Sams, 1977, pp. 363-364).

Earlier, we briefly covered some of the loop-filter design tradeoffs. Don, who seems to know more about the real-world idiosyncrasies of the 4046 than the data-sheet authors, says that both *R3* and *R4* are necessary to avoid driving the loop into near-oscillation. He reports that best operation is obtained when the resistance of *R4* is from 10 to 30 percent of that of *R3*. This provides enough damping to eliminate loop overshoot and oscillation, but still ensures a reasonably quick response to changes in the input frequency.

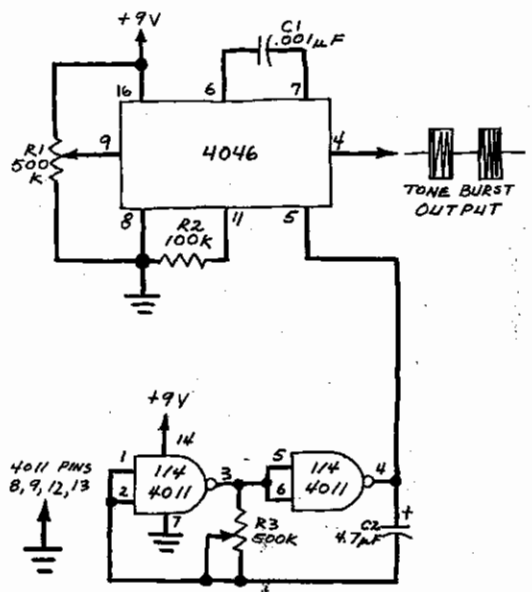


Fig. 4. A tone-burst generator in which R1 controls frequency and R3 burst rate.

Don recommends nominal values of 470,000 ohms for *R3*, 47,000 ohms for *R4*, and 0.1 μF for C2. A longer *RC* time constant means excessive delay when the loop is tracking quickly changing input voltages. A smaller *RC* product can cause erratic changes in the vco frequency as the loop tracks a rapidly changing signal.

I said that we would have more to say about the 4046 input amplifier later. Don comes directly to the point on this subject, so let's hear from him again. "*The linear amplifier operation of pin 14 is an unmitigated disaster when the wideband phase detector is being driven. Don't use it this way*! Linear operation causes extra amplitude-variation sensitivity, jitter, tearing and generally poor noise immunity" (*CMOS Cookbook*, p. 363).

One solution to this problem is to apply only full logic levels to the input. If this isn't possible or practical, pin 14 should be pulled up with a 10,000-ohm resistor to V_{DD}. The input signal can then be coupled into pin 14 by means of a 0.1-μF capacitor. In any event, if the input is a low-frequency train of slowly rising and falling pulses, the pulses must be conditioned with an appropriate pulse-shaping circuit.

VCO Application Circuits. An important feature of the 4046 is that the vco section can be used on its own for many practical applications, several of which will now be described. Experimenting with them will provide important experience for working with the chip as a complete PLL.

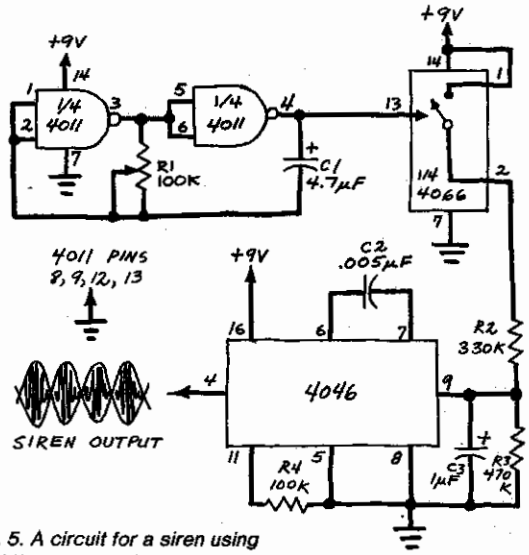


Fig. 5. A circuit for a siren using a 4066 analog switch to vary the sound.

Voltage-to-Frequency Converter. Figure 3 shows the most basic 4046 vco circuit possible, a simple V/F converter. Varying the input voltage from V_{SS} (ground) to V_{DD} will shift the output frequency over a range of 0 Hz to 18.5 kHz. You can use this circuit as a tunable oscillator by connecting the opposite ends of a 500,000-ohm potentiometer to V_{DD} and ground and by connecting the rotor to pin 9.

Figure 3 also includes a basic speaker amplifier that can be used with this and other 4046 circuits.

Tone-Burst Generator. Figure 4 is a simple tone-burst generator. Potentiometer *R1* controls the tone frequency and *R3* controls the burst rate.

Siren. The operation of the siren shown schematically in Fig. 5 is controlled by a 4066 analog switch. When the super-low-frequency NAND gate oscillator closes the switch, capacitor *C3* charges to V_{DD} through *R2*. When the analog switch is opened, *C3* discharges through *R3*. Because the voltage across *C3* controls the vco frequency, the result is an up-down siren effect.

Experiment with the various *RC* time constants to alter the sound of the siren. Components *R1* and *C1* control the cycle time, *R4* and *C2* control the frequency, and *R3* and *C3* control the wail.

To be Continued. In Part 2 we'll examine several PLL applications for the 4046. In the meantime, get some practical experience with this versatile chip by experimenting with circuits presented this month. ◇

Experimenter's Corner

By Forrest M. Mims

The Digital Phase-Locked Loop (Part 2)

IN LAST month's column, we introduced one of the most versatile MSI (medium-scale-integration) CMOS chips available, the 4046 micropower phase-locked loop (PLL). We also experimented with several application circuits, all of which used only the vco (voltage controlled oscillator) section of the 4046.

In this final installment on the 4046, we'll experiment with several applications that use the 4046 in its closed-loop or PLL mode. To refresh your memory about how the 4046 works, you might want to scan Part 1 before reading on since we'll be using several terms which apply exclusively to phase-locked loops.

The first circuit to be described, a PLL lock indicator, has no use on its own. Be sure to study it, though, since it serves a very important function when connected to a 4046. You can assemble it on a corner of a breadboard, and it will then be available should you want to connect it to the 4046 circuit with which you are experimenting.

PLL Lock Indicator. It's often difficult to determine whether or not a PLL is out of lock, particularly if a scope is not available. RCA application note ICAN-6101 recommends a simple NOR gate lock-detection circuit, a slightly modified version of which is shown in Fig. 1.

The lock indicator monitors the *phase pulses* output (pin 1) of phase comparator I and the output (pin 2) of phase comparator II. The output of the second NOR gate goes high and extinguishes the red LED when the loop is locked. When the loop is out of lock, the red LED flashes or appears to glow continuously. The optional NOR gate causes the green LED to glow when the loop is locked and go dark when the loop is out of lock.

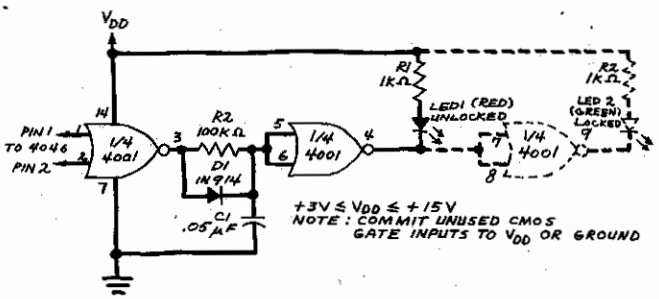


Fig. 1. A simple NOR-gate lock-detection circuit using a 4046 micropower PLL.

This simple circuit is a handy addition to any PLL since it provides an instant indication of a possible malfunction. It can also be used as an active part of a frequency detector or FSK demodulator. In the latter application, a binary signal is converted into a dual-frequency audio tone for remote transmission or storage on magnetic tape. A familiar example of FSK among computer hobbyists, the Kansas City Cassette Tape Standard, assigns a frequency of 1200 Hz to logic 0 and 2400 Hz to logic 1.

The PLL lock indicator can detect the presence of a 0 or 1 if the vco is adjusted so its minimum and maximum frequencies (see Part 1) encompass one of the two frequencies. The lock indicator will then go high for one tone and low for the second tone.

FSK Detector. A 4046 circuit designed specifically for Kansas City FSK detection is shown in Fig. 2. The vco is tuned by selecting *R1* and *R2* to give a capture bandpass from 2100 to 2700 Hz with a peak response of 2400 Hz. Frequencies outside the capture window are not detected; hence the lock detector goes high for a 2400-Hz input signal and low for a 1200-Hz input signal. These logic states can be reversed by adding a third gate in the 4001 to the output of the detector.

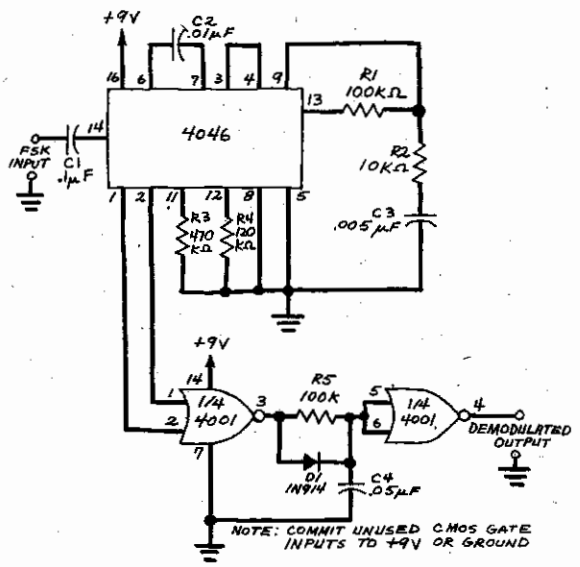


Fig. 2. A frequency-shift-keying (FSK) detector circuit.

Tone Detector. The circuit in Fig. 2 can be used to detect a wide range of input frequencies. For example, when *R4* is 1 kΩ and *R3* is 33 kΩ, the circuit responds to an incoming frequency of 48.775 kHz. The capture window with these values is *very* narrow (48.76-48.80 kHz). This demonstrates the possibility of using the 4046 as a precision tone detector. This application is normally reserved for the 567, a bipolar chip that uses considerably more power than the 4046.

It's easy to alter the response of the loop by substituting potentiometers for *R1* and *R2*. Or you can calculate the resistances required to define a specified frequency window (or loop capture range) by using the equations given in Part 1 or in the 4046 data sheet.

A commercial function generator or a simple dual-gate astable can be used to provide a variable-frequency input signal. A digital frequency meter to measure the peak detection frequency and the capture range is very helpful, but you can design a working circuit without one.

Analog Frequency Meter. In Part 1 we experimented with the 4046 vco as a voltage-to-frequency (V/F) converter.

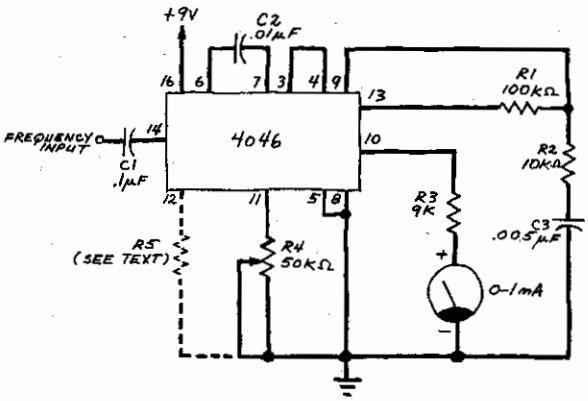


Fig. 3. Frequency-to-voltage converter as an analog meter.

Thanks to the filtered error voltage available from the source follower (pin 10), the 4046 can also be used as a micropower frequency-to-voltage (F/V) converter. Figure 3 shows one of many possible 4046 F/V application circuits: an analog frequency meter. The input frequency is read out on a 0-1-mA meter connected in series with pin 10 and a 9 kΩ load resistor (which doubles as a current limiter).

With the values shown, the frequency meter has a full-scale response of 100 to 8000 Hz. Below 100 Hz, the meter's needle will oscillate or indicate an erroneous reading.

The circuit is calibrated by applying a 5-kHz input signal and adjusting *R4* to produce a meter indication of 0.5 mA. Since the circuit does not have a perfectly linear response, you will need to make a new meter scale or conversion table if you want to use it as a practical frequency counter.

Resistor *R5* is used only to add an offset to the lower end of the frequency measurement scale. For example, when *R5* is 100 kΩ and R4 is adjusted to give an output of 0.5 mA at an input frequency of 5 kHz, the frequency measurement range is 2.3 to 7.0 kHz.

The lock indicator shown in Fig. 1 is a particularly handy addition to this circuit since it provides immediate warning when the circuit is out of range. This prevents erroneous frequency measurements.

Frequency Synthesis. Figure 4 shows how to synthesize exact multiples of a specified input frequency by inserting a

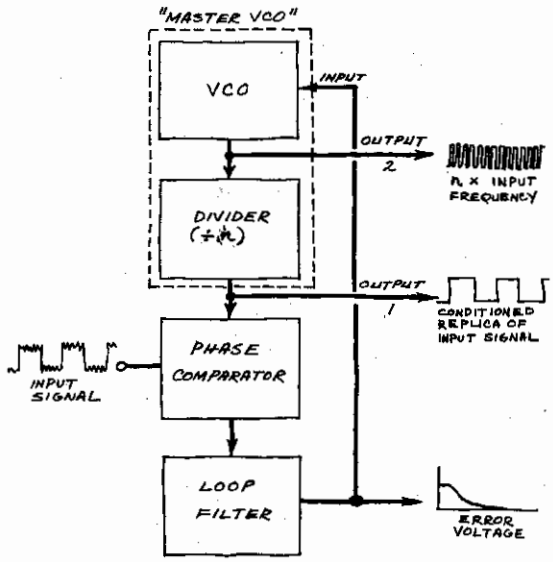


Fig. 4. A phase-locked-loop circuit with a divider.

divide-by-*n* counter between the vco and phase comparator of a PLL. You can understand how this arrangement works by thinking of the vco and divider as a single functional block or *master vco* instead of two separate circuits. The input (error voltage) and output (conditioned replica of the input signal)

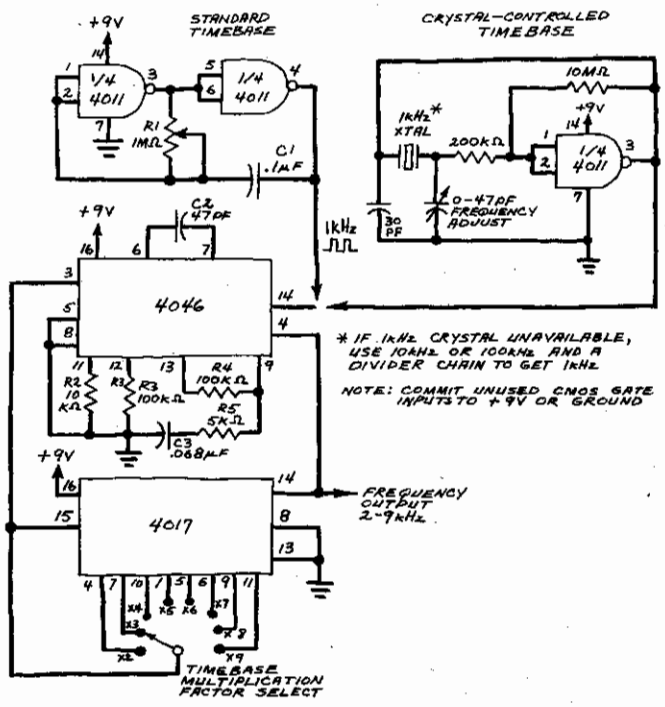


Fig. 5. Basic 2-to-9-kHz frequency synthesizer circuit.

of this master vco are indistinguishable from those of a loop without the divider. The only difference is a second output connected directly to the internal vco having a frequency of *n* times the input frequency.

PLLs with dividers are used in many kinds of frequency synthesizers and function generators. They are particularly important in CB radios and other multiple-channel telecommunications equipment since they provide a wide range of precise output frequencies from a single crystal-controlled reference oscillator.

Basic Frequency Synthesizer. One way to make practical use of a PLL with a divider inserted in the feedback loop is shown in Fig. 5. In this circuit, a 4017 counter is connected as a programmable divide-by-*n* counter where *n* is 2 to 9.

In operation, the NAND gate oscillator serves as a time-base which supplies a reference frequency of 1 kHz to the 4046 input. An 8-position selector switch connects the 4017 reset input to one of the eight count outputs. When the selected count is reached, the 4017 is reset and a new count cycle begins. This provides eight frequency steps ranging from two to nine times the time-base frequency. Each is a precise multiple of the time-base frequency.

For best results, especially in precision applications, use the crystal-controlled time base (also shown in Fig. 5). For non-precision applications or preliminary tests while you are

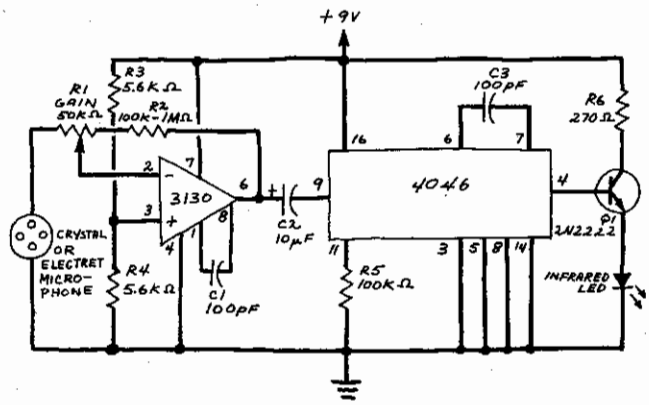


Fig. 6. Pulse-frequency-modulated lightwave voice transmitter.

awaiting arrival of the crystal, use the version without crystal control.

By using a string of divide-by-ten counters in place of the 4017 you can assemble a wide-range 10-Hz to 1-MHz synthesizer. You can achieve the same result by using programmable counters (*e.g.* 4522, 4018, etc.).

Pulse Frequency Modulator. The vco section of the 4046 can be used to make a simple pulse-frequency modulator which can be adjusted to provide a carrier frequency of 1 MHz or more. A simple pulse-frequency-modulated (pfm) lightwave voice transmitter, complete with a microphone preamp designed around a 3130 BiMOS op amp, is illustrated in Fig. 6. This circuit will also work with a 741 or other standard op amp. (Omit *C1* if you substitute op amp for the 3130 that has an internal compensation capacitor.)

With the values shown for *C3* and *R5*, the vco oscillates at a carrier frequency of about 100 kHz. This, and the circuit's modulation bandwidth, ensures reasonably good transmission of audio-frequency signals. The frequency-modulated signal drives an LED through *Q1* with *R6* limiting LED current.

The easiest way to test this circuit in conjunction with the receiver described next is to disconnect the microphone from *R1* and connect the output of a transistor radio to *R1* through a 0.1-μF capacitor.

Pulse Frequency Demodulator. Figure 7 shows a receiver system suitable for detecting and demodulating the pfm signal from the transmitter of Fig. 6. In operation, the infrared signal from the transmitter LED is detected by a phototransistor and coupled into a 3130 BiMOS op amp. This is the same op amp used in the transmitter and it, too, may be replaced with a 741 or other standard op amp. (Don't forget to omit *C2* if you use a 741.)

The amplified signal from the 3130 is ac-coupled via *C3* to the phase comparator input (pin 14) of a 4046. The vco is adjusted by *R5* and *C4* to create a center frequency identical to that of the transmitter (about 100 kHz). Components *C5* and *R7* form the loop filter that determines capture range. In this case, the resistor normally placed in series with the loop filter capacitor (see Part 1) has been omitted. This greatly simplifies the formula for determining the loop capture range:

$$f_c = \pm(1/2\pi)\sqrt{2\pi f_L/R7\ C5}$$

where f_c is the capture range and f_L is half the frequency lock range or, in this case, the vco center frequency. Substituting the values of *R7* and *C5* shown in Fig. 7 gives a capture range or bandwidth of ± 12.6 kHz.

For best results you should connect a lock detector like the one shown in Fig. 1 to the receiver's demodulator. You can use a single red LED to indicate loss of the signal or a single green LED to indicate acquisition of the signal. I prefer to use both the red and green LEDs for a clear go/no-go signal.

For preliminary tests, disconnect the transmitter's microphone from *R1* and connect a radio to *R1* as previously described. When the transmitter's LED is pointed at the receiver's phototransistor, the 4046 in the receiver should quickly lock onto the signal. You should then be able to hear the demodulated signal by means of an audio amplifier connected to the receiver's output.

If the receiver fails to capture the signal, tune its vco by adjusting *R5* until lock is established. If this fails, check the wiring of both the transmitter and receiver. If you've made no wiring errors, experiment with the radio's volume setting until lock is established.

When the receiver's demodulator has captured the input signal, block the beam and note that the signal is *sharply* cut off. This full-on/full-off reception is characteristic of FM transmission systems. It means that the signal from the receiver's demodulator has constant amplitude as long as the received signal has enough amplitude to be captured by the phase-locked loop.

You may notice that the receiver sometimes faithfully reproduces sound sent by the transmitter even when the receiver's 4046 is out of lock. This usually occurs when the signal level is weak. In such cases, the PLL is so close to establishing lock that the sound quality is unaffected.

Though the transmission range of these circuits is only several inches, external lenses or an optical fiber can substantially improve the range. For best results with free-space links, use GaAs:Si LEDs emitting at 940 nm. Suitable LEDs include the TIL-32 (Texas Instruments), OP-195 (Optron), 1N6266 (General Electric), etc.

Going Further. The 4046 is such a dynamic chip it was easy to come up with more than enough circuits to fill this two-part series. Review some of the books that include information about the 4046 if you intend to make full use of this important chip. For example, every 4046 user should obtain copies of the RCA (CD4046B) and Motorola (MC14046B) data sheets for this chip. RCA's ICAN-6101 CD4046B application note is equally valuable. Both the data sheets and the application note include very useful design equations.

Books that describe the 4046 include Don Lancaster's *CMOS Cookbook* (my best source of 4046 information), *Understanding CMOS Integrated Circuits* by Roger Melen and Harry Garland, and *Design of Phase-Locked Loop Circuits* and *Guide to CMOS Basics, Circuits, & Experiments*, the latter two written by Howard Berlin. All are published by Howard W. Sams & Co. In addition, I've included a few pages on the 4046 in *Engineer's Notebook*, a new book published by Radio Shack. ◇

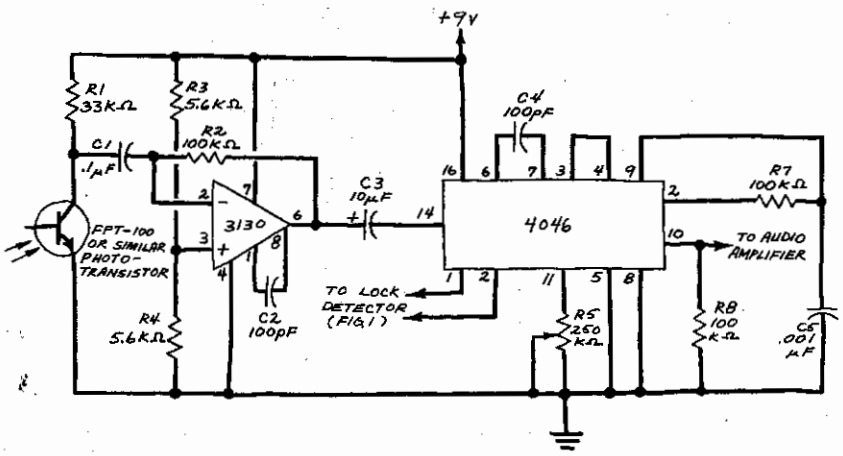


Fig. 7. A receiver system to be used for detecting and demodulating the pulse-frequency-modulated signal from Fig. 6.

Phase-locked loop includes lock indicator

by J.A. Connelly and G.E. Prescott
Georgia Institute of Technology, Atlanta, Ga.

One problem with phase-locked loops is that it's often hard to tell exactly when the loop is locked to the input signal. In many applications, it would be very useful to include a lock indicator in a phase-locked loop to display the state of the loop.

For example, in automatic test equipment, the lock indicator would afford a simple, yet efficient, way to measure the tracking and capture ranges of a phase-locked loop. Also, various low-pass filter configurations could be evaluated easily by sweeping the loop's input frequency range. A straightforward implementation for a phase-locked loop with lock indication is shown in the figure.

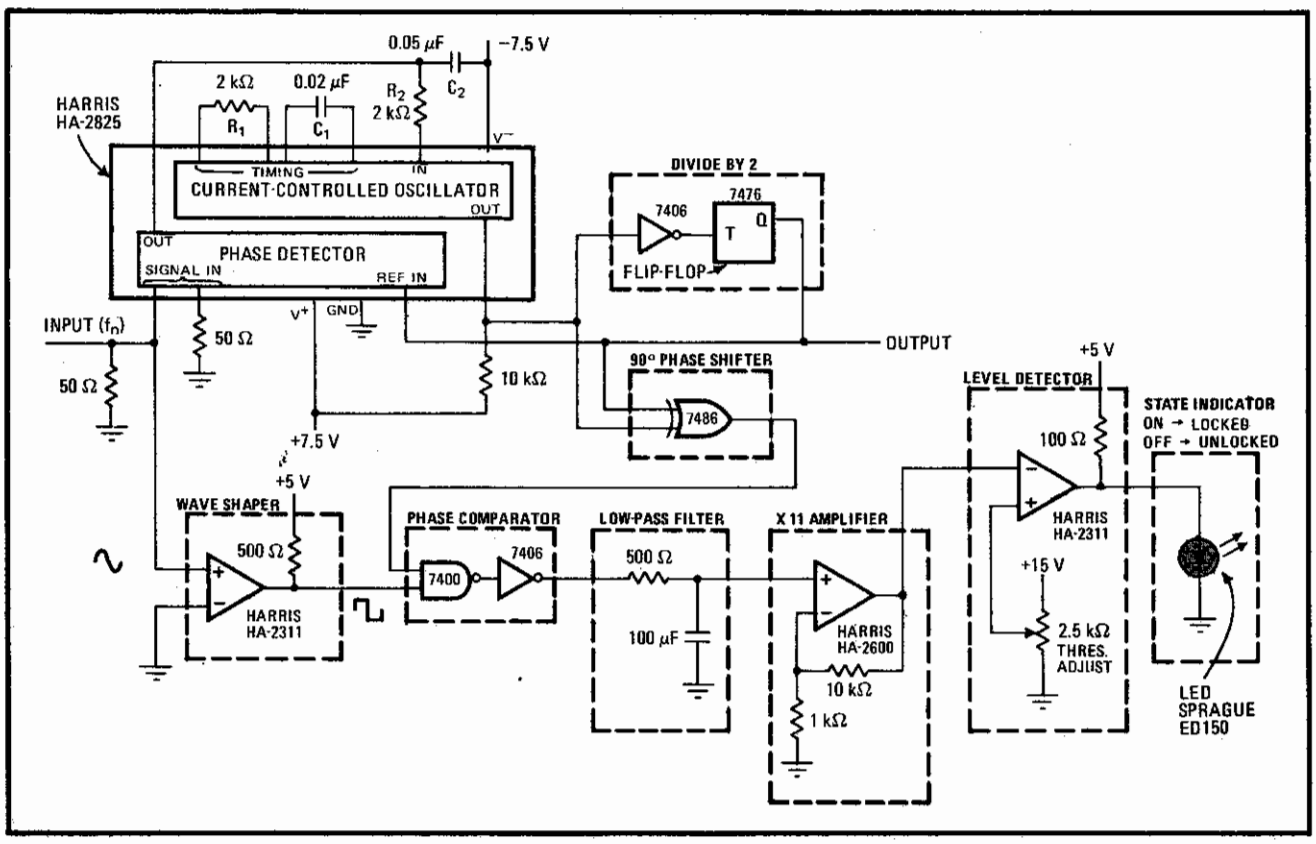
A phase-locked loop can be in its locked state over a range of input frequencies. The center frequency of this range occurs when the frequency of the input signal (f_n) is identical to the free-running frequency of the loop's controlled oscillator (CO). At the center frequency, the output of the CO will be shifted by 90° with respect to f_n. The CO frequency will track variations in f_n until the phase error of the feedback signal with respect to f_n reaches a limit set by the loop gain. For input-frequency variations beyond this limit, the loop reverts to its unlocked mode of operation, and the CO output returns to its free-running frequency.

In the circuit drawn here, the loop's feedback path is altered by breaking the normal feedback loop and inserting a divide-by-2 network. Since this network halves the CO output frequency, the CO free-running frequency must be doubled to achieve normal loop operation.

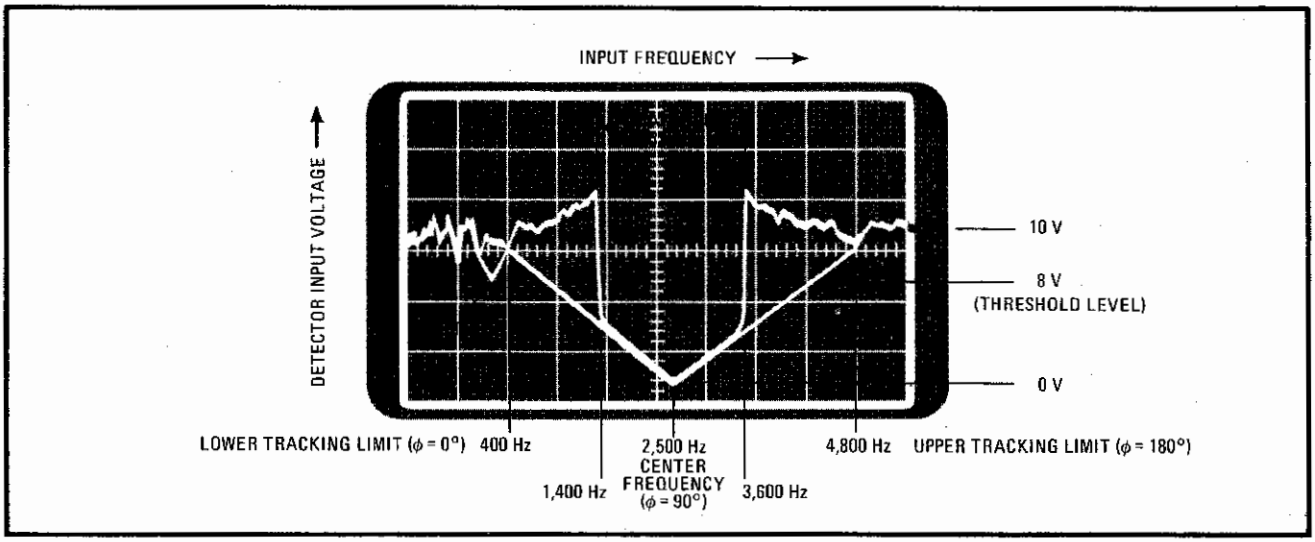
Both the output of the CO ($2f_n$) and the output of the divide-by-2 network feed a phase shifter, which produces a signal that lags the output from the divide-by-2 network by exactly 90°. The signal from the phase shifter is then compared with the input frequency, after this latter signal has been squared up by a wave shaper.

Whenever the input frequency is half the free-running frequency of the CO, the output of the CO will be shifted by 90° with respect to the input. The phase shifter introduces an additional 90° shift, causing the inputs to the phase comparator to be 180° out of phase with each other. Comparing two signals that have the same frequency but that are 180° out of phase produces a constant zero-level output.

However, if the input frequency changes, the inputs



Monitoring loop state. This phase-locked loop has an LED indicator that lights when the loop is locked and goes off when the loop is unlocked. The loop's normal feedback path is opened to accommodate the lock-indicator circuitry. And the free-running frequency of the loop's controlled oscillator must be doubled because of the divide-by-2 network. The circuit's output frequency characteristic is also shown.



to the phase comparator will no longer be exactly 180° out of phase. Instead, they will be skewed somewhat, depending on the phase error between the feedback signal and f_n. Variations in the input frequency cause a series of narrow pulses to be fed into the low-pass filter, which attenuates high frequencies and applies a dc voltage to the level detector.

As the input-frequency deviations from the free-running CO frequency become larger, the phase comparator and low-pass filter produce correspondingly larger dc voltages for the level detector. For a locked loop, the output of the level detector is high, and the LED lock indicator is turned on. When the loop is unlocked, the detector's output goes low, turning off the LED.

For the components shown here, resistor R_1 and capacitor C_1 set the CO free-running frequency at 5,000 hertz, making the input center frequency equal to 2,500 Hz. Resistor R_2 and capacitor C_2 serve as the conventional low-pass filter for the loop. The loop's capture range can be expressed as:

$$\textit{capture range} = \pm(8\pi^2)/[2\pi C_2(R_2+R_{in})]^{1/2}\ Hz$$

where R_{in} is the CO input impedance, which is approximately 500 ohms for the part used here.

The actual output frequency characteristic of the entire loop is also shown in the figure. This waveform is obtained by slowly sweeping the loop's input-frequency range, while monitoring the input voltage to the loop's level detector. The minimum voltage is developed when the loop is locked—the input frequency and the CO output are 90° out of phase. Any input-frequency deviation from this null point will result in a positive dc voltage. The steep edges within the V portion of the characteristic define the capture range of the loop. These abrupt transitions are created as the loop suddenly enters the locked mode from the unlocked condition.

When the input and CO output signals are either 0° or 180° out of phase, the inputs to the phase comparator will be in phase, and the voltage to the detector will be at its maximum level. At this point, the loop becomes unlocked, and the CO and input frequencies are no longer related. The notch appearing at the left end of the V trough is caused by beat frequencies that occur as the loop attempts to capture the input signal. For proper circuit operation over a wide frequency range, the threshold voltage of the level detector should be set lower than the minimum amplitude of this notch.

Through the threshold adjustment, the reference voltage for the level detector can be set as close as is practical to the maximum input detector voltage, without tripping the detector for the unlocked condition. When the input detector voltage drops below this reference level, the output from the detector goes high, lighting the LED to indicate that the loop is locked. In this circuit, the reference voltage is set at approximately 8 V.

If a bank of switchable active filters is used as the loop's normal filter, the lock indicator can serve as a control circuit for changing the tracking and capture ranges of the loop automatically. It does this by switching the loop filter upon loss of track. □

Logic gates and LED indicate phase lock

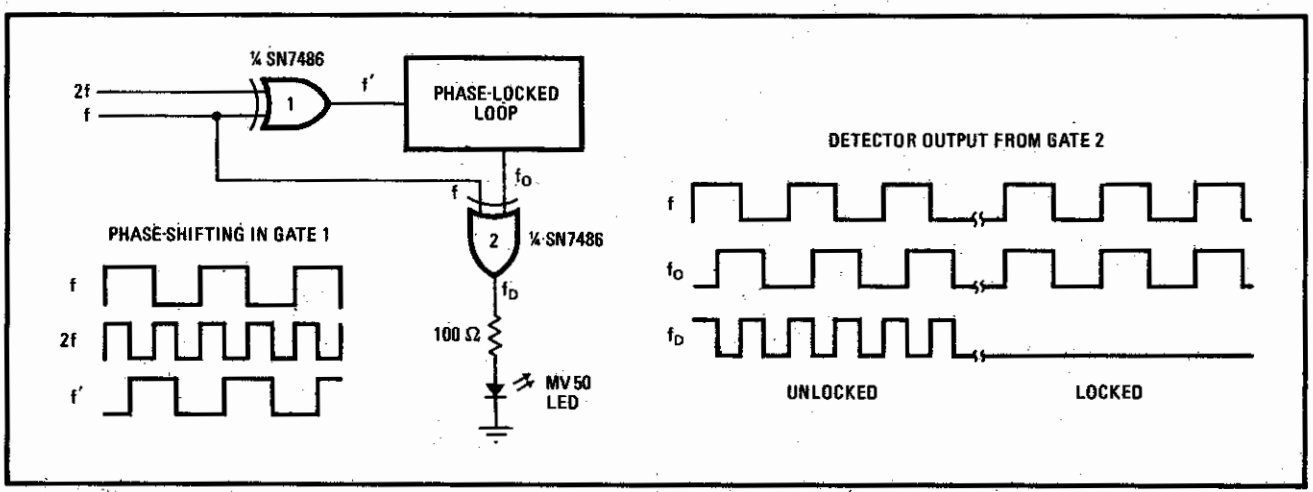
by R. P. Leck
Bell Laboratories, Crawford Hill, Holmdel, N.J.

Phase-locked loops are widely used for signal processing and digital applications such as fm demodulation, tone-decoding, and clock synchronization. If the error signal is accessible, signal acquisition and locking in the PLL can be observed from decrease of error voltage to zero. For integrated-circuit PLLs without an error-signal terminal, however, acquisition and lock can be indicated by two exclusive-OR gates and a light-emitting diode. The LED glows brightly when the input signal is first applied, then dims as the loop signal pulls into synchronism, and it goes out when the loop locks.

If the locked signal from the loop were in phase with the input to the loop, a single exclusive-OR gate would suffice for the indicator. In fact, however, the locked signal lags the input by 90°, so a second gate is needed to introduce an extra quadrature shift on either the input or output signal. As shown in the figure, the phase is shifted by applying frequencies f and 2f to an exclusive-OR gate. In the circuit shown here, the extra 90° is added to the locking signal before it goes into the loop; this procedure is convenient when f is generated by counting down from a master oscillator, because 2f is readily available.

From the square waves at f and 2f, gate 1 develops the 90°-shifted signal f′ that is the input to the loop-phase detector. Gate 2 functions as an auxiliary phase detector, comparing the phase between the loop output, f_O, and the non-phase-shifted input f. The output from gate 2, f_D, drives the light-emitting diode that indicates acquisition and lock.

When the loop is locked and its natural frequency is close to f, the inputs to the detector coincide. The resulting pulse width of the signal present at its output is either tiny or nonexistent, so the LED is turned off. When the loop is out of lock and its natural frequency is far from f, maximum output pulse width is obtained and the LED is turned on at its maximum brightness. As the loop acquires lock, the output-pulse width decreases, decreasing the brightness of the LED. □



Loop monitor. Phase-locked loop has LED monitor that glows brightly when loop is unlocked, dims as loop nears sync, and is dark at lock. Output from loop lags input by 90°; therefore, to permit comparison of output with locking signal, signal is shifted 90° before entering loop.

Engineer's notebook

Phase-locked loops replace precision component bridge

by Vilas Jagtap and Vidyut Bapat
Peico Electronics and Electricals Ltd., Pune, India

For accuracy and repeatability in measuring passive components, a resistor-capacitor bridge is difficult to surpass. But its one drawback is its prohibitively high cost. An inexpensive alternative is a circuit that uses two off-the-shelf phase-locked loops to perform this function accurately to within 0.1% and with a resolution of 0.01%.

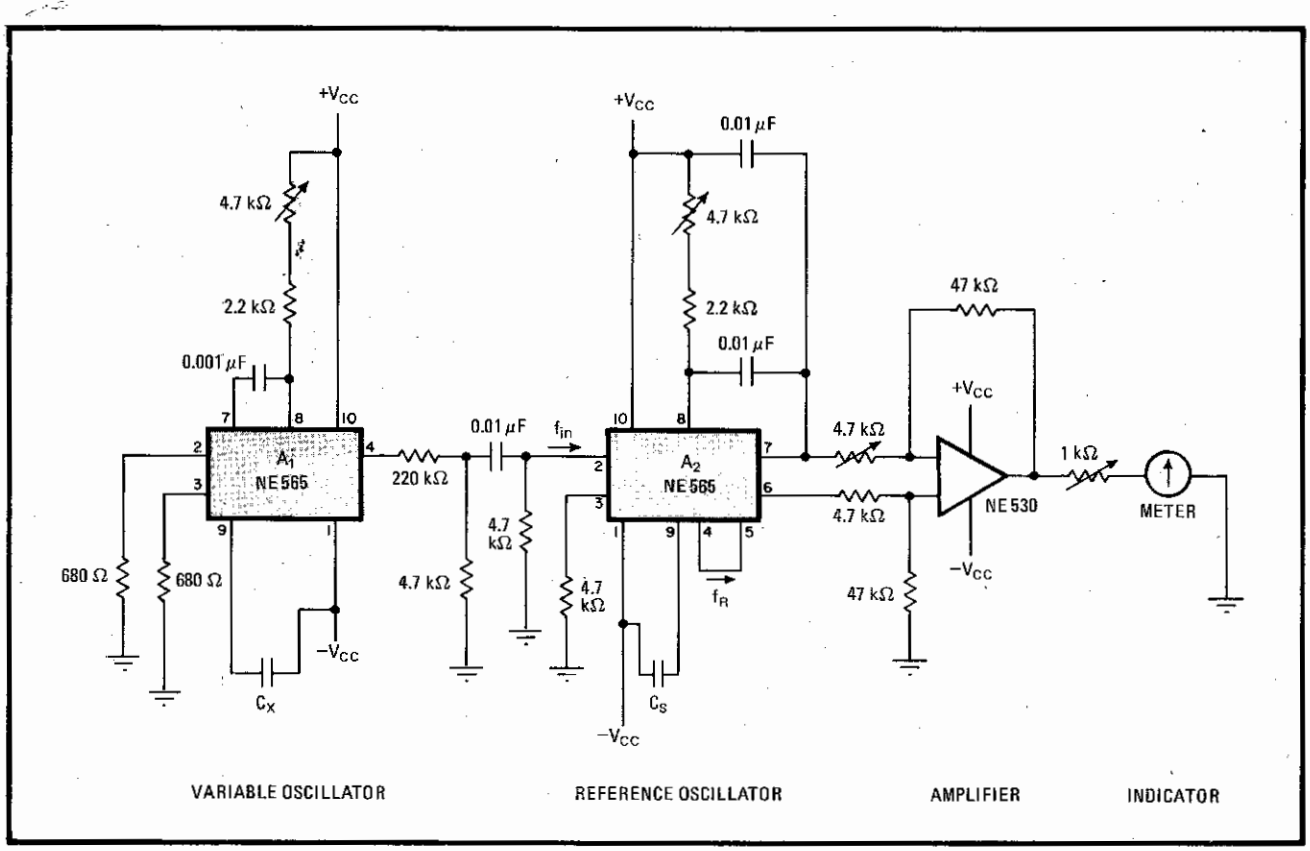
As shown in the circuit, which is configured to measure capacitance, the 565 phase-locked loop, A_1, generates a frequency, f_{in}, corresponding to the component under test, C_x. This signal is then brought to the input of a second loop, A_2, which itself generates a reference frequency, f_{ref}, corresponding to component C_s. The output of A_2 then produces a signal proportional to the difference frequency. The difference frequency, $f_{in} - f_{ref}$, is amplified by the 530 operational amplifier, with the resulting signal applied to a zero-center meter that can be calibrated in terms of the percentage difference between C_x and C_s.

The frequency at which the 565s oscillate is determined by the capacitance between pins 1 and 9 (C_x, C_s) and the resistance between pins 8 and 10 (see the 565 data sheet). A wide range of values may be determined simply by adjusting the 4.7-kilohm potentiometer–2.2-kΩ resistor combination that is connected between these latter pins.

When resistances are compared, only four components need be changed. C_x becomes R_x, C_s becomes R_s, and variable capacitors replace the previously mentioned potentiometers.

Calibration is equally simple in either the capacitor-measuring or the resistor-measuring mode. Since the 565's frequency of oscillation can be within ±10% of a nominal value for a given set of frequency-determining components, both oscillators should initially be aligned by setting $C_x = C_s$ (or $R_x = R_s$). The potentiometers (or variable capacitors) should then be trimmed for a null on the meter. □

Engineer's notebook is a regular feature in *Electronics*. We invite readers to submit original design shortcuts, calculation aids, measurement and test techniques, and other ideas for saving engineering time or cost. We'll pay $75 for each item published.



Matched? Phase-locked loops wired in series indicate percentage deviation between unknown and reference capacitors or resistors. A_2's output represents the difference between a standard and variable frequency, each of which is determined by C_s and C_x, respectively.

LES HADLEY

The Integrated Phase Locked Loop

A system-in-a-chip, the integrated phase-locked loop does an efficient synchronization task in many applications.

THE INTEGRATED phase locked loop (or pll) can rightly be called the "system-in-a-chip." As one might expect, this system or block, may be used in a multitude of different applications, from the reception of both a.m. and f.m. radio signals to the decoding of telephone dialing codes—frequency shift keying (fsk) and pulse code modulation (pcm), as well as many more.

Although the concept behind the phase locked loop has been around since the early 1930's, its use had not been easily realized in system design until the late sixties, when the Signetics Corporation developed the first monolithic, integrated phase locked loop. Prior to this time, its usage was limited, due to the complexity and expense of designing discrete phase locked loop systems. With integration came devices which were predictable in operation, versatile, compact, reliable, and above all, economical.

Les Hadley is an applications engineer with the analog division of the Signetics Corporation.

PLL OPERATION

Let's look into this powerful "system-in-a-chip" and see what makes it tick. In FIGURE 1 you will see the basic block diagram of a phase locked loop.

The input signal comes into the phase comparator, where it is "mixed" with the output signal from an internal reference oscillator, vco (voltage controlled oscillator).

PHASE COHERENCE

It is the primary purpose of the phase comparator to determine the "coherence," or degree of synchronism, between the input signal and the vco. If you have difficulty visualizing the concept of phase coherence, it may help to think of the timing sequence in an automobile ignition system. The spark timing occurs in fixed synchronism, or timing relationship, from the engine. The point in time when the piston reaches top-dead-center is used as a reference, from which the distributor is forced to advance or to retard the occurrence of the spark. It is this precise timing—or *phasing*—relative to the mechanical piston cycle, which is analogous to electrical coherence or synchronism between two signals being compared in the phase comparator (see FIGURE 2).

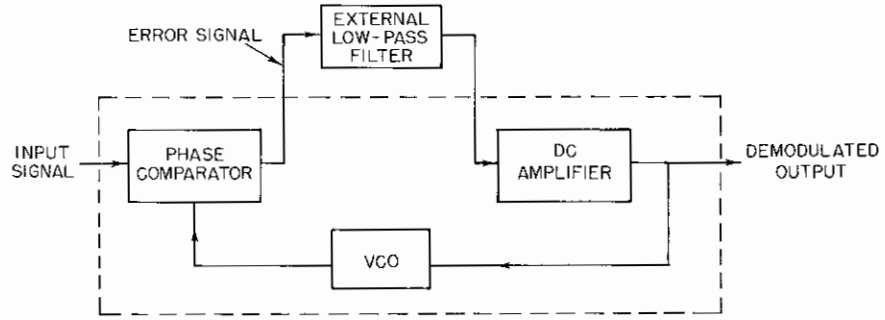


Figure 1. The phase locked loop block diagram.

CAPTURE AND LOCK

When the frequency of the input signal and the vco are equal, and the relative phase angle between them is constant, the phase locked loop is said to be *in-lock*. However, it is quite possible that the incoming signal may initially be different in frequency from the vco. This is where one of the unique characteristics of the pll comes into play, in the phenomenon called *capture*. When the incoming signal frequency closely approaches that of the vco (within what is called the capture range), an *error signal* is generated by the phase comparator, and fed through an external low-pass loop filter. The error voltage is initially a beat note equal to the frequency difference between the vco and the input signal. This varying signal modulates and drives the vco frequency toward the frequency of the incoming signal. The process continues to completion, at which point the beat-note error signal is reduced to a minimum and the vco frequency is equal to that of the incoming signal. Now the loop error signal is simply a dc voltage, proportional to the phase difference between the vco and the input signals. In the analog phase locked loop, once capture is complete, the system will follow slowly varying changes in the incoming signal, as in an f.m. system.

The vco is forced to run 90 degrees lagging with respect to the incoming signal when both signals are the same frequency. Another interesting feature of the pll is that the frequency range over which the system will remain in-lock is always greater than the capture range. Within certain limits, this capture range may be tailored to the needs of the designer, simply by changing the rolloff frequency of the loop filter.

THE EXTERNAL LOOP FILTER

At this point, loop filter design will not be discussed. Loop filters are external to the pll and are in themselves a complete design concept. Reference texts are available on filter design if needed. The combination of proper filter design techniques along with the characteristics of a pll combine to make a pll a very effective electronic filter. The filter design does permit some variations in the capture and lock characteristics of the pll. The ability to control the capture range enables the pll to selectively filter out unwanted signals which are outside the capture range and to latch on to those that are within. These principles are used for detection and recovery of various types of electronically coded information.

FIGURE 3 is a graphic representation of the capture and lock process, along with the respective phase comparator output signals.

In FIGURE 3(A), as the input frequency is swept toward the free-running frequency of the vco, ω_o, from a point below, capture occurs at ω_1. As the input continues to sweep upward, the vco is forced to run at higher and higher frequencies until a point is reached, ω_2 where the loop runs out of range (ability to track the incoming signal), breaks lock, and returns to the free-running frequency of the vco. In FIGURE 3(B), the conditions are reversed and the input sweeps down from a frequency above ω_o. The symmetry of the capture-and-lock range around the center, or free-running, frequency is characteristic of

Figure 2. The phase comparator determines the phase angle between a coherent input signal and the internal reference oscillator.

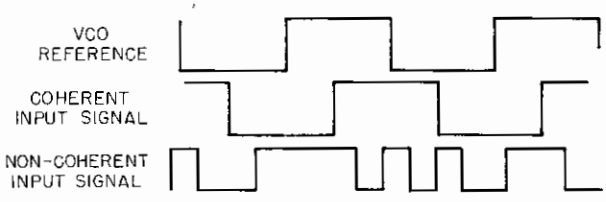
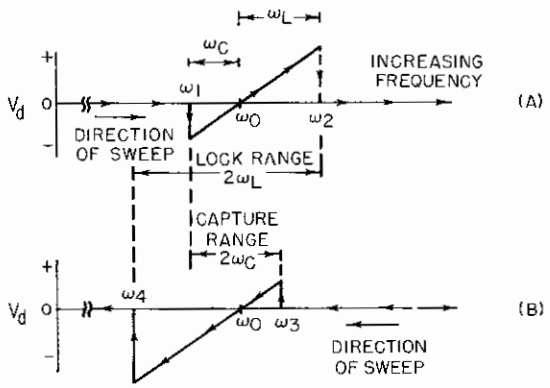


Figure 3. The capture-and-lock operation. Typical pll frequency-to-voltage transfer characteristics



ω_o = *Free-running frequency of the vco (internal reference oscillator.*
ω_1 = *Lower capture frequency.*
ω_3 = *Upper capture frequency.*
ω_2 = *Upper lock frequency.*
ω_4 = *Lower lock frequency.*
$2\omega_C$ = *Capture range.*
$2\omega_L$ = *Lock range.*
V_D = *Phase comparator output voltage.*

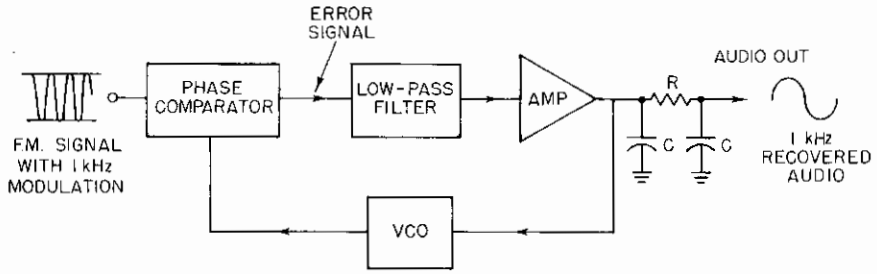


Figure 4. An f.m. demodulator block diagram.

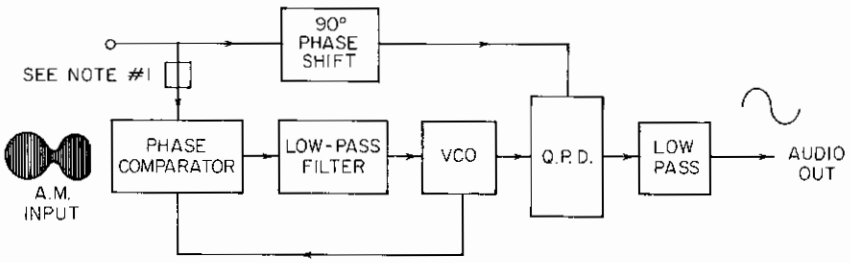


Figure 5. A pll a.m. synchronous detector block diagram. Note 1. The 90 degree phase shift network could be placed here instead (as in Figure 6).

an analog pll. Again, it should be remembered that the loop filter characteristics only affect the capture range and have no effect on the lock range. The actual phase difference between input signal and vco over the whole lock range can vary between 0 degrees and 180 degrees.

BASIC CHARACTERISTICS OF THE PLL

So far, we have covered in brief form some of the major operating principles of the pll. Before going into specific applications, let's summarize the basic characteristics of the pll.

1. The pll is a closed loop system which converts frequency and/or phase differences between an "unknown" incoming signal and a known reference into an error signal, which causes the *known reference frequency* to become synchronized to the unknown frequency.
2. Once capture has been achieved, the pll will follow slowly varying frequency changes in the unknown carrier instantaneously, thereby reproducing wave shapes with minimum distortion.
3. The pll can be controlled by external loop filter designs.
4. The pll is a stable system (single pole) and will not operate in an unstable mode unless poor system design techniques (specifically with regard to filter design) are employed.
5. The pll is an excellent building block for systems such as:
   a) FM demodulation
   b) AM demodulation
   c) FM Modulation
   d) Frequency synthesis
   e) Frequency shift keying (fsk) modems
   f) Pulse code modulation (pcm) techniques, etc., etc., et al.

SYNOPSIS OF AVAILABLE PRODUCTS & THEIR GENERAL USAGES

The following tables illustrate the wide range of pll's available, their general characteristics, and typical applications in which they will probably be found.

A.M. DEMODULATION

Less obvious is the use of the pll to demodulate amplitude modulated signals. This is the synchronous converter, or *synchrodyne*, first tried in the 1930's. Its use was more a theoretical novelty in the days of early vacuum tube technology, however, and the synchrodyne receiver was easily surpassed by the reliable *superhetrodyne*. The problem was stability. A local oscillator had to be precisely tuned to synchronize with the incoming a.m. carrier. The incoming signal was mixed and the product filtered to provide audio directly when the oscillator was exactly tuned. If the local oscillator was a little off, the output was a "hopeless garble."[1]

THE PLL AS AN A.M. DEMODULATOR

By making use of a 90 degree phase shift network and an extra quadrature phase detector (QPD), amplitude-modulated signals may be demodulated. Circuit simplicity makes this an attractive approach to certain signalling applications. It is not meant to be an alternative to the superhet receiver in broadcast reception, but it is ideal for low frequency signalling, such as WWVB reception, and carrier link tone detection.

THEORY

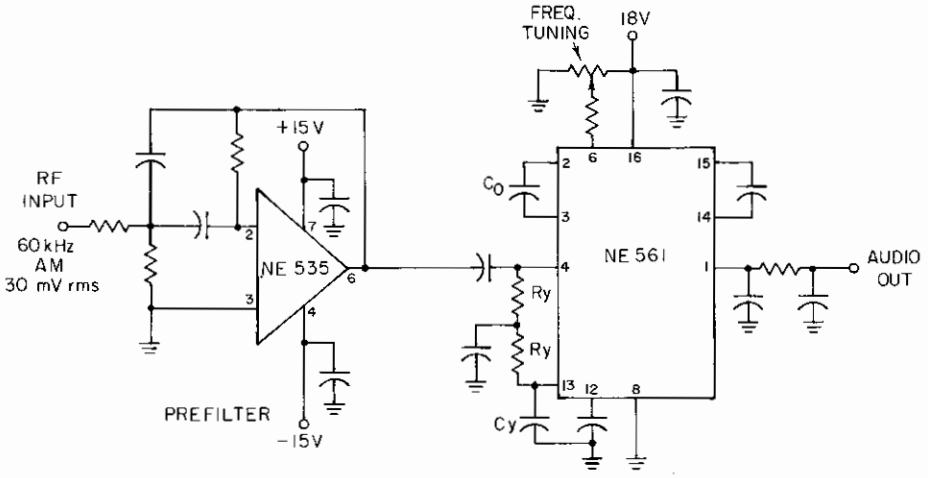
The pll a.m. detector differs in principle from the standard phase locked loop in that it requires two phase comparators. The second phase comparator is called the *quadrature detector* (or QPD) since the signal from the

Figure 6. A synchronous a.m. converter.

$$C_y = \frac{1.3 \times 10^{-4}}{F_0\ (H_z)}$$

$$F_y C_y = \frac{1}{2\pi F_0}$$

$$C_0 = \frac{300pf}{F_0\ (MH_z)}$$



a.m. input has been shifted 90 degrees relative to the main phase comparator. The block diagram shows the difference, compared to the standard pll, which detects f.m.

F.M. DEMODULATION

With the previously mentioned characteristics of the pll, let's apply the pll to an f.m. system, remembering that an f.m. signal consists of a carrier frequency with a modulating frequency superimposed (and this variation is small, less than 0.1 per cent).

In FIGURE 4, the following sequence occurs:

A. The f.m. carrier (10.7 MHz for an i.f. frequency) is compared to the internal reference oscillator. Since the known purpose of this particular pll is as an f.m. demodulator, the internal oscillator is set reasonably close to 10.7 MHz. The capture range of the pll compensates for variations due to temperature, component tolerance variations, voltage variations, etc.

B. Within a short period of time from the application of the f.m. signal (typically less than 10 cycles of the carrier or approximately 1 microsecond), the pll will lock onto the f.m.-i.f. carrier (10.7 MHz).

C. Once the pll has locked onto the carrier, any variation in the system will be tracked instantaneously (as long as the system is within its lock range). The audio-frequency variation becomes an "error signal," and is what appears at the system's output.

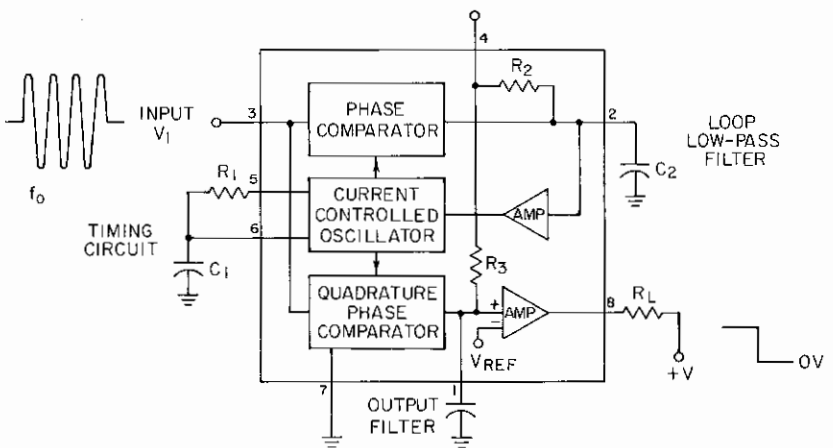
At this point mention should be made of the major difference between f.m. and a.m. demodulation. The f.m. demodulator operates as a function of the cosine of the error phase that is generated. The a.m. demodulator operates as a function of the sine of the error phase that is generated. Therefore, for f.m. demodulation, a 90 degree "error" angle is desirable, while a zero degree "error" angle is needed for an a.m. demodulation system. The additional phase comparator in the a.m. chip supplies the required phase shift (90 degrees).

CIRCUIT OPERATION

The circuit shown in FIGURE 6 is designed to operate at 60 kHz with an a.m. modulated signal. The NE 535 op amp is used to provide an MFB bandpass filter to improve selectivity and signal-to-noise. The signal from the filter feeds pin 4 of the NE 561 (the QPD), and in addition is phase-shifted 90 degrees and fed to the main phase comparator. Values of R_y and C_y may be calculated using the equations given. The center frequency is set by C_0 and fine tuning is accomplished by the 5k pot connected to pin 6. The capacitor across pins 14 and 15 is the loop filter. Its value determines the capture range, as discussed previously. The output pi filter at pin 1 is optimized for an audio bandpass of approximately 5 kHz.

A signal-to-noise ratio of better than 40 dB is possible for 30 mV rms input at 50 per cent modulation.

Figure 7. A pll tone decoder.



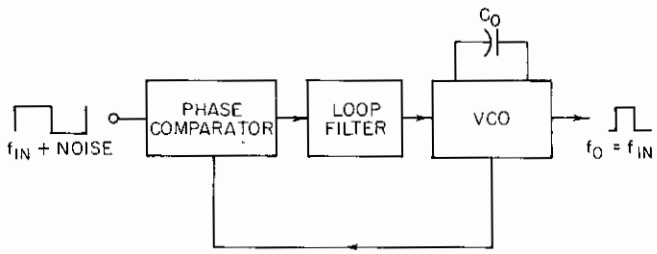


Figure 8. Signal regeneration and noise elimination.

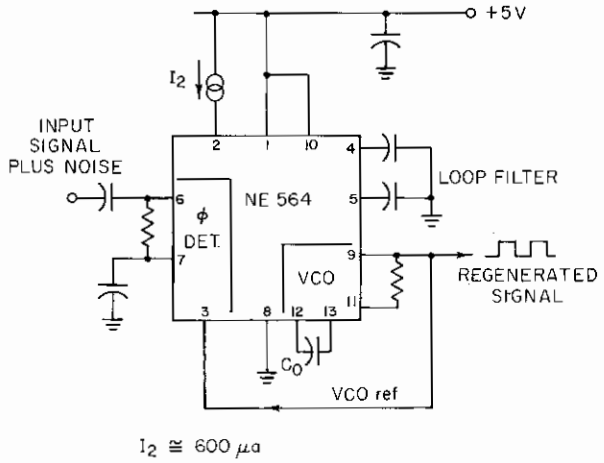


Figure 9. The noise filter circuit.

TONE DECODER

The tone decoder receives wide attention in the telephone industry, where it is valuable in all sorts of tone-signaling circuits. The output of the tone decoder is a d.c. logic level suitable for energizing relays or gates which automatically connect signal lines. The tone decoder uses two phase comparators in the loop to obtain lock information. Again, the second comparator is referred to as a *quadrature detector.* The tone decoder can be used as a tone burst a.m. detector. The linear range of the NE 567 tone decoder is limited and its functionality as anything other than a tone decoder is limited. An excellent application of this device is as a dual-tone, multiple-frequency (DTMF) decoder for use with telephone touch-tone signals. (*Touch-Tone* is a registered trade-mark of the Bell Telephone System.)

THE NE 567 TONE DECODING CIRCUIT

In the circuit shown in FIGURE 7, the NE 567 is used to detect tone signals within its capture range, which may be as narrow as ±5 per cent of the center frequency. Center frequency is determined by the vco free-running frequency. This in turn is set by the values of timing components R_1 and C_1. If a center frequency of 1 kHz were desired, for example, a value of C_1 equal to 0.1 μf would suffice. Note that the timing circuit (R_1C_1) is the heart of the circuit frequency accuracy and stability; therefore, quality components should be used. Capacitor C_1 should be a mylar or polystyrene device. The output is capable of sinking 100 milliamperes and goes low when a tone is received. Tone control links using a.m. or f.m. transmissions over radio, fibre optic or wire line are possible.

In essence, the normal pll vco output signal lags the incoming signal a nominal 90 degrees. The main phase comparator is referenced to this phase differential and is a cosine function; thus, its output is a null, or zero, when the pll is in-lock. In order for the QPD output to be a maximum when the pll is in-lock, an additional 90 degree phase shift is necessary, resulting in an output which is now directly proportional to input signal amplitude.

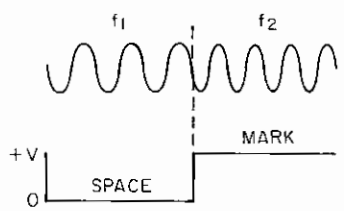


Figure 10. Frequency shift conversion. The carrier frequency is shifted down or up from its center frequency.

Figure 11. A pll with filter for fsk applications.

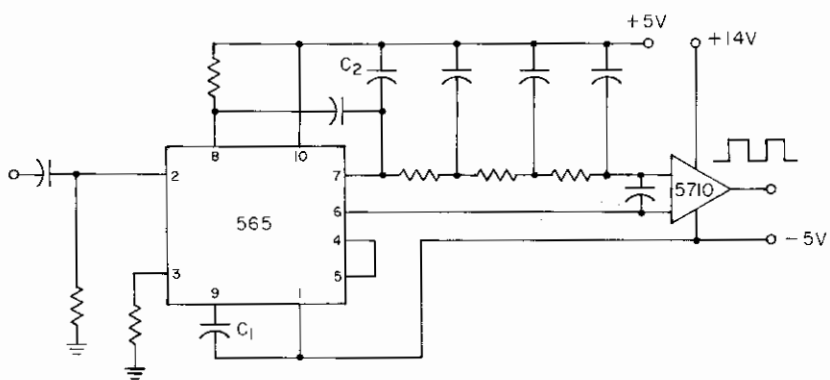
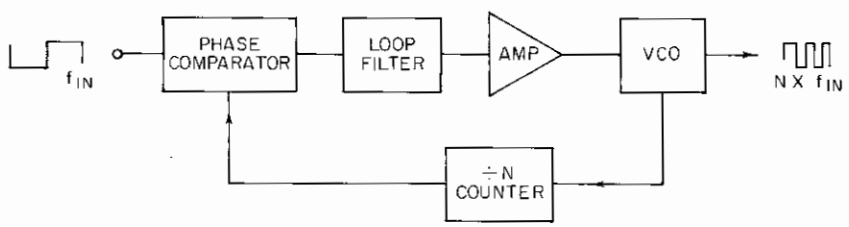


Figure 12. A pll frequency synthesizer block diagram.



Signetics Number	Upper Freq. (MHz)	Max. Lock Range (% F_0)	FM Distor-tion	Output Swing ±5% Deviation (Volts P.P.)	Center Frequency Stability (PPM/°C)	Frequency Drift/W Supply Voltage (%/V)	Input Resist-ance	AM Output Avail.	Typical Supply Current (mA)	Supply Voltage Range (Volts)
NE560	30	40%	.3%	1	±600	.3	2k**	No	9	+16 to +26
NE561	30	40%	.3%	1	±600	.3	2k**	Yes	10	+16 to +26
NE562	30	40%	.5%	1	±600	.3	2k**	No	12	+16 to +30
NE564	50	30+			±200++					+5 to +10V
NE565	.5	120%	.2%	.15	±200	.16	5k	No	8	±6 to ±12
SE565	.5	120%	.2%	.15	±100	.08	5k	No	8	±6 to ±12
NE567	.5	14%	5%*	.20	35±60	.7	20k**	Yes*	7	+4.75 to +9
SE567	.5	14%	5%*	.20	35±60	.5	20k**	Yes*	6	+4.75 to +9
NE566	.5	N/A	.2%	30%/V***	±200	.16			7	+12 to +26
SE566	.5	N/A	.2%	30%/V***	±100	.08			7	+12 to +26

*The 567 a.m. and f.m. outputs are available, but are not optimized for linear demodulation
**Input biased internally
***Figure shown is vco gain in percent deviation per volt
+With external control current
++@ 500 kHz

General Device Characteristics: High selectivity; noise immunity; bandwidth control; reference oscillator control; wide voltage operating range; wide frequency range; low power consumption.
These properties are accomplished with the use of very few peripheral components.

Table I. A quick-look guide to analog pll's.

NOTE—On Table I, don't overlook the General Device Characteristics listed below the tabulation.

NOISE FILTER

The pll may be used to lock on to a signal which is nearly buried in the noise. Once locked, the loop filter integrates out the noise pulses and the vco output provides a "cleaned up" version of the original CW signal (see FIGURE 8).

FREQUENCY SHIFT CONVERSION

Closely related to linear f.m. detection using the pll is the method of detecting digitally-encoded data signals which use fixed frequency shift keying or modulation techniques. Systems using this form of communication have been in use since vacuum tube days for the transmission of teletype signals. More recently, similar techniques are being used in computer modems.

The principle consists of having a center or carrier frequency which is frequency-shifted a fixed number of cycles above the center frequency for a *mark* and an equal number of cycles below f_0 for a *space*.

Early systems used selectively tuned L-C filters to detect fsk signals. FIGURE 11 shows a circuit incorporating the NE 565 as an fsk converter. Typically, the signal frequency is shifted ±5 to ±10 per cent for mark and space conditions with data rates of 300 BAUD (300 mark-space combinations per second, or 150 Hz). The signal is transmitted over wire line or radio link and fed into the NE 565 at a

Table II. Typical applications of phase locked loops.

Application	Device Type	Comments on Selection
Standard FM Demodulation	560, 562, 565	These are optimized for standard FM dev. of 75 kHz
AM Demodulation	561	The only PLL capable of synchronous operation
Low Freq. PLL Modems, etc.	565	Operates up to 500 KHz
High Freq. PLL CATV, Video, etc.	564	Operates up to 50 MHz
FSK (Telecomm, Modems)	564* 565	*Needs no external filtering
Modulator (Low Frequency)	566	This is a VCO
Modulator (High Frequency)	564, 562	The output of oscillator is available.
Single 5V Supply Operation (TTL Level Compatible)	564	The only one available
Freq. Synthesizers	564	The divider network can be TTL