Discriminator computes frequency differential

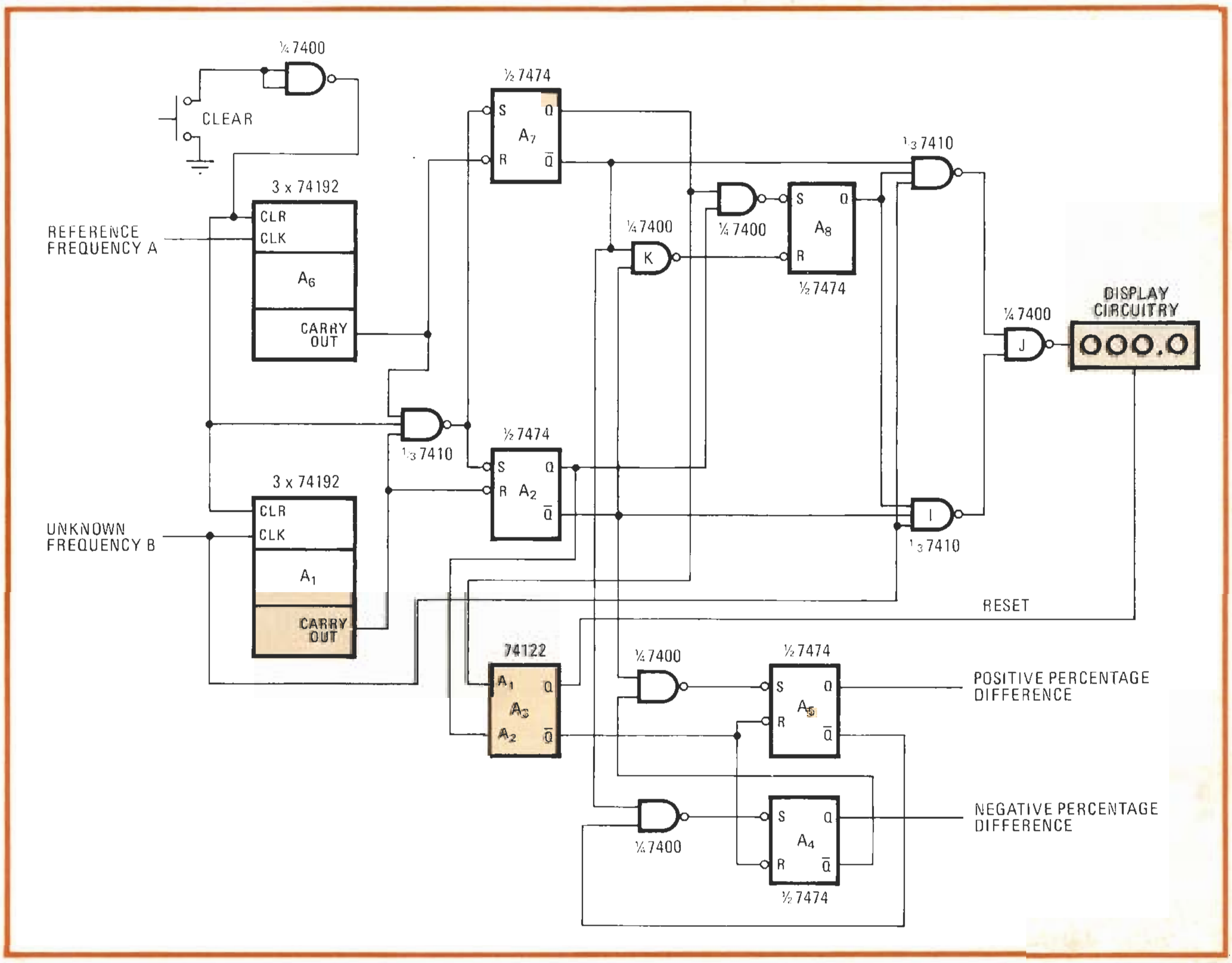
by T. J. John
Meerut, Uttar Pradesh, India

This circuit computes the percent difference of two frequencies to 0.1% without needing an accurate, crystal-controlled timebase. It is useful in industrial applications that convert a process variable into a train of pulses in order to monitor that unknown quantity.

The circuit finds $\pm d = 100(p_x - p_r)/p_r$, where d is the percent difference, and p_x and p_r are the number of pulses counted from an unknown and a reference source, respectively, in a given time. By making p_r equal to a decade multiplier of 10^n for any general n, the first equation becomes $\pm d = (p_x - 10^n)(10^{2-n})$, where $p_x - 10^n$ is the difference between the number of pulses generated by the unknown source and the 10^n pulses generated by the reference, and 10^{2-n} indicates the position of the decimal point. Thus the equation is reduced to a form where it can be solved in hardware with off-the-shelf logic elements.

Note that for an accuracy of 0.1%, the value of n must be 3. Therefore, three cascaded decade counters must be used at each input for counting up to $10^3 = 1{,}000$, as shown in the figure.

A system clear initializes the counters to 0 and presets several circuit flip-flops. The carry output of the last 74192 in each chain then generates a negative-going pulse each time it counts to 1,000. Assuming a positive difference between unknown frequency B and reference frequency A, A_1 reaches 1,000 first and resets flip-flop A_2. A_2's $\overline{Q}$ output then fires one-shot A_3, whose on-time must be small compared to the period of the unknown



Comparison. The circuit for finding ± (A – B)/A, in percent, needs no frequency standard and it can be built with standard logic elements. Results are directly displayed. Accuracy of measurement is 0.1%, obtained by using three cascaded decade counters at each input.

frequency measured. Flip-flops A_4 and A_5, the polarity-difference indicators, are then reset.

The preceding actions permit the 1,001st pulse counted by A_1 to be passed directly from the input to the display-counting circuit through enabled gates I and J. For each pulse appearing at the output of J, the counter is advanced by 1, starting from the least significant bit displayed. When the reference-frequency counter, A_6, reaches 1,000, A_7 is reset. A_8 in turn is reset through gate K and gate I is disabled. At that time, the display will directly indicate the magnitude of the difference between frequencies A and B, in percent. Because A_1 reaches 1,000 before A_2, A_5 is set and will indicate there exists a positive frequency difference between B and A.

In the event a negative percentage difference is measured, A_2 reaches 1,000 first. A sequence of events similar to those discussed previously then occurs, but with the upper portion of the circuit becoming active first, and with the end result that the negative-difference indicator, A_4, is set. □

One-shot/flip-flop pairs detect frequency bands

by Edward E. Pearson
Opelousas, La.

A retriggerable monostable multivibrator and a type D flip-flop can form a simple reliable frequency comparator that senses if an input frequency is greater than or less than a predetermined reference. Connecting additional comparators in parallel, together with AND logic, permits the detection of input frequencies that fall within selected bands.

Both the one-shot and the flip-flop are wired for positive edge triggering. Each input pulse causes the monostable's output to go high for the period of its preset timing interval. The flip-flop is triggered simultaneously, but its output is determined by the state of its D input at the time of trigger threshold.

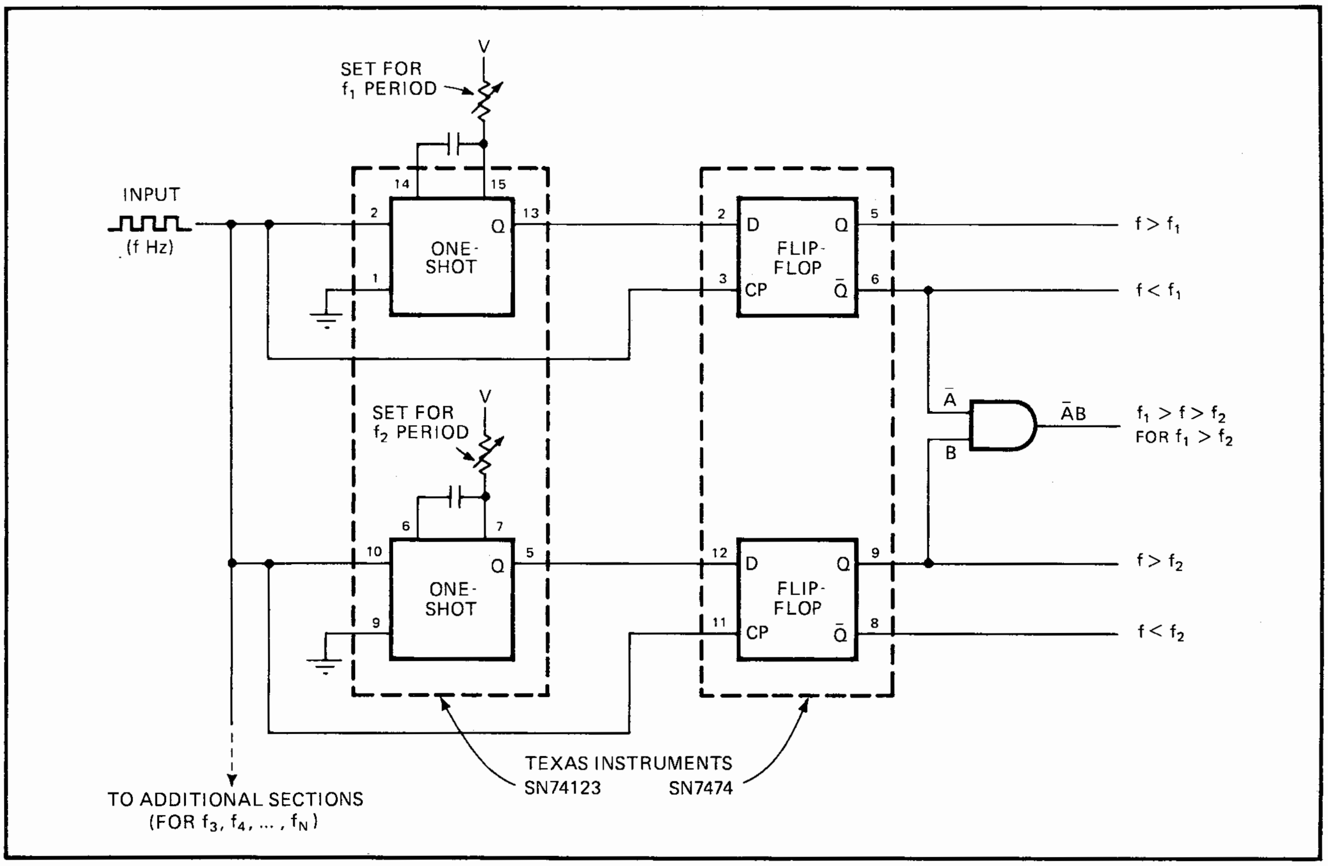
If the period of the input frequency is shorter than the preset timing of the monostable, a constant high level will be present at the D input, forcing the flip-flop's Q output to remain high. If the input frequency period becomes greater than that of the monostable, the D input will go low prior to the next incoming trigger. The flip-flop's Q output then goes low and remains low until the input period becomes shorter than that of the monostable.

To determine whether an input frequency (f) falls between two known frequencies, f_1 and f_2, two one-shot/flip-flop combinations are required, as shown. The top pair of devices detects an input greater or less than f_1, while the bottom pair detects an input greater or less than f_2. The AND gate provides a high output when the input frequency lies inside the preset band (less than f_1 or greater than f_2, if f_1 is greater than f_2). This detection scheme can be expanded to include any desired number of segments within the operating passband.

The frequency band detector also has an inherent memory function that could be particularly useful in control applications. When the input signal terminates, for example, with a tone burst, no trigger is available to the flip-flops, and all outputs remain static until the input signal returns.

Although the detector responds only to the period of the input signal and does not require the input to maintain a specific duty cycle, input pulses must have a rapid rise time. All trigger thresholds must be reached within an interval that is appreciably less than the monostable's propagation delay time. Circuit speed is limited only by the setup and hold performance of the components being used. □

Sensing frequency. Retriggerable one-shot and flip-flop compare frequency of input to preset reference frequency. To form frequency-band detector, two frequency comparators and AND gate are needed. Depending on period of input pulse train, each one-shot output is high or low. Each flip-flop triggers to level seen by its D input prior to trigger threshold. AND gate output goes high when f falls between f_1 and f_2.



In-range frequency detector has jitter-free response

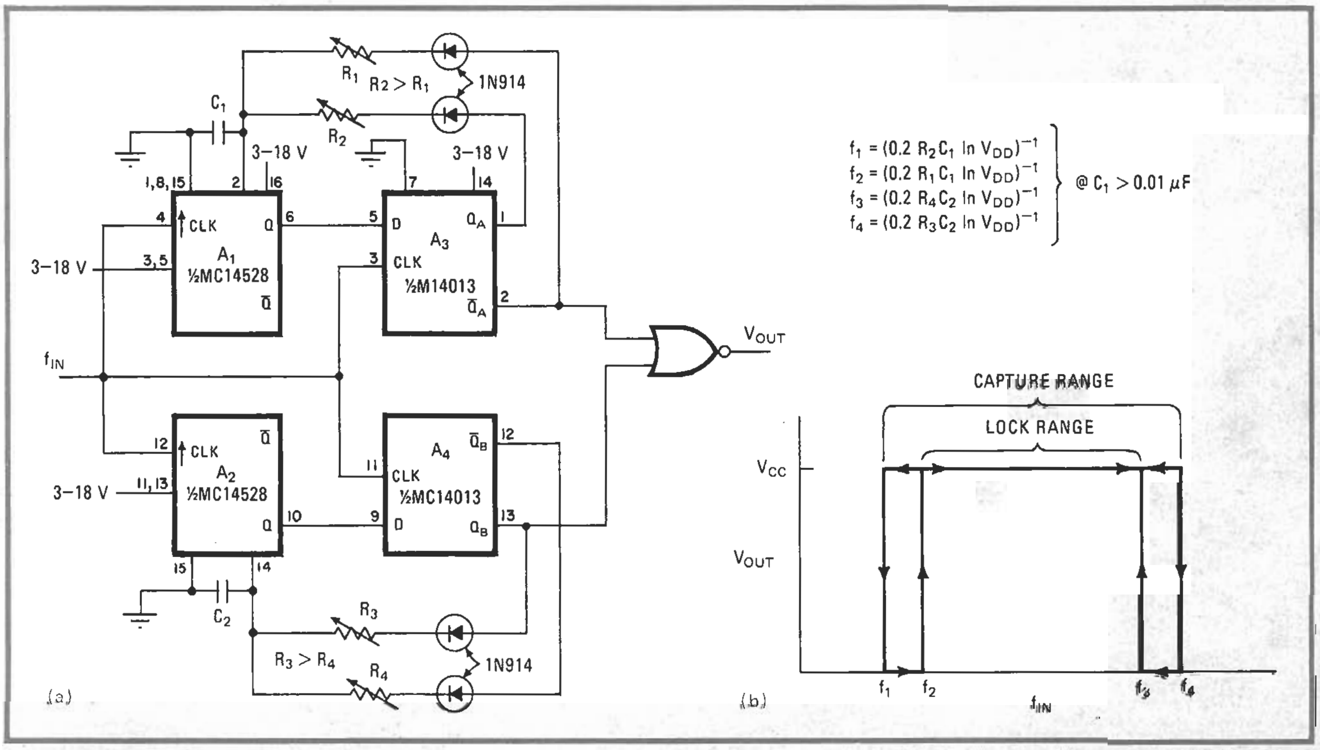
by A. J. Nicoll
Instromedix Inc., Beaverton, Ore.

This simple circuit will detect when an input signal falls within a specified frequency range and is thus ideal for use as an out-of-tolerance alarm or as a rudimentary phase-locked loop. It could also be called unusual, since it uses hysteresis to provide separate lock and capture ranges that eliminate the jitter of the circuit's logic-level output.

The diagram shown in (a) and the hysteresis curve shown in (b) help make the circuit's operation clear. A_1 and A_2 are two retriggerable one-shots. Their pulse widths, and therefore their maximum frequency of operation, are controlled by R_1–R_4. Whether R_1 or R_2 controls the width of A_1 and R_3 or R_4 controls the width of A_2 depends upon the state of the A_3 or A_4 D-type flip-flops.

Assume R_1 and R_4 are the controlling elements as an input signal of arbitrary frequency, f_{in}, arrives to trigger both one-shots simultaneously. The positive transition of f_{in} then fires A_1 and A_2, as shown. The next positive-going transition will trigger both A_1 and A_2 again while clocking the previous output states, which were generated before retriggering, into A_3 and A_4.

If this second transition occurs before either one-shot has returned to its time-out state, a logic 1 will be clocked into its respective flip-flop, changing the state of that flip-flop. Once the flip-flop moves from a 0 to a 1, the pulse width of the one-shot will be controlled by one of the two timing elements, R_2 and R_3.



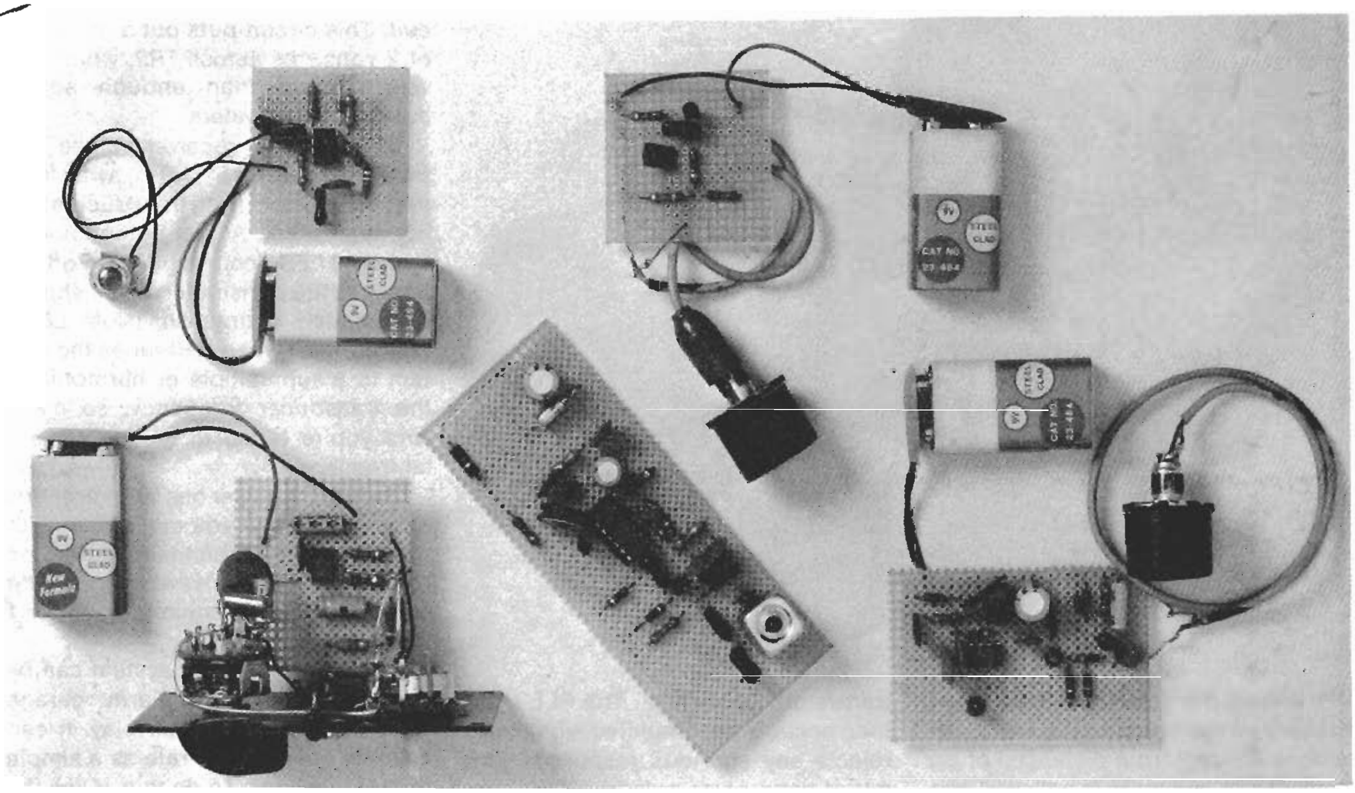
$$
\left.\begin{aligned}
f_1 &= (0.2\ R_2C_1 \ln V_{DD})^{-1}\\
f_2 &= (0.2\ R_1C_1 \ln V_{DD})^{-1}\\
f_3 &= (0.2\ R_4C_2 \ln V_{DD})^{-1}\\
f_4 &= (0.2\ R_3C_2 \ln V_{DD})^{-1}
\end{aligned}\right\}\ @\ C_1 > 0.01\ \mu F
$$

Within limits. Circuit (a) detects whether input signal is within user-set frequency range f_2–f_3 (b). Flip-flops enable selectable hysteresis so that circuit, once locked, will not change state until f_{in} moves below f_1 or moves above f_4. Lock and capture ranges are controlled by R_1–R_4. Hysteresis eliminates jitter that would normally occur at output if f_{in} were near f_2's or f_3's edges.

The curve (b) shows more clearly how the lock and capture ranges are controlled by R_1–R_4, where f_1–f_4 are equal to the reciprocals of the pulse widths determined by C_1–R_1 or –R_2 and C_2–R_3 or –R_4. A_3 will move high when f_{in} rises above f_2, and it will not move back to its initial state until f_{in} falls below f_1. Similarly, A_4 will change from a 0 to a 1 when f_{in} rises above f_4, and it will change back to a 0 only when f_{in} falls below f_3. The amount of hysteresis acting upon f_1–f_2 and f_3–f_4 can be chosen by simply selecting the appropriate resistance values for R_1–R_4.

The NOR gate output moves high when f_{in} is within the set limits of f_2–f_3. It will not move low again until the input frequency falls below f_1 or above f_4. If desired, an OR gate can be used instead of a NOR gate, since both the Q and $\overline{Q}$ outputs are available in D-type flip-flops. ☐

Designer's casebook is a regular feature in *Electronics*. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



EXPERIMENTING WITH PHASE-LOCKED LOOPS

Four simple but useful circuits that will increase your understanding of these versatile 565 and 567 IC's.

BY HERB COHEN

WHEN phase-locked-loop (PLL) integrated circuits began to appear on the hobby market, the experimenter was faced with the same problem always encountered with new devices: what to do with it. If he tried to understand the theory—usually available in abundance—he was clouted with terms like rads/second, capture ratio, lock range, and lag networks. Needless to say, there was an urge to slam shut the book and treat the IC as a "black box"—not really such a bad idea.

Although there have been a number of articles published in various magazines explaining the basics of PLL theory (see "How Phase-Locked Loops Work," February 1975), a "hands-on" session with these IC's will tell you more about them than all the reading you're likely to do. As an example, the 565 and 567 PLL's are so simple to work with and require so few external components that you don't need a stage-by-stage understanding of what goes on inside them to put them to use.

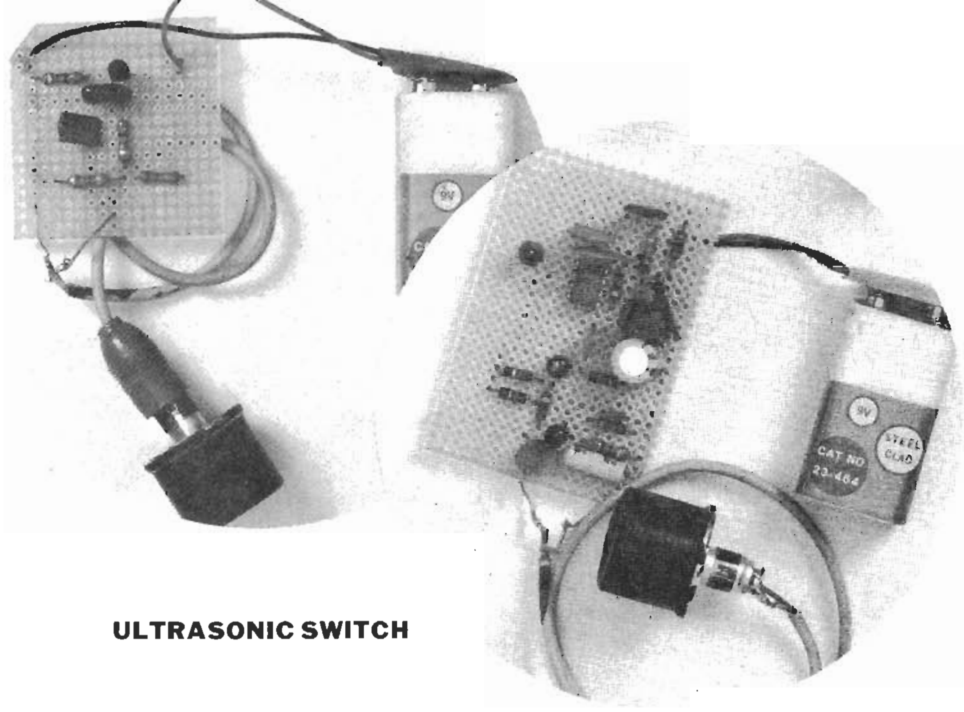
In this article, we describe four simple projects you can build around a pair of commonly available PLL's to give a "feel" for how they perform. Each project illustrates a different aspect of phase-locked-loop technology, and each is a practical circuit you can put to immediate use. Before proceeding to the projects themselves, however, let us first discuss the specific PLL's used in our projects.

Two PLL's. Of the many phase-locked-loop IC's available, the 567 is the only one that is designed primarily for switching applications. When this PLL goes into lock, its output transistor, driven from a quadrature detector, is capable of passing 100 mA of current. This makes the 567 ideal as an SCR or relay driver.

Another unique feature of the 567 PLL is its ability to be driven from a low-voltage (4.5 to 10 volts) power supply at a nominal 10-mA drain. This means that the IC can be powered by a 9-volt transistor battery with good life expectancy. So, although it doesn't have the bandwidth or sensitivity of other PLL's, the 567 is ideal for hundreds of tone-decoder applications in the range from 1 Hz to 100 kHz.

The 565 is a general-purpose PLL IC and is by far the most popular now being used. It exhibits a very wide ±60% locking range and a 1-mV input sensitivity. This PLL is ideal for use as an SCA decoder, which will let you receive the hidden subchannels on FM.

The following four projects are examples of the simplicity and versatility of the PLL IC. The first three are built around the 567, while the fourth—an SCA decoder—employs the 565 PLL. The circuits can be assembled easily on perforated boards or pc boards.



ULTRASONIC SWITCH

Ultrasonic Switch. The simple transmit/receive system shown in Fig. 1 can receive a signal from distances of up to 40′ (12 m) and more in hallways and enclosed areas where the acoustical properties are good. The transmitter is shown in B, while the receiver is shown in A.

Transducers *TR1* and *TR2* in the receiver and transmitter are 40-kHz barium-titanate ultrasonic transducers. Transducer *TR1* in the receiver picks up the sound waves from transmitter transducer *TR2* and passes them to the amplifier consisting of transistors *Q1* and *Q2*. The PLL (*IC1*) then accepts the amplified signal and rejects any spurious responses and out-of-band noise pulses.

Light-emitting diode *LED1* and limiting resistor *R9* are installed in the circuit only temporarily to assist in tuning the system. Once the system has been properly tuned, these components are removed and replaced with the load to be driven (relay, lamp, etc.).

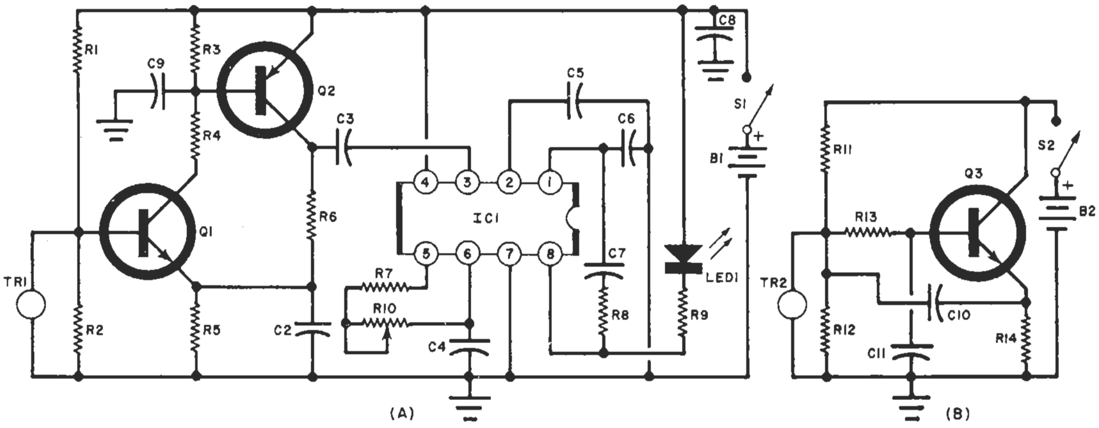
The transmitter shown in B is a Colpitts oscillator configuration that uses transducer *TR2* in the resonance circuit. This circuit puts out a minimum of 2 volts rms across *TR2*, which develops more than enough sound power for the system.

To tune the receiver, place the transmitter about 5′ (1.5 m) away from the receiver with both transducers facing each other. Adjust potentiometer *R10* until *LED1* comes on. Turn off the power to the transmitter; *LED1* should immediately extinguish. (Note *LED1* may light up when *R10* tunes the system to a submultiple or harmonic of the transducer frequency, so make sure you're tuned to the fundamental frequency.)

Once the receiver has been properly tuned, the range you can obtain with this system is dependent mainly on room acoustics. However, you should be able to obtain a minimum of 20′ (6.1 m) of range.

The ultrasonic relay system can be used as an intruder alarm, garage door opener, or remote relay. It can even be made to operate as a simple motion detector. To do this, place the transmitter and receiver about 10′ (3 m) apart and with their transducers facing the same wall in a room. The LED in the receiver should come on; if it doesn't, move the transmitter closer to the receiver until it does. Then, move it away until the LED just extinguishes. Now, walk along the side of the room that the transmitter and receiver are facing. As you move, the LED will blink on and off.

Fig. 1. A simple transmit/receive ultrasonic relay.



PARTS LIST

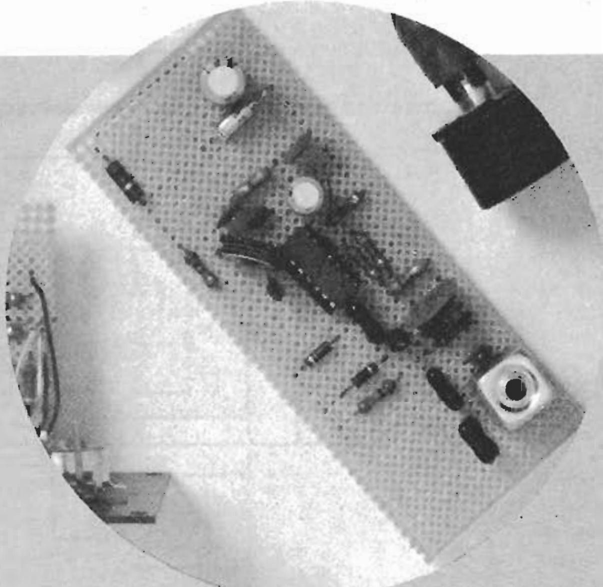
B1,B2—9-volt battery
C1,C6—0.04-µF disc capacitor
C2—5-µF, 10-volt electrolytic capacitor
C3,C4—0.0047-µF disc capacitor
C5—0.1-µF disc capacitor
C7,C10—0.02-µF disc capacitor
C8—100-µF, 10-volt electrolytic capacitor
C9—0.001-µF disc capacitor
C11—330-pF disc capacitor
IC1—567 PLL IC
LED1—Light-emitting diode
TR1,TR2—Ultrasonic transducer (Detectron No. HC1)
Q1—2N4946 pnp transitor
Q2—2N4917 npn transistor
Q3—HEP S0007 npn transistor
The following are ¼-watt, 10% resistors:
R1—180,000 ohms
R2—43,000 ohms
R3,R4—2200 ohms
R5,R13,R14—1000 ohms
R8,R7—2700 ohms
R9—330 ohms
R11—22,000 ohms
R12—47,000 ohms
R10—10,000-ohm miniature potentiometer
S1,S2—Spst switch
Misc.—Battery clips; hookup wire; solder; etc.

shown in Fig. 3, is hard to beat. Just by touching the plate, body capacitance unbalances the circuit and pulls *IC1* into lock. An external signal is normally fed into the PLL *(IC1)* via pin 3 and *C1* and *R1* are used to tune the voltage-controlled oscillator to the input frequency. When lock occurs, the vco adjusts itself to be 90° out-of-phase with the input signal.

With the input signal at pin 3 coming from the output of the vco (pin 5 of *IC1*) through *C4, R2,* and *R3,* the two signals are in-phase with each other and the circuit cannot lock. However, when the touch plate is approached, enough capacitive phase shift is introduced to allow the circuit to lock.

Wiring the jumper into the circuit as shown allows the system to latch in the on position even after your hand is removed from the touch plate. To reset the system to off requires *S1* to be closed momentarily.

SCA DECODER



SCA Decoder. Our final PLL project is an SCA decoder built around the 565 phase-locked-loop IC. This is essentially a 67-kHz FM detector. However, a PLL is a better detector for FM than any of the traditional detector designs because it has the ability to dive 6 dB below the noise level and still lock onto a signal.

In the case of an SCA subchannel where the information is only 10% of the total program power (most of that lost in the audio filtering), the 565 IC's ability to reject noise is an important factor in building a simple and effective SCA decoder.

Capacitors *C1, C2,* and *C3* and coil *L1* (Fig. 4) form a bandpass filter that peaks at 67 kHz and rejects all low-frequency components of the audio signal in an FM tuner. Transistor *Q1* amplifies this signal and passes it to *IC1*. The PLL IC is tuned by *C7, R6,* and *R10*. Since the tuning frequency is also a function of the supply voltage, the IC should be zener-diode regulated.

The demodulated audio signal comes out of the decoder at a 50-mV level. It has a 7,000-Hz audio bandwidth that can hardly be considered hi-fi. This bandwidth, however, is more than sufficient for background music.

The tuning procedure is simple. Connect the output of your FM tuner to the input of the SCA decoder and the output of the decoder to your audio amplifier. Set *R10* to the center of rotation. Scan the FM dial; all you should be able to hear at this point is noise and no stations. An SCA subchannel will appear as a sharp drop in the noise level, accompanied by a distorted music program. Now, adjust *R10* for the best signal-to-noise (S/N) ratio and highest fidelity.

Tune to the weakest SCA subchannel you can find. Adjust *L1* for the lowest possible noise level. The SCA decoder is now ready to use.

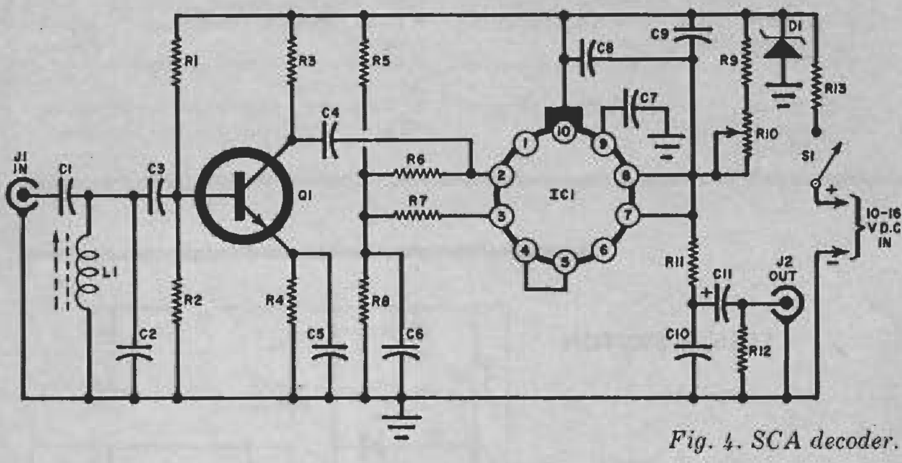


Fig. 4. SCA decoder.

PARTS LIST

C1—220-pF disc capacitor
C2—0.002-μF disc capacitor
C3—330-pF disc capacitor
C4—560-pF disc capacitor
C5,C9,C10—0.04-μF disc capacitor
C6—0.1-μF disc capacitor
C7—0.001-μF disc capacitor
C8—0.001-μF disc capacitor
C11—30-μF, 15-volt electrolytic capacitor
D1—12-volt zener diode
IC1—565 PLL IC
J1,J2—Phono jack
L1—10-mH slug-tuned inductor (Miller No. 9060)
Q1—2N2926 npn transistor

The following are ¼-watt, 10% resistors:
R1—100,000 ohms
R2—22,000 ohms
R3—8200 ohms
R4—1500 ohms
R5—15,000 ohms
R6,R7,R11—4700 ohms
R8—6800 ohms
R9—1000 ohms
R12—47,000 ohms
R10—10,000-ohm, linear-taper potentiometer
R13—47,000-ohm, ½-watt, 10% resistor
S1—Spst switch
Misc.—Battery clip; hookup wire; solder; etc.

Closing Comment. The preceding four projects illustrate only a small portion of the possible applications to which the versatile phase-locked-loop IC can be put. A couple of the projects should be able to suggest other projects of your own. ◆

Experimenter's Corner

By Forrest M. Mims

THE 567 TONE DECODER

THERE ARE many applications for circuits that can be made to respond to a specific tone frequency while ignoring all others. Some of these include radio controlled garage door openers and model airplanes, automatic paging systems, intrusion alarms, communications systems, and highly secure electronic locks.

Over the years, several practical circuits which respond to a specific tone frequency have been designed. Two of the best known are the resonant reed relay, once very popular with radio control modelers, and narrow bandpass active filters using one or more operational amplifiers.

The arrival of sophisticated single chip phase-locked loops (PLL's) a few years ago has made possible a variety of versatile tone-detection circuits, the 567 being designed especially for this role. Supplied in either an 8-pin mini-DIP or TO-5 can, the 567 is available from several sources listed in the Electronics Market-place in this magazine for less than $1.75.

The functional block diagram of the 567 tone decoder is shown in Fig. 1. The circuit incorporates 62 transistors to provide synchronous AM lock detection and a power output stage. In operation, a current controlled oscillator (cco) operates at a frequency determined by external components *R1* and *C1*. This frequency is called the center frequency (f) and is equivalent to 1.1/*R1C1*. Both the input and the cco signals are fed into a pair of phase detectors. When the input frequency falls within the detection bandwidth of the circuit (0 to 14% of f), an output transistor capable of sinking up to 100 mA turns on. The output can directly control miniature lamps, relays, and LED's.

The 567 is an incredibly flexible chip with many different operating characteristics and capabilities. For example, it has a tone detection range of from 0.01 Hz to 500 kHz and will lock onto a signal with an amplitude of only 20 mV rms! Operating voltage ranges from a TTL-compatible 4.75 volts to a high of 9 volts. Standby current consumption is a reasonably low 6 to 10 mA, while activated current consumption without load is 11 to 15 mA.

Experimenter's Circuit. I think the best way for you to relate to the 567 PLL is to try it in an actual circuit, such as shown in Fig. 2. This circuit is a straightforward tone decoder with a built-in variable-frequency oscillator made from a single 555 timer.

The 555 is operated in its astable mode to produce square shaped output pulses. The repetition rate of the 555 is controlled by *R4* and *C5*. Increasing the values of *R4* and *C5* slows the repetition rate, while decreasing

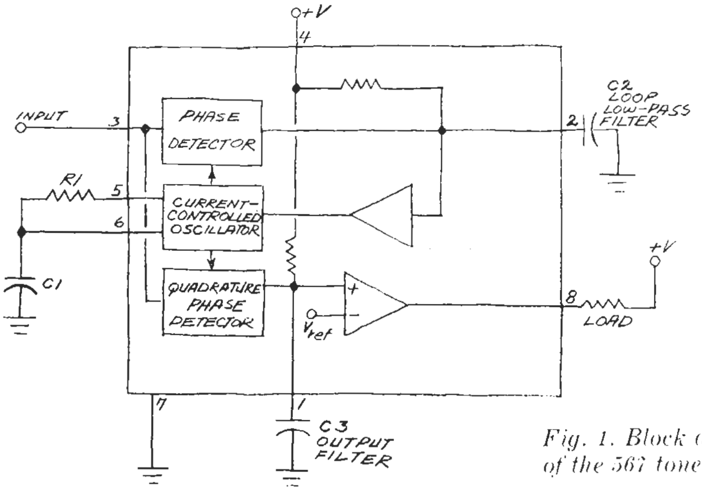
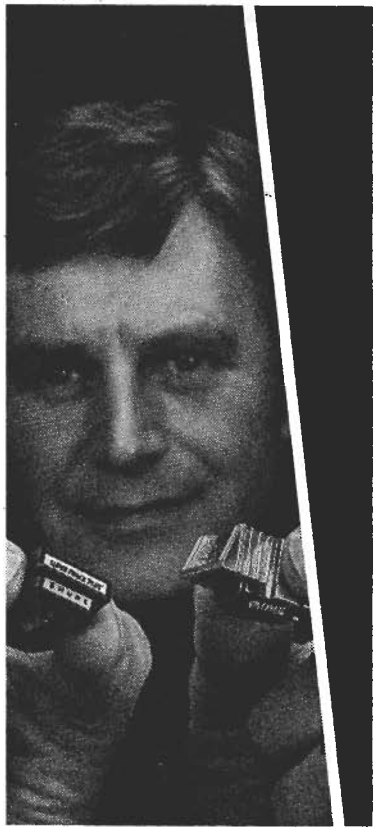
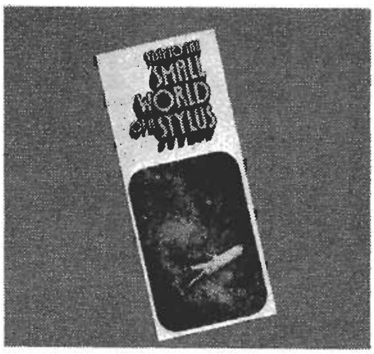


Fig. 1. Block diagram of the 567 tone decoder.





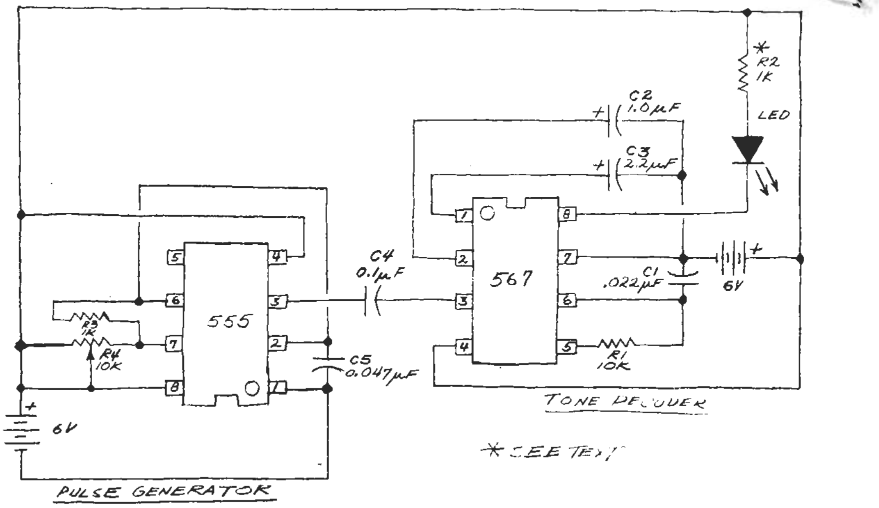


Fig. 2. Tone decoder demonstration circuit.

values speeds up the repetition rate.

With the component values given in Fig. 2, f_0 should be 5000 Hz (1.1/10,000 × 0.022 × 10^{-6}. The test circuit, however, gave an f of 4480 Hz. I measured *R1* with a digital multimeter and found its actual resistance to be 10,320 ohms. This new value gave an f_0 of 4845 Hz, which is within 3% of the predicted frequency, and any error is traceable to the tolerance of *C1.*

After you put the circuit together, experiment with the adjustment of *R4* while watching the LED. The LED should turn rapidly on and off as you rotate *R4's* shaft past the point where the 555 oscillates at the f of the 567. If you dim the room lights, you may notice the LED flickering just before and after it turns full on and off. Resistor *R2* limits LED current to about 3.5 mA. If your workbench is brightly illuminated or your LED inefficient, you can reduce the value of R2 (say, to 500 ohms) to get more current through the LED. In any event, be sure to use a regulated dc supply or fresh batteries.

Frequency Response. A graph showing the response of the circuit in Fig. 2 in the acceptance bandwidth region is shown in Fig. 3. The graph shows the input frequency from the 555 versus the output current through the LED. Note that the bandwidth is fairly wide when the input frequency goes high to low and vice versa.

After you've tried changing the frequency of the input tone, replace *R1* of the tone decoder with a 2000-ohm fixed resistor in series with a 20,000- or 25,000-ohm potentiometer and readjust *R4* to provide an unknown input tone. You should easily be able to lock onto the unknown input frequency by adjusting the potentiometer. You can arrive at a rough estimate of the frequency of the unknown tone *without* using a scope or counter by measuring the total resistance of the potentiometer and its 2000-ohm series resistor and using the center-frequency formula.

At this point, the 567 would appear to work just fine, since it triggers an LED in response to any desired tone. But if you actually build the test circuit, you'll soon discover that the 567

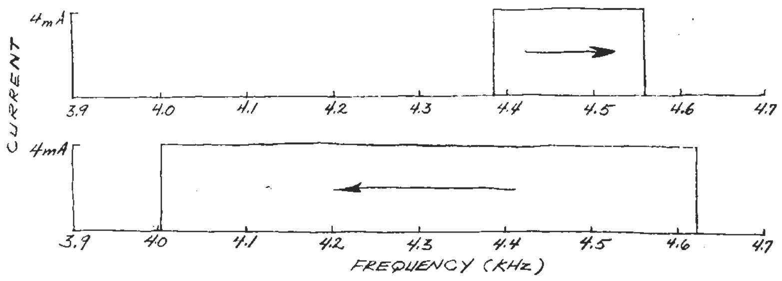


Fig. 3. Frequency response of circuit in Fig. 2. Arrows indicate positive and negative frequency changes.

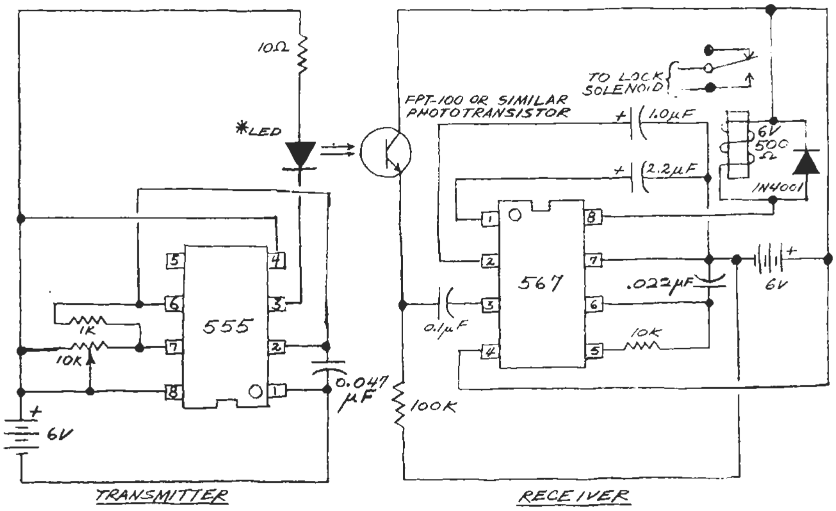
has a tendency to trigger on what appear to be harmonics of the center frequency. The 567 will, in fact, lock onto frequencies corresponding to input signals near f_0 (4n + 1) (where n = 0, 1, 2, 3 . . .). Also, the square pulses from the 555 will cause an output for $f_0/2$.

Fortunately, the response of the 567 to tones other than f_0 is usually of no consequence. And if false triggering to undesired tones becomes a problem, you can either change the center frequency of the 567 or attenuate the offending tone with a notch filter.

Other Applications. After you have experimented with the 567 using the basic circuit in Fig. 2, you will probably think of lots of interesting applications. One fascinating possibility is a secret photoelectric lock activated by a tone-modulated LED. A phototransistor connected to the input of the 567 can be used to receive the signal from the LED, as shown in Fig. 4. This circuit has an optical range of a few centimeters without external lenses at either the LED or phototransistor. This is all the distance you need for most lock applications, but for more range you can add an amplifier between the phototransistor and the 567 and use a lens at each end.

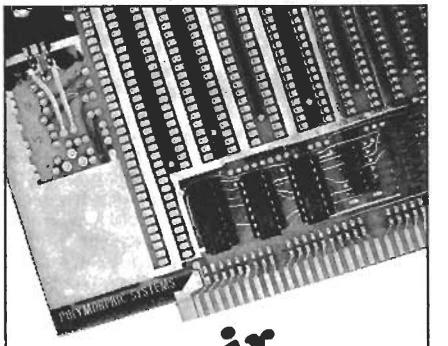
Whether checking out a potential application or just for fun, don't hesitate to experiment with the basic 567 circuit in Fig. 2. For best results, Signetics recommends that the resistance of R1 be between 200 and 20,000 ohms. Capacitor C2, the loop low-pass filter, should be selected from the Bandwidth versus Input Signal Amplitude graph given in both the National and Signetics data sheets on the 567.

At very low input frequencies, the time required for the 567 to lock onto the input tone can become relatively long. For example, I found that an input tone of 500 Hz required a full second for lock to occur. These and other eccentricities of the 567 are covered in detail in the manufacturer's (Signetics) data sheet, and I urge you to obtain this well-prepared document to assist you while experimenting with the 567. Another excellent source of information on the 567 is found in the Signetics Digital/Linear/MOS Applications book (Section 6, "Phase Locked Loop Applications"). ◈



*USE HIGH EFFICIENCY INFRARED EMITTER SUCH AS SSL-55C, TIL 31, ETC. 555 APPLIES 45μS WIDE PULSES WITH PEAK CURRENT OF 120mA TO LED

Fig. 4. Infrared-activated secret lock.



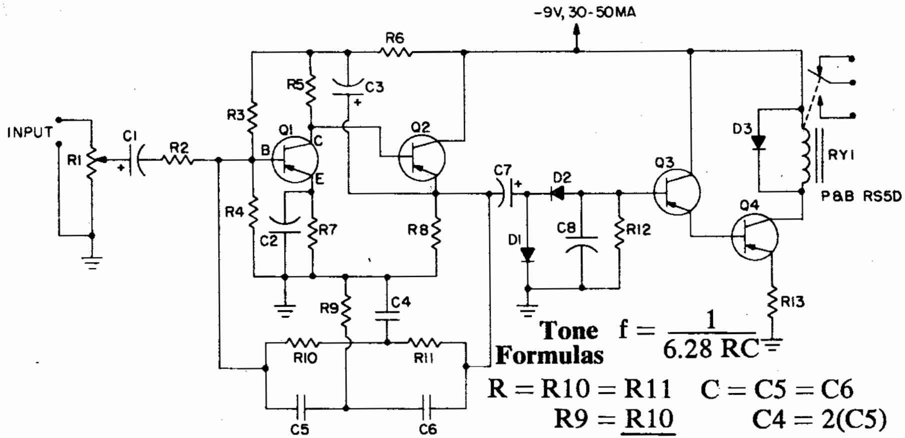
94 Tone Controlled Relay

NEW 1976

☐ This tone controlled relay circuit is a lot more complex and more expensive than the usual tone control circuit but it's suggested for use when you need super-sensitivity and/or super-Q (the ability to respond only to the control frequency). Capacitor C8 provides a small delay of about 0.5 second so the unit can distinguish between the control input tone and random frequencies from sounds picked up by, say, a dynamic microphone which can be connected to the input. In typical use potentiometer R1 is adjusted for the minimum input signal that provides reliable tripping of the relay.

The values shown provide an operating frequency of approximately 1500 Hz. The frequency is determined by R9, R10, R11, C4, C5 and C6. The relationship between these components is shown in the schematic. Frequency is calculated with the formula $F = \frac{1}{2\pi RC}$. Use 4,700-ohm resistors for R10 and R11 even if it limits the range of frequencies you can use.

Virtually any general purpose PNP transistors of the type indicated in the parts list can be used. Diodes D1 and D2 should be the germanium 1N34/1N60 type. Be very careful about all power supply and capacitor polarities.



Tone Formulas $f = \frac{1}{6.28\,RC}$

$R = R10 = R11 \qquad C = C5 = C6$

$R9 = \frac{R10}{2} \qquad C4 = 2(C5)$

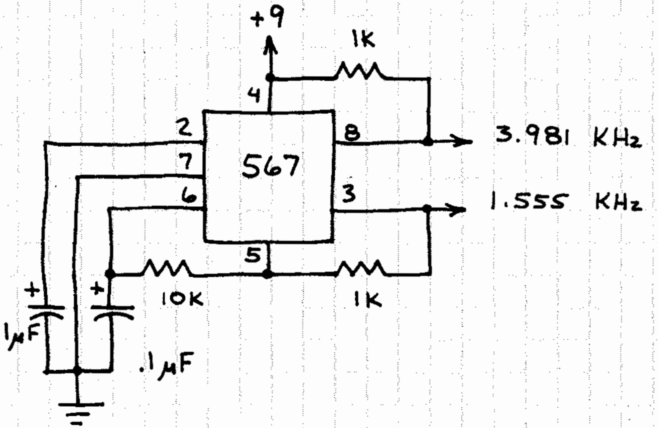
PARTS LIST FOR
TONE CONTROLLED RELAY

Resistors ½ watt, 10%, unless otherwise specified
- **R1**—25,000- to 50,000-ohm linear potentiometer
- **R2, R10, R11**—4,700-ohms
- **R3**—100,000-ohms
- **R4**—10,000-ohms
- **R5**—5,600-ohms
- **R6**—2,200-ohms
- **R7**—1,200-ohms
- **R8**—3,300-ohms
- **R9**—2,400-ohms
- **R12**—47,000-ohms
- **R13**—22-ohms

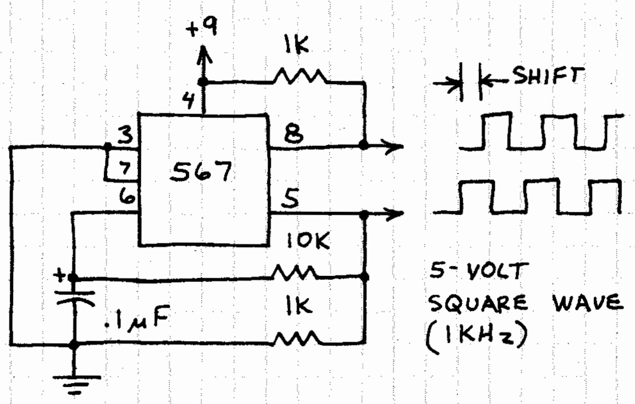
Capacitors rated 10-VDC or higher
- **C1, C2, C4**—0.047-uF
- **C3**—2-uF
- **C5, C6**—0.022-uF
- **C7**—15-uF
- **C8**—50-uF
- **Q1, Q2, Q3, Q4**—2SB22, (Radio Shack 276-2003 or equiv.)
- **D1, D2**—Germanium diode type 1N60 or equiv.
- **D3**—Silicon rectifier type 1N4001 or equiv.
- **RY1**—Relay, 200- to 400-ohm coil, 6-VDC, P&B RS5D-6 or equiv.

TONE DECODER (CONTINUED)
567

2-FREQUENCY OSCILLATOR



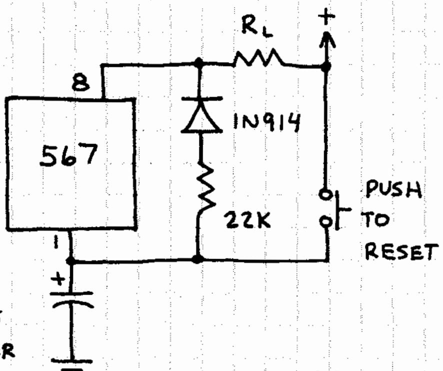
2-PHASE OSCILLATOR



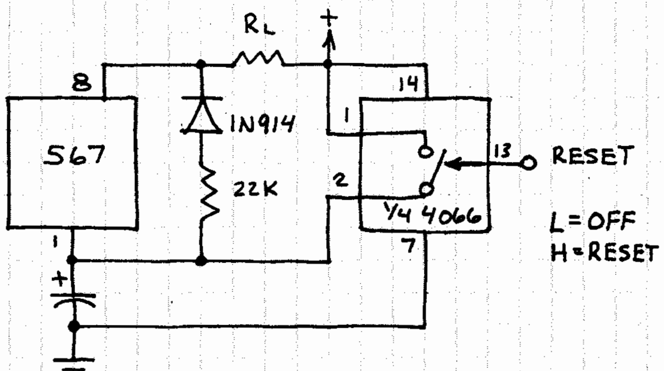
LATCHING THE 567 OUTPUT *

BOTH CIRCUITS SHOW ONLY THE LATCH COMPONENTS. RL IS THE LOAD (LED, RELAY, ETC.).

*OUTPUT STAYS ON EVEN AFTER INPUT TONE IS REMOVED.

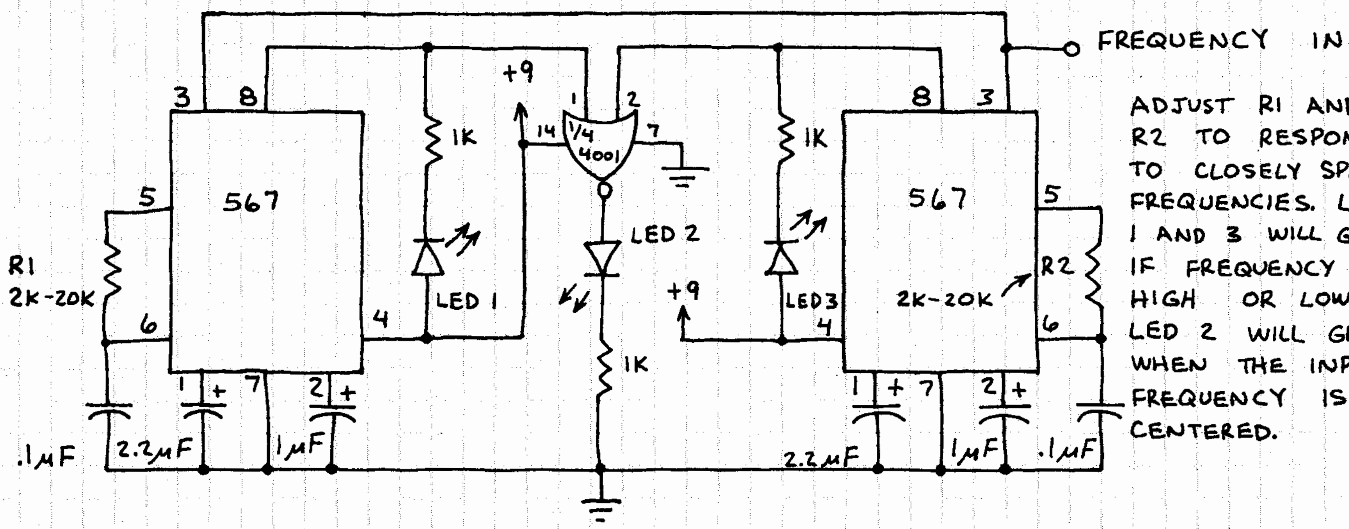


MANUAL RESET



LOGIC RESET

NARROW BAND FREQUENCY DETECTOR

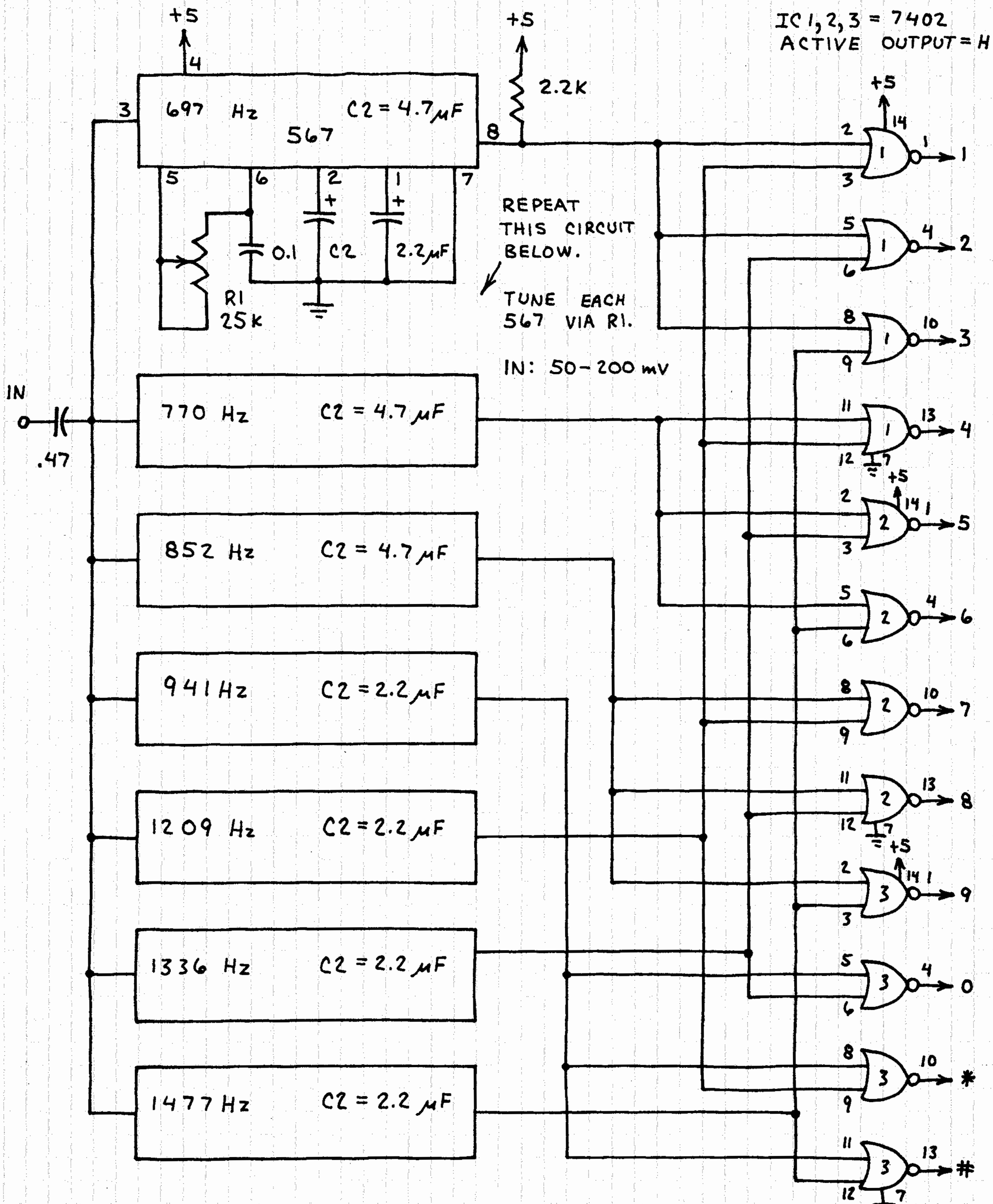


ADJUST R1 AND R2 TO RESPOND TO CLOSELY SPACED FREQUENCIES. LEDs 1 AND 3 WILL GLOW IF FREQUENCY IS HIGH OR LOW. LED 2 WILL GLOW WHEN THE INPUT FREQUENCY IS CENTERED.

TONE DECODER (CONTINUED)

567

TOUCH-TONE® DECODER



IC 1, 2, 3 = 7402
ACTIVE OUTPUT = H

REPEAT THIS CIRCUIT BELOW.

TUNE EACH 567 VIA R1.

IN: 50-200 mV

Missing-pulse detector handles variable frequencies

by Joe Lyle and Jerry Titsworth
Bendix Corp., Aircraft Brake and Strut Division, South Bend, Ind.

Virtually all missing-pulse detectors require an input signal of fixed frequency in order to operate satisfactorily. They malfunction when the input frequency varies because their circuits employ detection networks that have a fixed time constant. Through the implementation of inexpensive voltage-to-frequency and frequency-to-voltage converters to derive an average, or reference, frequency that tracks the input signal, this circuit can pinpoint missing pulses without being affected by input frequency variations.

As shown in the figure, A_1 and A_2 establish the reference frequency, f_{ref}, using input frequency f_{in}. Missing pulses do not change the reference because of the integrating capacitors within the converters. Meanwhile, the three NAND gates comprising the one-shot produce pulses of 10 microseconds in duration, with a frequency determined by the input signal.

The chip labeled A_4 is clocked by f_{ref} and A_3 through a NAND gate. As long as the input train is continuous, the Q output of A_4 is low. If a missing pulse is detected, however, the one-shot will not generate a pulse to the reset pin of A_3, and the Q output of A_3 (which is also clocked by f_{ref}) will go high to clock A_4. A_4 and f_{ref} will then switch A_5's Q output to high.

This turns on transistor Q_1 and the pilot lamp glows. Switch S_1 is used to reset the circuit after a missing pulse has been detected. Note that circuit operation remains independent of the input frequency, since the arrival of f_{ref} and the 10-µs pulse at A_3 is synchronized to f_{in}.

The circuit should be calibrated by setting A_1 for an output voltage of 10 when a 10-kilohertz input signal is applied. Similarly, A_2 should be set to generate a 10-kHz signal for a 10-V input. ☐

Synchronous. The circuit detects the missing pulse independently of the pulse train frequency. Voltage-to-frequency and frequency-to-voltage converters derive a reference frequency whose average remains the same for small anomalies occurring in the pulse train: converters' integrating capacitors hold f_{ref} steady despite missing pulses. The reference in this way serves as a synchronous clock.