WORKING WITH LED DISPLAY DRIVERS

Learn all about 7-segment display decoder/drivers in our continuing coverage of optoelectronic IC's.

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IN OUR LAST INSTALLMENT WE looked closely at theory and practical applications of the LM3914-series of LED bargraph driver IC's and concluded with 7-segment display systems. In this article, we'll examine 7-segment display driving techniques in detail, concentrating on decoder/driver devices and circuitry.

Display latching

In the last article we introduced 7-segment displays and simple BCD-to-7-segment decoder/driver IC's that can be used to activate those displays. Figure 1 shows how three sets of those IC's can be used with a trio of decade counters to make a simple digital-readout "frequency" meter. In the figure, the amplified external frequency signal is fed to the input of the series-connected counters with one pin of a 2-input AND gate. The other input is derived from a timebase generator.

When the timebase input signal is low, the AND gate is off, and there is no input to the counters. When the timebase gate signal switches high, a brief RESET pulse is fed to all three counters, setting them all to zero. Simultaneously, the input gate turns on and remains on for one second. During that time the input-frequency pulses are summed by the counters. At the end of the one-second period, the gate turns off as the timebase gate signal goes low again. That ends the count and enables the display modules so that they give a steady reading of the total pulse count, and therefore the frequency. The whole process repeats itself again one second later when the timebase gate signal goes high.

The simple system illustrated has one major drawback: The display blurs during the counting period, becoming stable and readable only when each count is complete and the input gate is off. Figure 2 shows a circuit for frequency meters designed to overcome display blurring. In the circuit, a 4-bit data latch is wired between the output of each counter and the input of its decoder/driver IC.

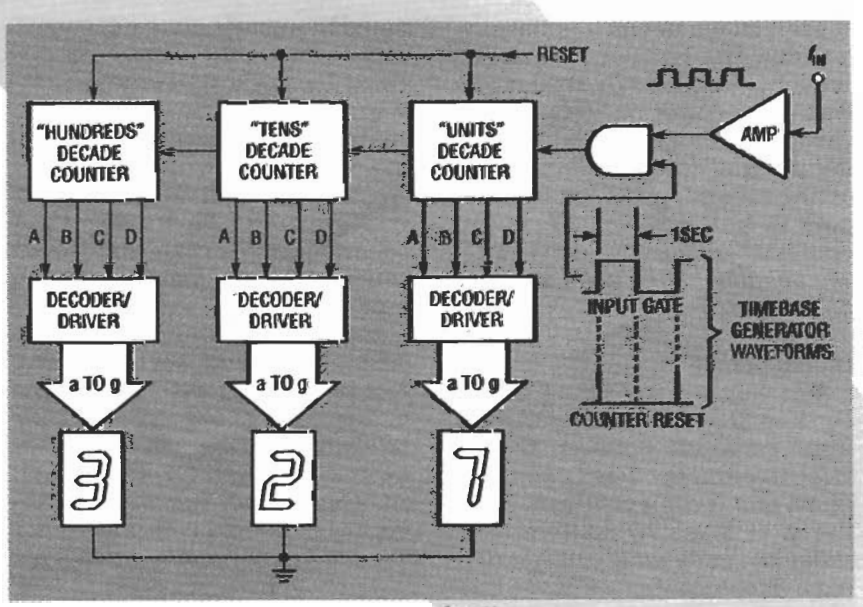

FIG. 1—SIMPLE DIGITAL frequency-meter circuit.

When the timebase gate signal goes high, a reset pulse is fed to all counters, setting them to zero. Simultaneously, the input gate is turned on, and the counters start to sum the input signal pulses. The count continues for one second while the 4-bit latches prevent the counter output from reaching the display drivers. As a result, the display remains stable during that interval. At the end of the period a brief LATCH-ENABLE pulse is fed to all latches.

The instantaneous binary-coded decimal (BCD) outputs of each counter are then latched into memory, and also fed to the display via the decoder/driver IC's. That steadies the reading of the display to give a total pulse count, which corresponds to the input signal frequency. A few moments later, the sequence repeats itself with the counters resetting and then counting the input frequency pulses for one second, and so on.

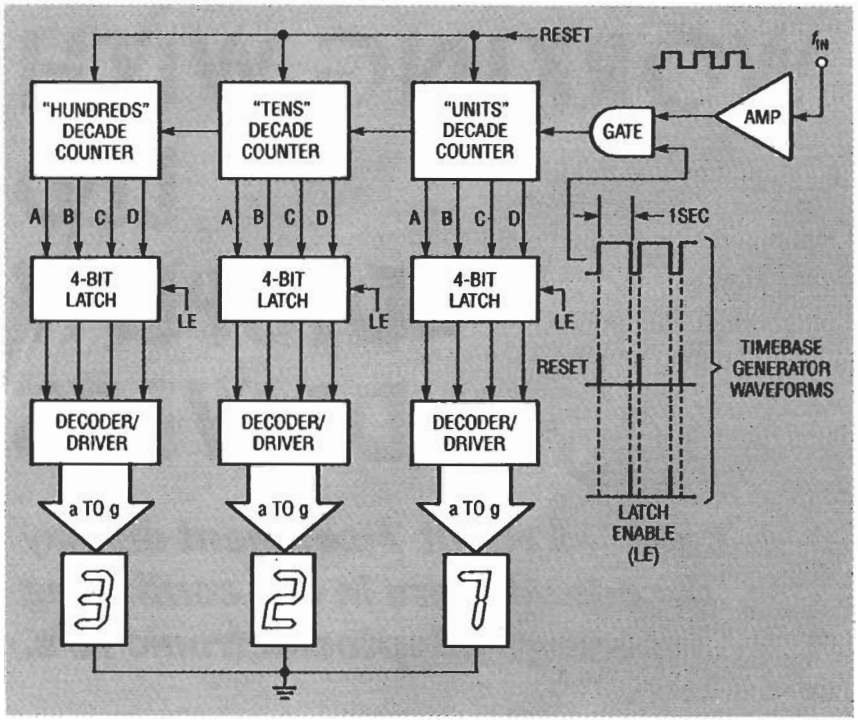

FIG. 2—IMPROVED DIGITAL frequency-meter circuit.

The circuit in Fig. 2 generates a stable display that is updated once per second. In actual circuits, the count periods shown in Figs. 1 and 2 can be set at any decade multiple or submultiple of one second, provided the display is suitably scaled. Many commercial decoder/driver IC's are available with built-in 4-bit data latches.

Multiplexing

You can see in Figs. 1 and 2 that at least 21 connections must be made between the IC circuitry and the 7-segment displays of a 3-digit readout. Similarly, at least 70 connections must be made for a 10-digit display. The number of IC-to-display connections can be significantly reduced with a technique known as *multiplexing*. Figures 3 and 4 illustrate multiplexing.

Figure 3 shows how each digit of a 3-digit common-cathode LED display is individually activated with only 10 external connections. In the display circuitry, all "a" segments are connected together, as are all other sets of segments ("b" to "g"). Thus only seven external "a" to "g" connections are made to the display, regardless of the number of digits used. However, no 7-segment display is illuminated by signals on the segment wires unless the display is enabled by tying its common terminal to ground. In Fig. 3, enabling is achieved by activating switching transistors Q1, Q2, and Q3 with suitable external signals. However, this scheme calls for an additional connecting wire for each display module.

Figure 3 also shows how three different sets of segment data can be selected with switch S1-a, and each of the three display modules can be selected with switch S1-b and Q1, Q2, or Q3. S1-a and S1-b are ganged together to form a two-pole rotary switch which provides the multiplexing. These switch elements represent a fast-acting electronic switch capable of cycling the contacts through positions 1, 2, and 3 fast enough for flicker-free multiplexing.

The operating sequence of the circuit shown in Fig. 3 will be discussed here. Assume initially that the contacts of S1-a and S1-b are in position 1 so that S1-a selects segment data of display module 1 (1_{a-g}), and S1-b activates display module 1 with Q1. Module 1 will then show an illuminated number "3." Moments later the switch contacts move to position 2, selecting segment data 2 (2_{a-g}) and illuminating module 2 with Q2. Module 2 will then be illuminated to show the number "2." Moments after that, the switch contacts move to position 3, causing module 3 to show the number "7." Thus only one digit is ever on at any one time.

In practical displays, the sequence is repeated fast enough so that you do not see the display segments being turned on and off. Your eye's persistence of vision makes it look as if the three digits are all lit up together. The multiplexing frequency must be about 1 kHz.

Figure 4 shows a more realistic arrangement for multiplexing a 3-digit frequency meter. The multiplexer (MUX) is located between the outputs of the three BCD data latches and the input of a display-driving BCD-to-7-segment decoder/

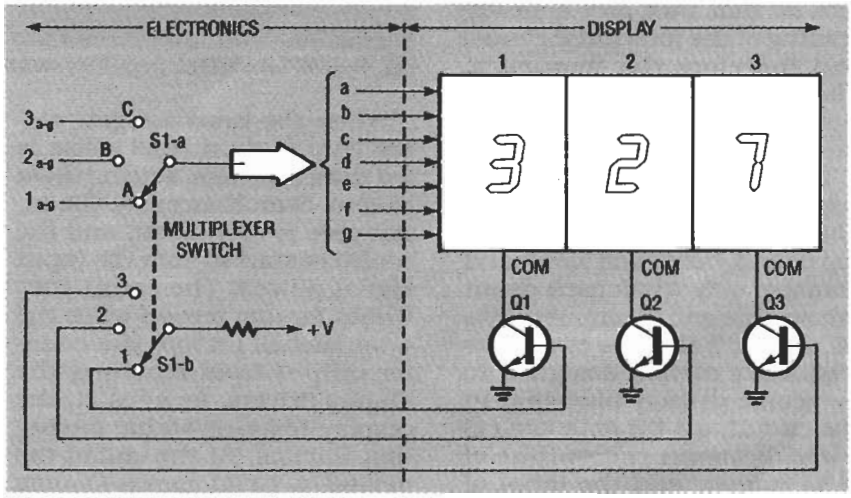

FIG. 3—MULTIPLEXING METHOD for a 3-digit common-cathode LED display.

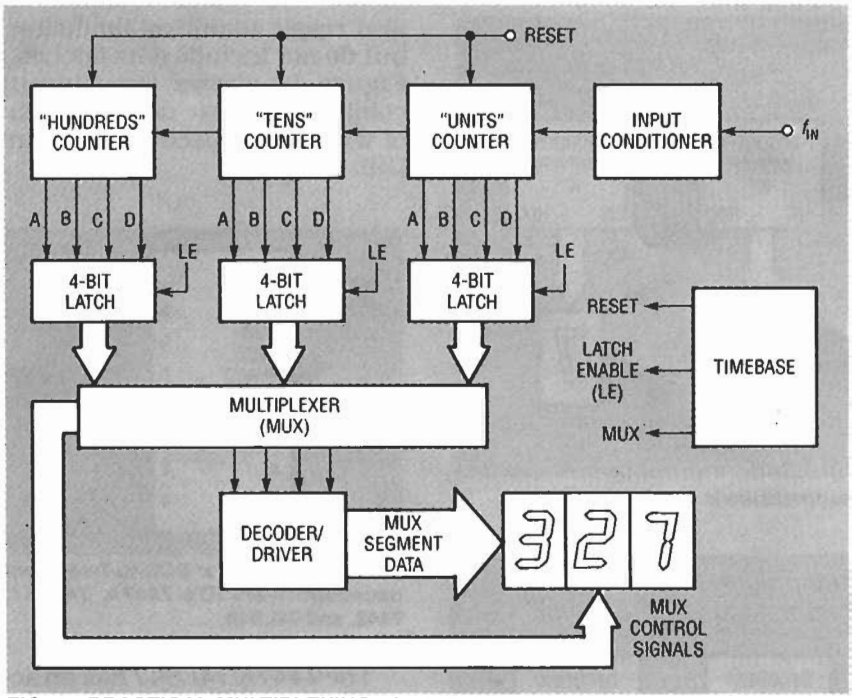

FIG. 4—PRACTICAL MULTIPLEXING of a 3-digit frequency meter.

driver IC. The scheme shown has two major advantages: Only one decoder/driver IC is needed (regardless of the number of readout digits), and its multiplexer includes only five ganged 3-way sequencing switches. One of those switches is for control data, and four are for BCD-segment data. That arrangement saves three ganged 3-way switches, as compared with the eight needed in Fig. 3.

Commercial large-scale integrated (LSI) IC's now available can perform all of the counting, latching, multiplexing, decoding, timing, and display-driving functions in Fig. 4. A device of this complexity is typically packaged in a dual-in-line package (DIP) with only 20 pins. Those pins provide for all necessary connections to the power supply, display modules, and inputs. Therefore, a complete 4-digit counter can be built with a dedicated IC in a circuit such as that shown in Fig. 5. Another example of an LSI IC in a display circuit is the 3½-digit digital voltmeter (DVM) chip shown in Fig. 6.

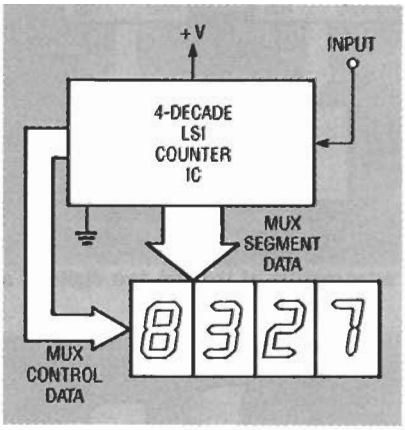

FIG. 5—4-DIGIT COUNTER CIRCUIT based on an LSI chip.

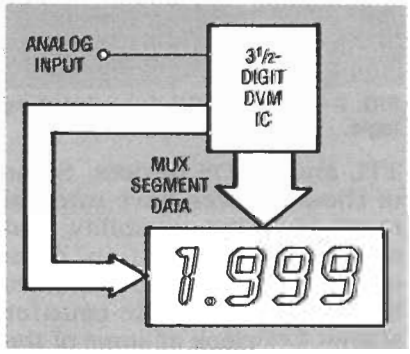

FIG. 6—3-1/2-DIGIT VOLTMETER based on an LSI chip.

Ripple blanking

Unless there is automatic suppression of the two unwanted leading zeros, the 4-digit circuit in Fig. 5 will give an actual reading of 0027 if it is used to measure a count of 27. Similarly, if the 3½-digit circuit of Fig. 6 measures 0.1 volt, it will display 0.100 volt unless the two unwanted trailing zeros are automatically suppressed.

In practical circuits, automatic blanking of leading or trailing zeros can be performed with a *ripple-blanking* technique, as shown in Figs. 7 and 8. Each decoder/driver IC (with a BCD input and 7-segment output) is provided with a RIPPLE-BLANKING INPUT (RBI) and scripple-blanking output (RBO) pins.

Assuming those pins are active-high, if the RBI terminal is held low (logic 0), the 7-segment outputs of the IC are enabled, but the RBO terminal is disabled (held low). If the RBI terminal is biased high (logic 1), the 7-segment outputs become disabled in the presence of a BCD 0000 input, and the RBO output goes high under the same condition. The RBO terminal, therefore, is normally low and goes high only if a BCD 0000 input is present at the same time the RBI terminal is high.

Figure 7 shows the ripple-blanking technique for leading-zero suppression in a 4-digit display with a reading of 207. The RBI input of the thousands or most significant digit (MSD) decoder/driver is tied high, so the readout is automatically blanked in the presence of a zero when the RBO terminal is high. Consequently, the RBI pin of the hundreds IC is high, the readout shows 2, and the RBO terminal is low. The RBI input of the tens unit is low, so the readout shows 0 and its RBO output is low. The units readout shows the least significant digit (LSD), which does not require zero suppression. Its RBI pin is grounded and the readout shows 7. The display therefore gives a total reading of 207.

In the leading-zero suppression circuit, Fig.7, the ripple-blanking feedback is applied backwards from the MSD to the LSD. Figure 8 shows how trailing-zero suppression is accomplished by reversing the direction of feedback from the LSD to the MSD. Therefore, when an input of 1.1 volts is fed to that circuit, the LSD is blanked, because its BCD input is 0000 and its RBI input is high. The RBO

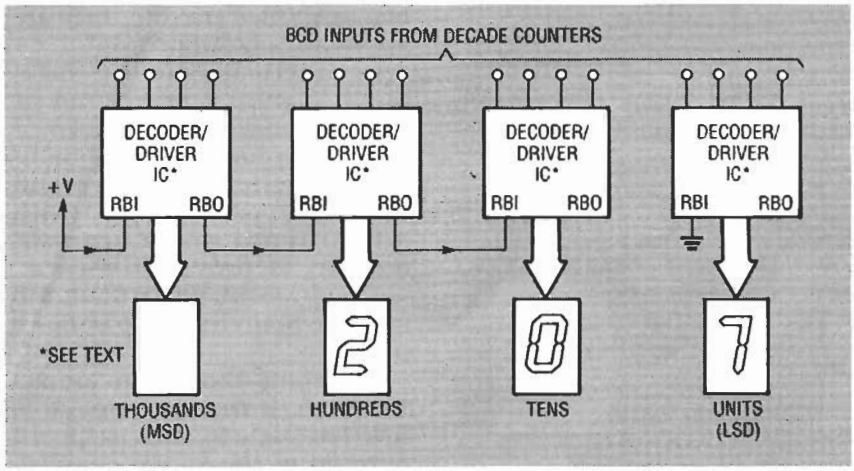

FIG. 7—RIPPLE-BLANKING for leading-zero suppression in a 4-digit counter.

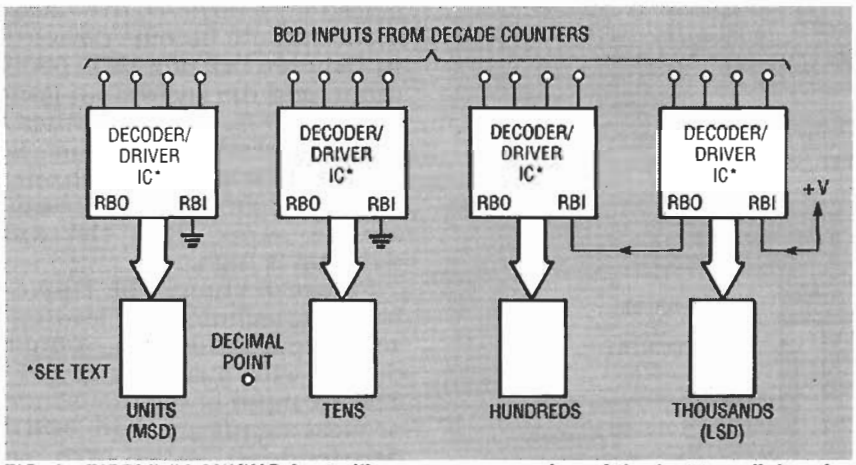

FIG. 8—RIPPLE-BLANKING for trailing-zero suppression of the last two digits of a 3-1/2-digit DVM readout.

terminal is high under that condition, so the hundredth's digit is also blanked in the presence of a 0000 BCD input.

Most decoder/driver IC's have RIPPLE-BLANKING INPUT and RIPPLE-BLANKING OUTPUT pins. Usually these pins are active-low. If a decoder/driver IC does not include integral ripple-blanking logic, it can usually be obtained by adding external logic circuitry similar to that shown in Fig. 9. The RBO pin is connected to the BLANKING INPUT pin of the decoder/driver IC. Figure 9 shows an active-high circuit in which the output of the 4-input NOR gate goes high only with a 0000 BCD input. The RBO output goes high only if the 0.0 input is present when RBI is biased high.

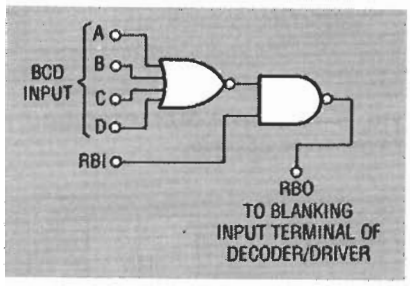

FIG. 9—ACTIVE-HIGH ripple-blanking logic.

Decoder/driver IC's

Many decoder/driver IC's are available commercially as both TTL and CMOS devices. Some of those devices have integral ripple-blanking capability, and others have built-in data latches. A few of those devices have built-in decade-counter stages. Let's look at some of the most popular of those devices.

The 7447A and 7448 7-segment decoder/driver IC's are in the standard TTL family. They are also available in a low-power Schottky (LS) form designated as 74LS47 and 74LS48, respectively. All of those IC's have integral ripple-blanking facilities, but do not include data latches. Figure 10 shows the pinout common to those devices, each of which is housed in a 16-pin DIP.

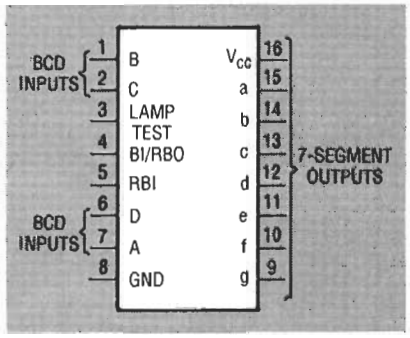

FIG. 10—PINOUT for BCD-to-7-segment decoder/drivers IC's 7447A, 74LS47, 7448, and 74LS48.

The 7447A/74LS47 has an active-low output designed for driving a common-anode LED with external current-limiting resistors (R_X), as shown in Fig. 11. The 7448/74LS48 has an active-high output that drives a common-cathode LED in a manner similar to that of the circuit in Fig. 11, but with the common terminal of the display connected to ground. In all cases, the R_X current-limiting resistors should be chosen to limit the individual segment currents below the following absolute limits:

7447A = 40 mA
74LS47 = 24 mA
7448 and 74LS48 = 6 mA

Figure 12 shows how a 7448/74LS48 can drive a liquid-crystal display (LCD), using a pair of 7486 or 74LS86 quad 2-input XOR gate IC's. An external 50-Hz square wave applies the necessary phase signals to the display.

As shown in Fig. 10, each of the 7447/7448 IC's has three input control pins: LAMP TEST, BI/RBO, and RBI. The LAMP TEST pin drives all display segments on when the pin goes to logic-low with the RBO pin on or at logic-high. When the BI/RBO pin is pulled low, all outputs are blanked. The BI/RBO pin also functions as a RIPPLE-BLANKING OUTPUT pin. Figure 13 shows how to connect the RIPPLE-BLANKING pins to give leading-

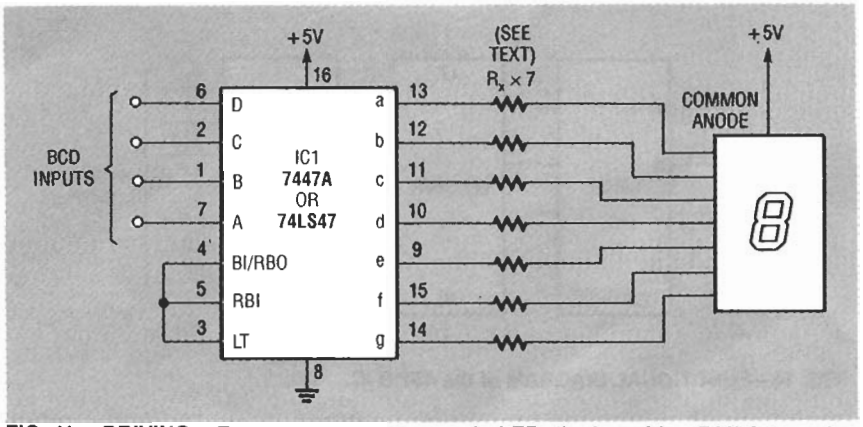

FIG. 11— DRIVING a 7-segment common-anode LED display with a 7447A-type decoder/driver.

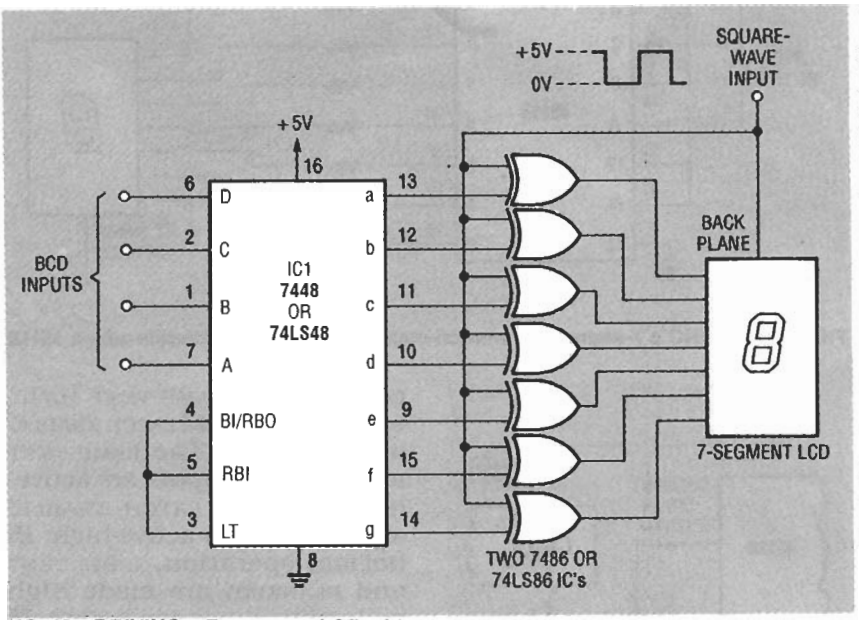

FIG. 12—DRIVING a 7-segment LCD with a 7448-type decoder drivers.

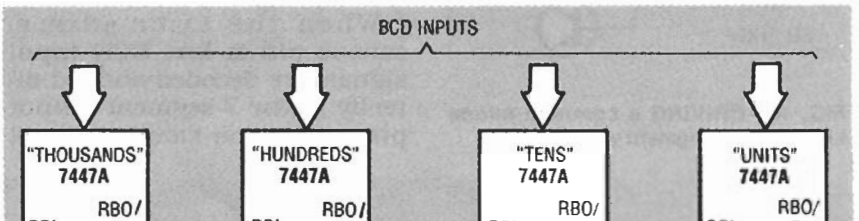

FIG. 13— SUPPRESSION OF FIRST THREE digits of a 4-digit display with 7447A-type decoder/drivers.

zero suppression on the first three digits of a 4-digit display.

The 4511B is a BCD-to-7-segment decoder/driver IC with an integral 4-bit data latch, but it lacks built-in ripple-blanking. That CMOS device features NPN bipolar transistor output stages capable of handling output currents up to 25 mA. It can drive most popular 7-segment displays. Figure 14 is a functional diagram of the IC. The 4511B will operate from any 5- to 18-volt power supply.

The 4511B has three input-

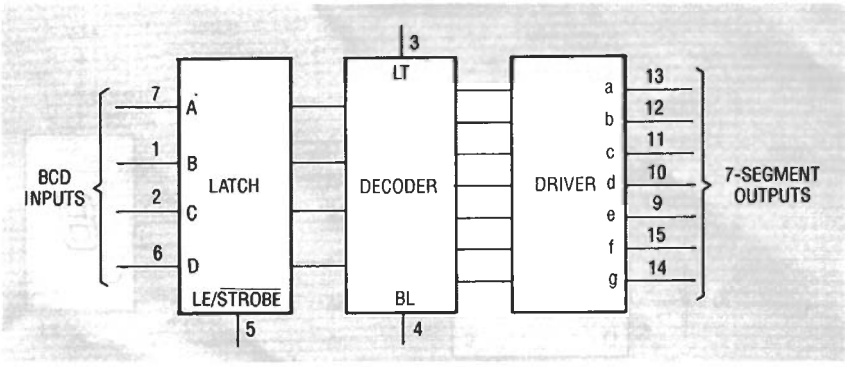

FIG. 14—FUNCTIONAL DIAGRAM of the 4511B IC.

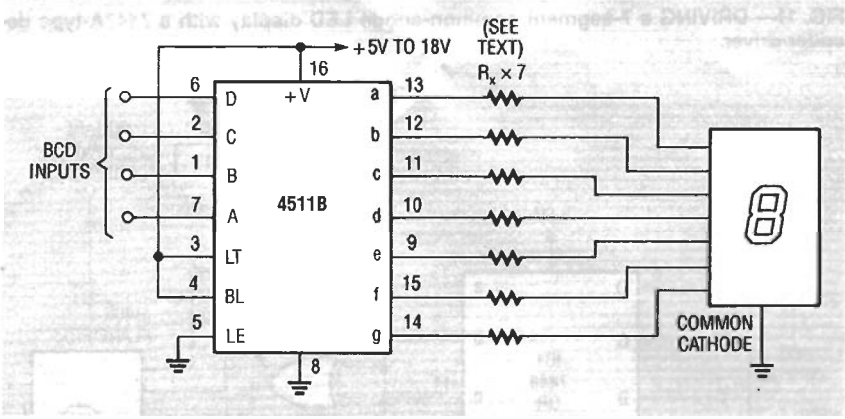

FIG. 15—DRIVING a 7-segment, common-cathode LED display module with a 4511B.

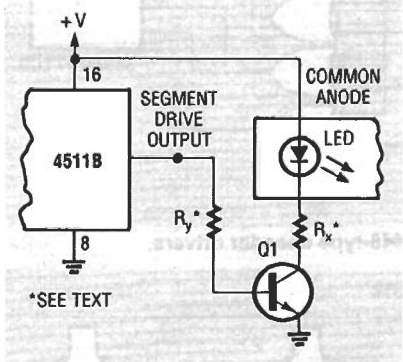

FIG. 16—DRIVING a common-anode LED lamp or segment with a 4511B.

control pins: LAMP TEST (LT), BLANKING (BL), and LATCH ENABLE/STROBE (LE/S). The LAMP TEST and BLANKING inputs are active-low, and the LATCH ENABLE/STROBE input is active-high. In normal operation, LAMP TEST and BLANKING are made high and LATCH ENABLE/STROBE is held low.

When the LATCH ENABLE/STROBE pin is low, BCD input signals are decoded and fed directly to the 7-segment output pins. If LATCH ENABLE/STROBE

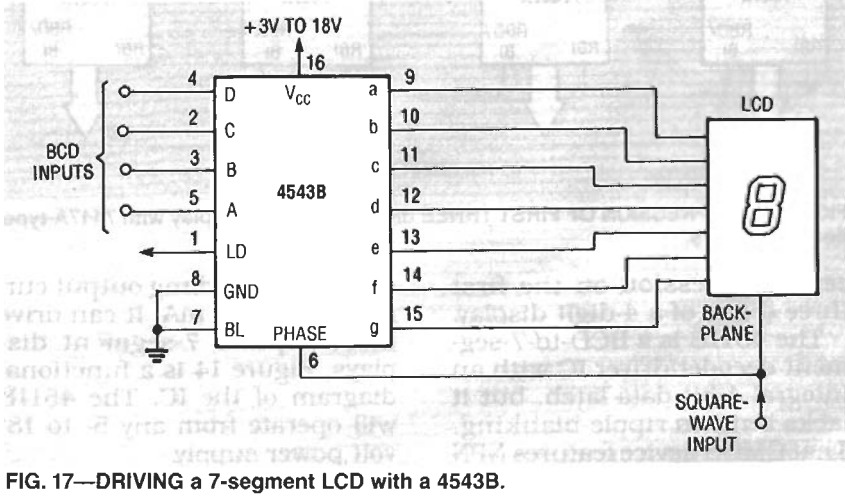

FIG. 17—DRIVING a 7-segment LCD with a 4543B.

goes high, the BCD input signals present at the moment of transition are latched into memory and fed (in decoded form) to the 7-segment outputs, while LATCH ENABLE/STROBE remains high. If the LAMP TEST input is grounded, all output segments are activated, regardless of the BCD inputs. If the BLANKING input is grounded (while LAMP TEST is positive), all output segments are blanked.

Figure 15 shows the basic connections for driving a common-cathode LED. A current-limiting resistor (R_X) must be wired in series with each display segment, and it must have a value chosen to hold the segment current below 25 mA. Note that the segment outputs of the 4511B are not internally current-limited. Therefore, the device has no output-overload protection.

Figure 16 shows how to modify the circuit in Fig. 15 to drive an LED common-anode display. In the example shown in Fig. 16, an NPN buffer transistor must be used between each output-drive segment and the input segment of the display. Resistor R_X sets the operating segment current of the display in those examples, and R_Y sets the base current of the transistor.

The 4511B can also drive 7-segment liquid-crystal displays (LCD) with an external square-wave PHASE signal and a set of XOR gates similar to those of Fig. 12. In practical circuits, however, it is better to use a 4543B IC for that specific application.

The 4543B is a 7-segment CMOS decoder/driver with an integral 4-bit data latch. It was designed for driving LCD's, but it can also drive most other 7-segment displays.

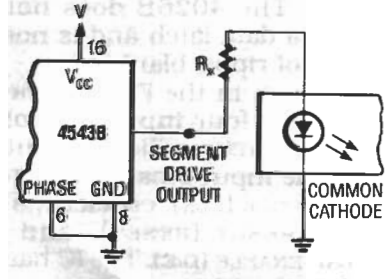

FIG. 18—DRIVING A common-cathode LED lamp or display segment with a 4543B.

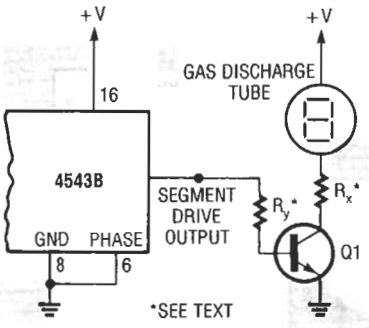

FIG. 19—DRIVING A gas-discharge tube or display segment with a 4543B.

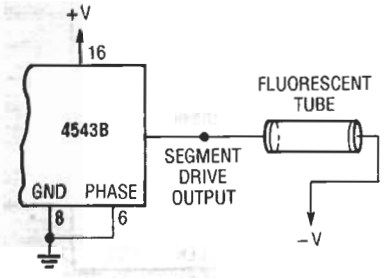

FIG. 20—DRIVING A fluorescent tube or display segment a 4543B.

The 4543B has three input control pins: LATCH DISABLE (LD), PHASE, and BLANKING (BL). In normal use, the LATCH DISABLE pin is biased high and the BLANKING pin is tied low. The state of the PHASE pin depends on the display that is being driven. For driving LCD displays, a square wave (approximately 50 Hz, swinging fully between the ground and V_{cc}) must be applied to the PHASE pin. The PHASE pin must be grounded for driving common-cathode LED's and it must be tied to logic-high for driving any common-anode displays.

The display can be blanked at any time simply by driving the BLANKING pin to the logic-high state. When the LATCH DISABLE pin is in its normal high state, BCD inputs are decoded and fed

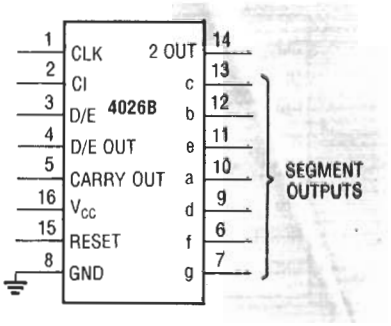

FIG. 21—PINOUT of the 4026B decade counter with 7-segment outputs.

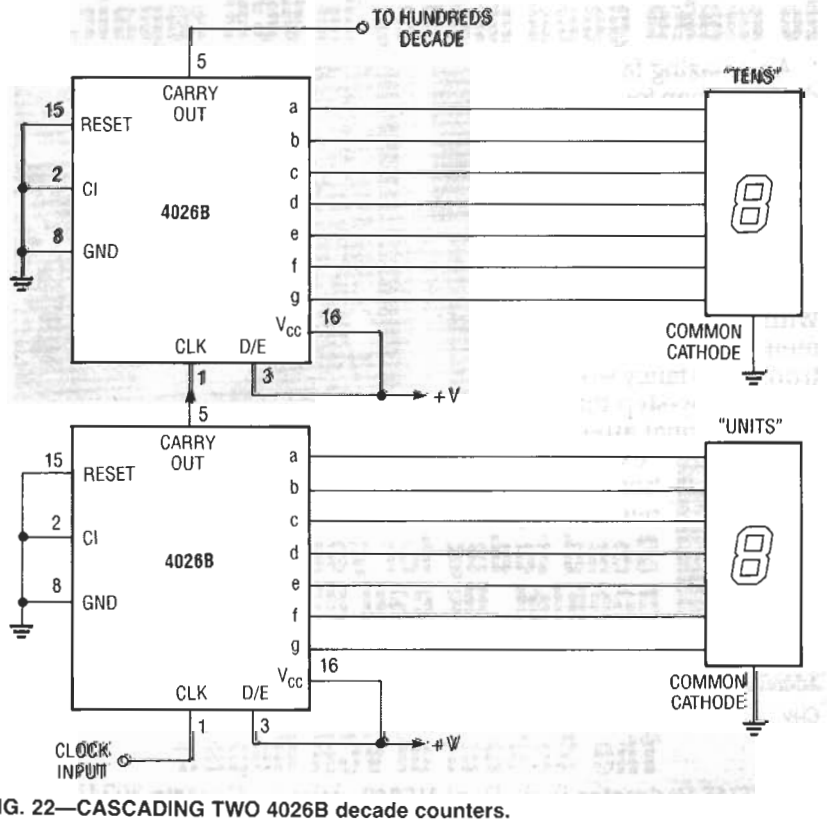

FIG. 22—CASCADING TWO 4026B decade counters.

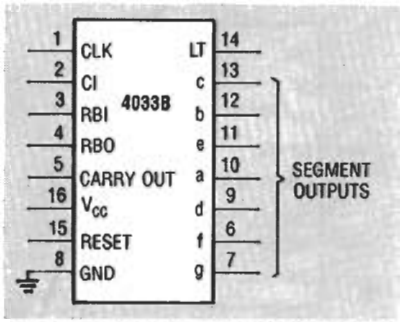

FIG. 23—PINOUT for the 4033B decade counter with 7-segment outputs and ripple blanking.

directly to the 7-segment output pins of the IC. When the LATCH DISABLE pin is pulled low, the BCD input signals present at the moment of transition are latched into memory and fed (in decoded form) to the 7-segment outputs while LATCH DISPLAY remains low.

Figure 17 shows a method for using the 4543B to drive an LCD, and Figs. 18–20 show how that circuit can be modified to drive other 7-segment displays.

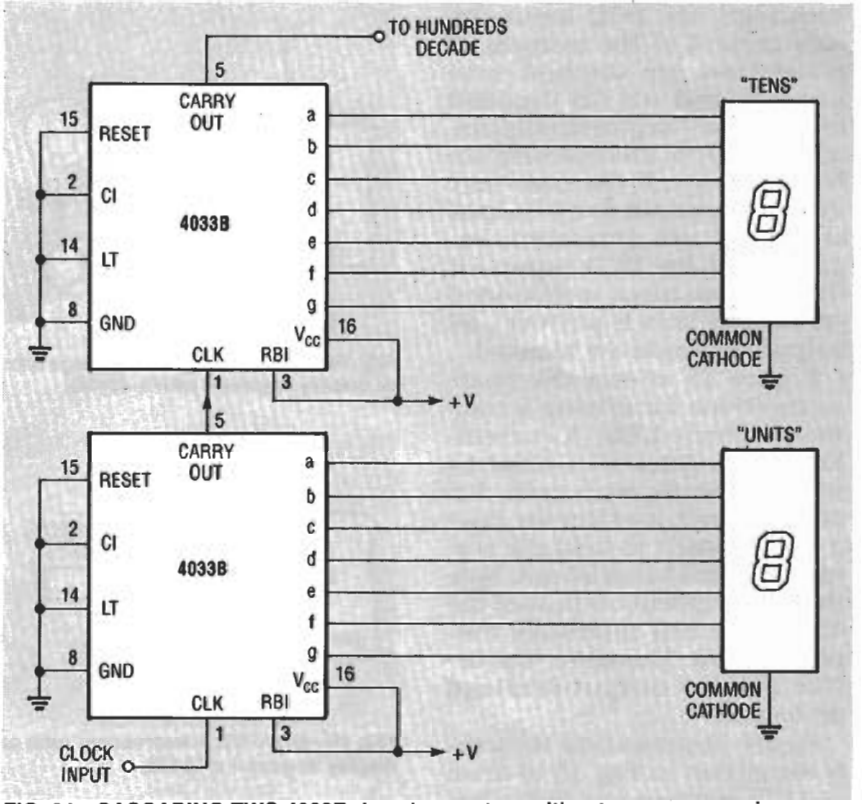

FIG. 24—CASCADING TWO 4033B decade counters without zero suppression.

The value of R_X in Fig. 18 must be chosen to limit the output drive current to below 10 mA per segment (individual LED lamp). If higher drive currents are needed, use a buffer transistor between the output of the 4543B and the input of the display segment.

Figure 21 shows the pinout of the 4026B, a complete decade counter with integral decoder/driver circuitry. It can drive a 7-segment common-cathode LED display directly. The segment output currents are internally limited to about 5 mA with a 10-volt supply or 10 mA with a 15-volt supply. Therefore, the display can be connected directly to the output of the IC without external current-limiting resistors. The 4026B does not include a data latch and is not capable of ripple blanking.

As shown in the Fig. 21, the 4026B has four input control pins and three auxiliary output pins. The input pins are designated: CLOCK (CLK), CLOCK INHIBIT (CI), RESET (RESET), and DISPLAY/ENABLE (D/E). The IC has a Schmitt trigger on its CLOCK (CLK) input line, and clock sig-

continued on page 93