designideas

Microcontroller's single I/O-port line drives a bar-graph display

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Instrument designs featuring a digital display may benefit from a secondary display that provides an analog version of the displayed parameter. A bar-graph display provides an easily interpreted graphical indicator that allows comparison with its fullscale value, but a conventional microcontroller-based design uses at least one eight-line I/O port to drive an eightsegment-bar-graph LED display.

As an alternative, some microcontrollers include a PWM (pulse-widthmodulated) output. You can minimize the number of required I/O lines by using the PWM output to drive National Semiconductor's (www. national.com) LM3914 bar-graph-display-driver circuit or an equivalent. In operation, the microcontroller's program adjusts the PWM output's pulse width such that the average voltage that feeds to the LM3914 circuit illuminates the required number of bars in the display.

The design in **Figure 1** obviates the shortcomings of these approaches and uses only one port line to drive an eight-segment bar graph. This design does not use a PWM output and hence can apply to any microcontroller.

Referring to the timing diagram in Figure 2, whenever the bar-graph display requires an update, the microcontroller's software delivers a pulse train through its output port. The first pulse comprises a pulse of width T₁ that's longer than the width of the pulse T_2 , which triggering monostable IC1, a 74123 or equivalent, produces. You apply both pulses to IC₃, a 7400 or equivalent NAND gate, which together with IC₁ forms a long-pulse detector. Use the equation in IC_1 's data sheet to select values for C_1 and R_1 that yield a value of approximately 1.5 msec for T₂'s output pulse. Typical widths for T₁ and T_3 are 3 and 1 msec, respectively.

The output pulse from IC₃ goes low for a duration of $T_1 - T_2$, and this pulse clears IC₂, an 8-bit serial-in parallel-out shift register, which forces all of IC₂'s outputs to go low and lights all segments of the bar-graph array (LED₁ to LED₈).

To light N segments of the bar-graph array, the microcontroller immediately sends a serial train of (8-N) pulses of width T₃ through the output-port line. Because the width of these pulses is less than T₂, NAND gate IC₃'s output always remains high and thus does not clear the shift register. The rising edge of each of





Figure 2 During the first pulse of the microcontroller's output-pulse sequence, the NAND gate's output clears the shift register and lights all of the display's segments.

the microcontroller's output pulses loads a high to one of IC₂'s outputs.

Note that shift register IC,'s OA output connects to the bar graph's most significant segment. Hence, the first pulse switches off the most significant segment. Starting with the most significant segment, for (8-N) pulses, 8-Nsegments switch off, and N segments beginning with the least significant segment remain lighted. Using this reverse logic takes advantage of the shift register's outputs' ability to sink more current than they can source—8 versus 0.4 mA, respectively, and thus produce a brighter bar-graph display without adding output buffers. Figure 2 shows a sample timing diagram that lights five of eight display segments.

If a second output-port line is available, you can omit using monostable multivibrator IC_1 and NAND gate IC_3 and use the second port to clear the shift register by outputting a zero whenever the bar graph requires an update. To obtain finer resolution, you can add segments to the bar graph by cascading additional shift registers. To light N segments of a display that is M segments long, the first output port sends M-N pulses to the shift register's clock input.

This design lends itself well to situations in which unused I/O-port lines are at a premium, as is the case for microcontrollers with reduced pin counts, or if you need to retrofit a bar-graph display by adding a daughterboard to a design.EDN