A New Thermal-Management Paradigm for Power Devices

By Dr. Paul A. Magill, Vice President of Marketing and Business Development, Nextreme Thermal Solutions, Durham, N.C.

Compatible with semiconductor fabrication and processing technologies, thermoelectric thin-film materials allow the cooling function to be integrated within power-semiconductor devices.

Power-semiconductor devices such as thyristors, MOSFETs and IGBTs operate in a high current-density mode in which they dissipate a high level of power, with heat-dissipation management becoming a crucial challenge. Compounding the heat-dissipation challenge is that the drive for most semiconductor devices is toward ever-smaller form factors, resulting in the need to properly control higher heat-dissipating device levels. The price structure for these smaller devices tends to run between $0.50 and $4 each, which means that the thermal-management solution must be a fraction of the cost.

Integrating Heat Management

Thermal-management solutions for power devices will be required that integrate not just high heat-flux capability, but also must meet extreme cost requirements. To meet these requirements, a solution is needed that can be integrated into the electronics-packaging process.

Thin-film thermoelectric materials are available as one attractive choice for thermal management. Thin-film material layers ranging from fractions of a nanometer to several micrometers in thickness are available for this purpose, and their use is growing in popularity. These materials can be grown using a metal organic chemical vapor deposition (MOCVD) reactor, and devices are then fabricated using conventional semiconductor fabrication processes.

One packaging form suitable for thin-film heat management is the flip-chip package, which is one of several package forms in which power-semiconductor devices are housed. Flip chip is a method for interconnecting semiconductor devices, such as IC chips and micro-electromechanical systems, to external circuitry with solder bumps that have been deposited onto the chip pads.

It is possible to package power devices in a flip-chip format or a flip-chip format that approaches surface-mount processes. The flip-chip bumping process offers an opportunity to integrate thermal functionality close to the heat source using thin-film thermoelectric technology.

Thermal Copper Pillar Bump

The core technology for this new thermal-management paradigm is the thermal copper pillar bump, which is also referred to as the "thermal bump." The thermal bump is a thermoelectric structure made from a thin-film thermally active material that is embedded into flip-chip interconnects (in particular, copper pillar solder bumps) for use in electronics packaging. The thermal bump is compatible with the existing flip-chip manufacturing infrastructure, extending the use of conventional solder-bumped interconnects to provide active, integrated cooling of a flip-chipped component using the widely accepted copper pillar bumping process.

The thermal bump was developed as a method for integrating active thermal-management functionality at the chip level in the same manner that transistors, resistors and capacitors are integrated in conventional circuit designs today. Unlike conventional solder bumps that provide an electrical path and a mechanical connection to the package, thermal bumps act as solid-state heat pumps and add thermal-management functionality locally on the surface of a semiconductor chip or other electrical component.

Thermal bumps today are already extremely small. They are 238 μm in diameter by 60 μm high, and have the capability to be scaled to different sizes. The size advantage of the thermal bump enables the integration of thermal-management capabilities at the wafer, die or package levels.

The thermal bump makes use of the thermoelectric effect, which is the direct conversion of temperature differences to an electrical voltage and vice versa. Simply put, a thermoelectric device creates a current flow when there is a temperature difference on each side of the device. Or,

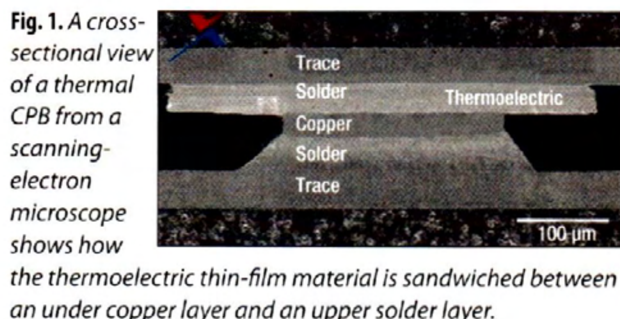

Fig. 1. *A cross-sectional view of a thermal CPB from a scanning-electron microscope shows how the thermoelectric thin-film material is sandwiched between an under copper layer and an upper solder layer.*

alternatively when a voltage is applied to it, a temperature difference is created. This effect can be used to generate electricity, to measure temperatures, to cool objects or to heat them.

For each bump, thermoelectric cooling occurs when a dc current is passed through the bump. The thermal bump pulls heat from one side of the device and transfers it to the other as current is passed through the material. This is known as the Peltier effect. The direction of heating and cooling is determined by the direction of current flow and the sign of the majority electrical carrier in the thermoelectric material.

When combined with a feedback mechanism, the temperature of a target surface can be controlled and maintained by systematically toggling the direction of the current flow.

The use of thermal bumps in power electronics offers many advantages in terms of size, efficiency and power-pumping capability. The bump adds as little as 100 µm of thickness to a heat spreader, enabling unobtrusive integration close to the heat source.

Thermal bumps have been shown to achieve a temperature differential of 60°C between the top and bottom headers and have demonstrated power-pumping capabilities exceeding 150 W/cm^2. This makes thermal bumps ideally suited for applications involving high heat-flux flows.

CPB Structure

Fig. 1 shows a scanning-electron microscope cross-section view of a thermal bump. The bump is structurally identical to a copper pillar bump (CPB) except that it has an extra layer, the thermoelectric layer, incorporated into the stackup. The addition of this layer transforms a standard CPB into a thermal bump. When properly configured electrically and thermally, this element provides active thermoelectric heat transfer from one side of the bump to the other side. The direction of heat transfer is dictated by the doping type of thermoelectric material (either a p-type or an n-type semiconductor) and the direction of electrical current passing through the material.

Fig. 2 shows a schematic of a typical CPB and a thermal bump for comparison. These structures are similar, with both having copper pillars and solder connections. The primary distinction between the two is the introduction of either a p-type or an n-type thermoelectric layer between

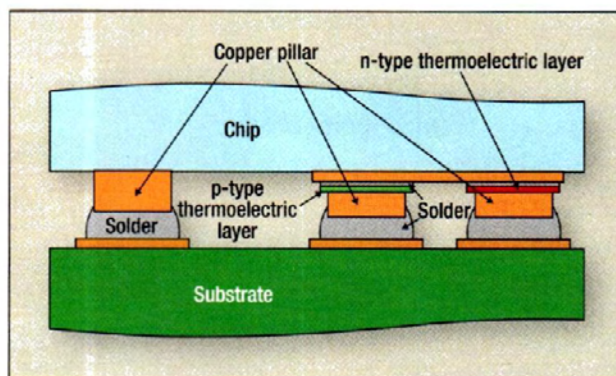

Fig. 2. *A copper pillar bump can be built next to a p-type and an n-type pillar bump. The p-type and n-type bumps together make up a pn couple that, when connected in series electrically, provides for either Peltier cooling or Seebeck power generation.*

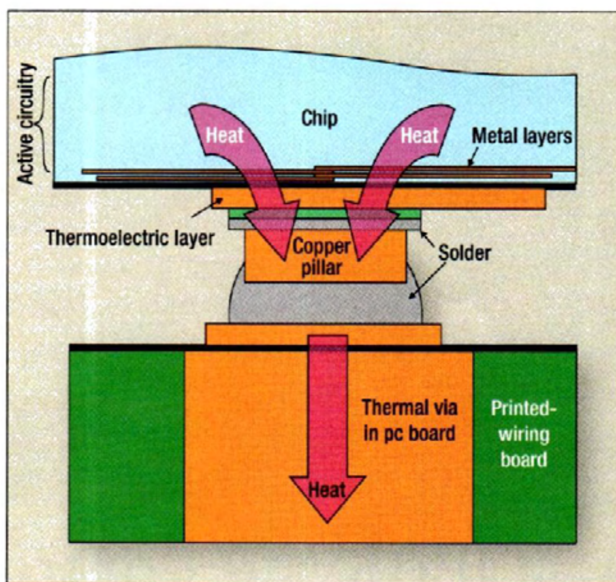

Fig. 3. *A closeup of a CPB shows the flow of heat through a thermal bump. Also shown are the multilayer metal traces often used in complex ICs. These metal layers would be beneficial for gathering heat from larger areas and funneling it into the thermal bump, reducing the thermal-constriction resistance in the circuit. A thermal via is shown in the printed-wiring board for an improved heat-rejection path.*

two solder layers. The solders used with CPBs and thermal bumps can be any one of several commonly used tin-based solders.

Fig. 3 shows a device equipped with a thermal bump. The thermal flow is shown by the arrows labeled "heat." Metal traces, which can be several micrometers high, can be stacked or interdigitated to provide highly conductive pathways for collecting heat from the underlying circuit and funneling that heat to the thermal bump.

The metal traces shown in Fig. 3 for conducting electrical current into the thermal bump may or may not be directly connected to the circuitry of the chip. In the case

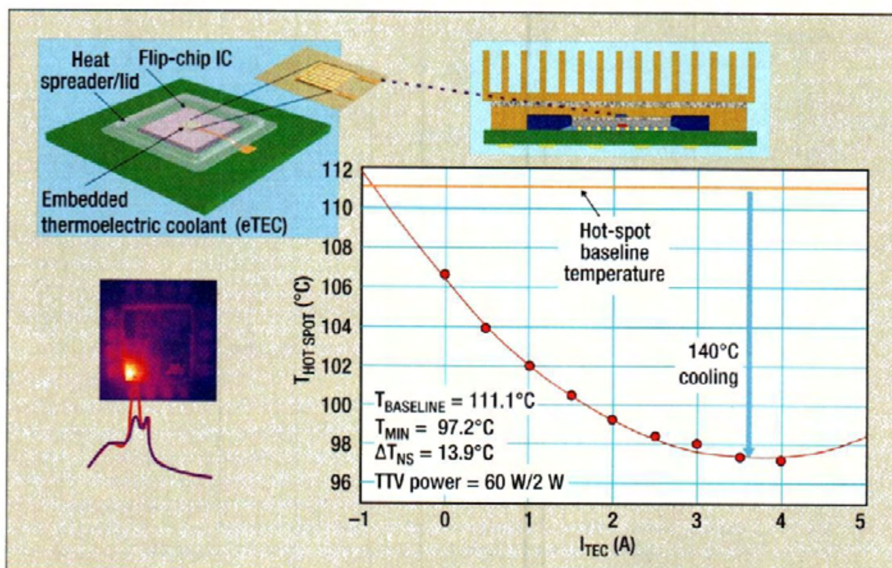

Fig. 4. *Backside cooling can be enhanced by introducing thermal bumps either into the heatsink, to form an active heatsink, or into the heat spreader.*

where there are electrical connections to the chip circuitry, on-board temperature sensors and driver circuitry can be used to control the thermal bump in a closed-loop fashion to maintain optimal performance. The heat that is pumped by the thermal bump and the additional heat created by the thermal bump in the course of pumping that heat will need to be rejected into the substrate or board.

Since the performance of the thermal bump can be improved by providing a good thermal path for the rejected heat, it is beneficial to provide high thermally conductive pathways on the backside of the thermal bump. The substrate could be a highly conductive ceramic substrate like aluminum nitride or a metal with a dielectric like copper, copper-tungsten or copper-molybdenum. In this case, the high thermal conductance of the substrate will act as a natural pathway for the rejected heat.

The substrate might also be a multilayer substrate like a printed-wiring board designed to provide a high-density interconnect. In this case, the thermal conductivity of the printed-wiring board may be relatively poor. Additionally, adding thermal vias (e.g., metal plugs) can provide excellent pathways for the rejected heat.

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IXTP28P065T	-65V	-28A	0.045Ω	46nC	TO-220
IXTA24P085T	-85V	-24A	0.065Ω	41nC	TO-263
IXTP18P10T	-100V	-18A	0.120Ω	39nC	TO-220
IXTA44P15T	-150V	-44A	0.065Ω	175nC	TO-263
TrenchP™ P-Channel Power MOSFETs					
IXTA52P10P	-100V	-52A	0.050Ω	60nC	TO-263
IXTP36P15P	-150V	-36A	0.110Ω	55nC	TO-220
IXTH48P20P	-200V	-48A	0.085Ω	103nC	TO-247
IXTA10P50P	-500V	-10A	1.000Ω	50nC	TO-263
IXTH16P60P	-600V	-16A	0.720Ω	92nC	TO-247

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3-D Cooling

Combining thermal bumps with a 3-D chip stack structure will lead to thermal-management solutions that are also of a 3-D nature. By extending the only currently available option of passive backside cooling to also include active backside cooling, front-side heat removal as well as lateral heat removal, thermal management of the 3-D stack is significantly enhanced.

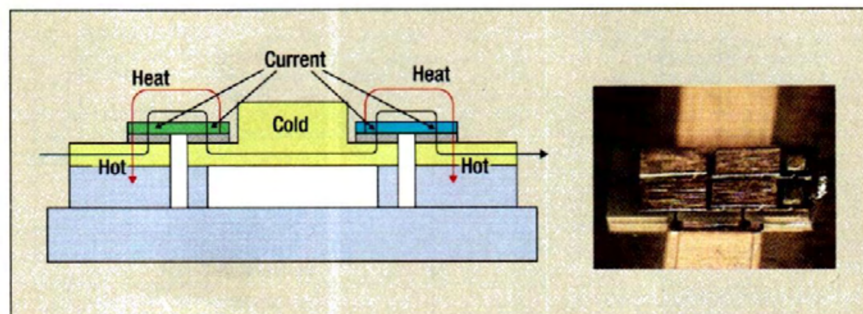

Fig. 5. *The lateral heat removal can be combined with an interposer, through which the heat can be removed.*

Backside cooling can be enhanced by the introduction of thermal bumps either into the heatsink to form an active heatsink or into the heat spreader. Fig. 4 illustrates this approach. In the figure, discrete devices are used to mitigate hot spots generated on the front side of a die. In fact, while the following example demonstrates the feasibility of hot-spot cooling using integrated thermoelectric cooling, it also reveals the limitations of cooling the hot spot from the backside of the die.

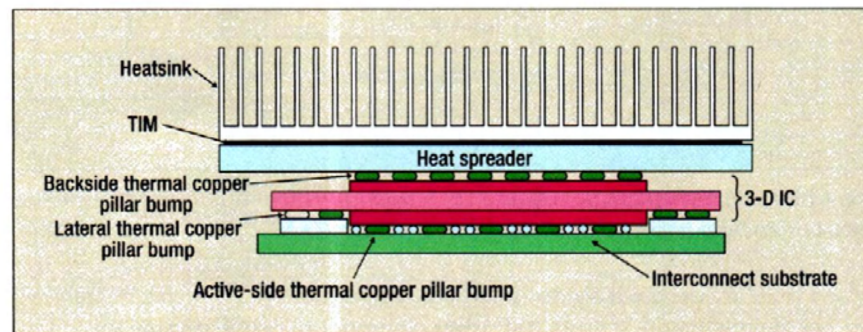

Fig. 6. *This is an integrated 3-D thermal management solution.*

The hot spot is on the active side of the die, while the cooling device is attached to the copper heat spreader. The heat spreader is flipped onto the backside of the die, so that the cooler is located near the backside of the die, behind the first-level thermal interface material (TIM1).

In this specific example, the entire chip dissipates 62 W, with 2 W generated by the hot spot, resulting in a hot-spot heat flux of 1250 W/cm². The baseline temperature in the area of the hot spot without the thermoelectric cooler is about 111°C. In this example, the integrated thin-film cooler reduced hot-spot temperature by up to 14°C.

Fig. 5 illustrates the concept and implementation in practice for lateral heat removal. Here, the current flows from left to right, but the heat flows from the center of the module outwards.

For a 3-D chip stack, this lateral heat-removal concept can be combined with an interposer through which the heat can be removed. Here the thermoelectric material is underneath the substrate, and the heat is pulled from the center segment to the side. Therefore, the center of the platform will be cool, and the sides will be hotter as shown in Fig. 5. With this approach, heat is dissipated laterally to the walls.

The last approach is active-side cooling. In Fig. 6, an artist's rendition depicts the active side of a microprocessor. The smaller structures represent conventional copper pillar bumps next to the larger thermal bump. There could be as few as 10 to 20 or as many as 600 to 1200 thermal bumps strategically placed on the chip only in the vicinity of the hot spots. By doing so, it is not necessary to use a large amount of thermoelectric material — as little as 1 mm × 1 mm per hot spot — to achieve the desired cooling effect with a higher efficiency.

Optimal Cooling

The integration of high heat-flux thermal management solutions into the electronics packaging process is essential to higher operating efficiencies in power devices. Thin-film thermoelectric materials — for example, thermally active CPBs embedded in flip-chip packages — are an ideal solution. By combining thermally active CPBs with a 3-D chip stack structure, heat management is further enhanced via passive and active backside cooling, as well as front-side and lateral heat removal. Thermally active CPBs enable optimal cooling in a highly efficient, cost-effective manner. **PETech**

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