DESIGNING WITH THERMAL IMPEDANCE

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ABSTRACT

Power switching techniques used in many modern control systems are characterized by single or repetitive power pulses, which can reach several hundred watts each. In these applications where the pulse width is often limited to a few milleseconds, cost effective thermal design considers the effect of thermal capacitance. When this thermal capacitance is large enought, it can limit the junction temperature to within the ratings of the device even in the presence of high dissipation peaks. This paper discusses thermal impedance and the main parameters influencing it. Empirical measurements of the thermal impedance of some standard plastic packages showing the effective thermal impedance under pulsed conditions are also presented.

INTRODUCTION

Power switching applications are becoming very common in many industrial, computer and automotive ICs. In these applications, such as switching power supplies and PWM inductive load drivers, power dissipation is limited to short times, with single or repeated pulses. The normal description of the thermal performance of an IC package, Rth(j -a) (junction to ambient thermal resistance), is of little help in these pulsed applications and leads to a redundant and expensive thermal design.

This paper will discuss the thermal impedance and the main factors influencing it in plastic semiconductor packages. Experimental evaluations of the thermal performance of small signal, medium power, and high power packages wil be presented as case examples. The effects of the thermal capacitance of the packages when dealing with low duty cycle power dissipation will be presented and evaluated in each of the example cases.

THERMAL IMPEDANCE MODEL FOR PLASTIC PACKAGES

The complete thermal impedance of a device can be modeled by combining two elements, the thermal resistance and the thermal capacitance.

The thermal resistance, Rth, quantifies the capability of a given thermal path to transfer heat. The general definition of resistance of the thermal path, which includes the three different modes of heat dissipation (conduction, convection and radiation), is the ratio between the temperature increase above the reference and the heat flow, DP, and is given by the equation :

$$R_{th} = \frac{\Delta T}{\Delta P} = \frac{\Delta T}{\frac{\Delta Q}{\Delta t}}$$

Where : ΔQ = heat
Δt = time

Thermal capacitance, C_{th}, is a measure of the capability of accumulating heat, like a capacitor accumulates a charge. For a given structural element, C_{th} depends on the specific heat, c, volume V, and density d, according to the relationship :

$$C_{th} = c\ d\ V$$

The resulting temperature increase when the element has accumulated the heat Q, is given by the equation :

$$\Delta T = \Delta Q / C_{th}$$

The electrical analogy of the thermal behaviour for a given application consisting of an active device, package, printed circuit board, external heat sink and external ambient is a chain of RC cells, each having a characteristic time constant :

$$\tau = RC$$

To show how each cell contributes to the thermal impedance of the finished device consider the simplified example shown in figure 1. The example device consists of a dissipating element (integrated circuit) soldered on a copper frame surrounded by a plastic compound with no external heat sink. Its equivalent electrical circuit is shown in figure 2.

The first cell, shown in figure 2, represents the thermal characteristics of the silicon itself and is characterized by the small volume with a correspondingly low thermal capacitance, in the order of a few mJ/C. The thermal resistance between the junction and

the silicon/slug interface is of about 0.2 to 2 °C/W, depending on die size and on the size of the dissipating elements existing on the silicon. The time constant of this cell is typically in the order of a few milliseconds.

The second cell represents the good conductive path from the silicon/frame interface to the frame periphery. In power packages, where the die is often soldered directly to the external tab of the package, the thermal capacitance can be large. The time constant for this cell is in the order of seconds.

From this point, heat is transferred by conduction to the molded block of the package, with a large thermal resistance and capacitance. The time constant of the third cell is in the order of hundreds of seconds.

After the plastic has heated, convection and radiation to the ambient starts. Since a negligible capacitance is associated with this phase, it is represented by a purely resistive element.

When power is switched on, the junction temperature increase is ruled by the heat accumulation in the cells, each following its own time constant according with the equation :

$$\Delta T = R_{th}\, P_d\, [1 - e^{(t/\tau)}]$$

The steady state junction temperature, T_j, is a function of the $R_{th\ (j\ a)}$ of the system, but the temperature increase is dominated by thermal impedance in the transient phase, as is the case in switching applications.

A simplified example of how the time constants of each cell contribute to the temperature rise is shown in figure 3 where the contribution of the cells of figure 2 is exaggerated for a better understanding.

When working with actual packages, it is observed that the last two sections of the equivalent circuit are not as simple as in this model and possible changes will be discussed later. However, with switching times shorter than few seconds, the model is sufficient for most situations.

Figure 1 : Simplified Package Outline.

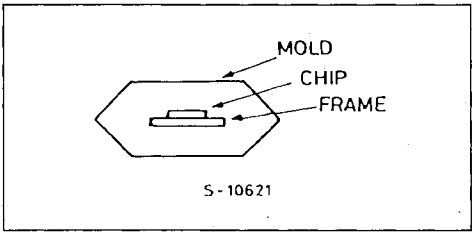


Figure 2 : Equivalent Thermal Circuit of Simplified.

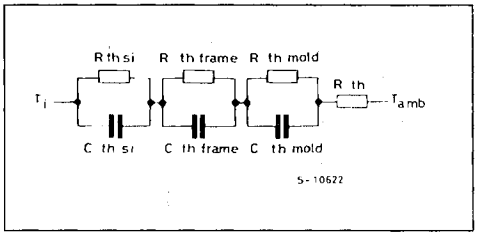
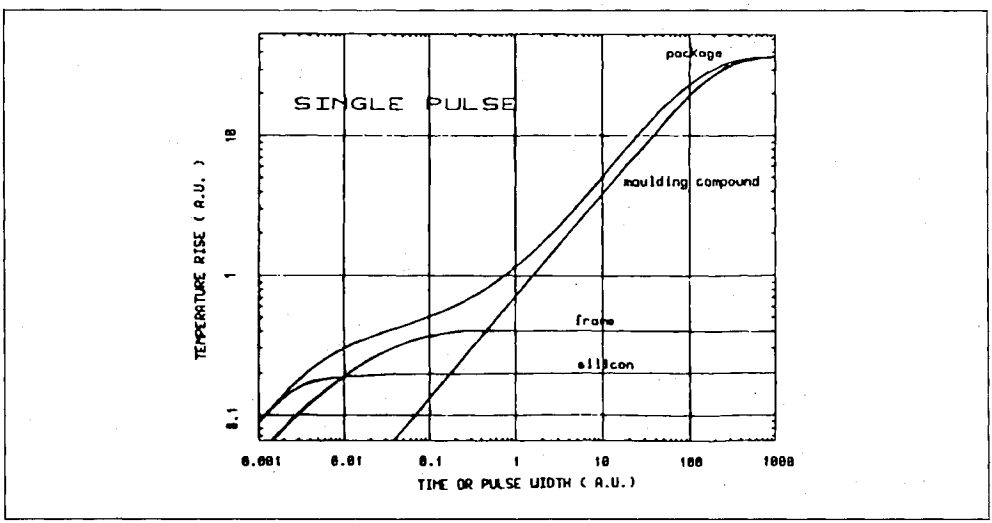


Figure 3 : Time Constant Contribution of Each Thermal Cell (qualitative example).



EXPERIMENTAL MEASUREMENTS

When thermal measurements on plastic packages are performed, the first consideration is the lack of a standard method. At present, only draft specifications exist, proposed last year and not yet standardized (1).

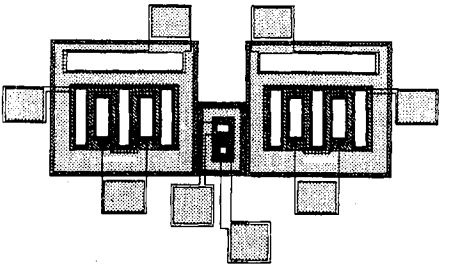
The experimental method used internally for evaluations since 1984 has anticipated these preliminary recomendations to some extent, as it is based on test patterns having, as dissipating element, two power transistors and, as measurement element, a sensing diode placed in the thermal plateau arising when the transistors are biased in parallel.

The method used has been presented elsewhere (2) for the pattern P432 (shown in figure 4), which uses two small (1000 sq mils) bipolar power transistors and has a maximum DC power capability of 40 W (limited by second breakdown of the dissipating elements).

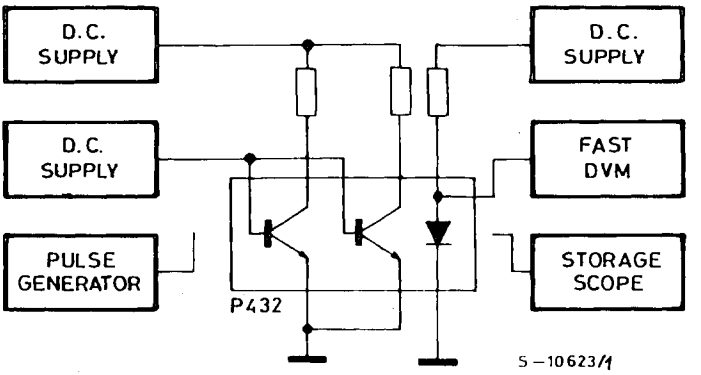
A similar methodology was followed with the new H029 pattern, based on two D-Mos transistors (3) having a total size of 17.000 sq mils and a DC power capability of 300 W on an infinite heat sink at room temperature (limited by thermal resistance and by max operating temperature of the plastics).

Figure 4.

a) P432 Test Die



b) P432 Measurement System

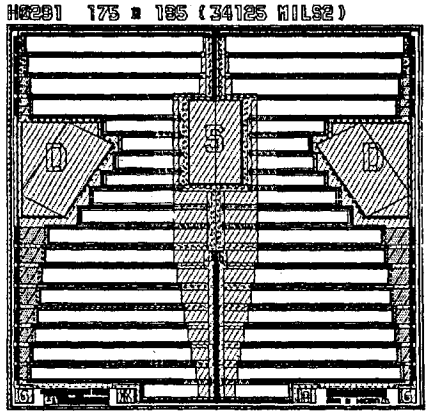


Using the thermal evaluation die, four sets of measurements were performed on an assortment of insertion and surface mount packages produced by SGS-Thomson Microelectronics. The complete characterization is available elsewhere (4). The four measurements taken were :

1) Junction to Case Thermal Resistance (Power Packages)
2) Junction to Ambient Thermal Resistance
3) Transient Thermal Impedance (Single Pulse)
4) Peak Transient Thermal Impedance (Repeated Pulses)

Figure 5.

a) H029 Test Die



b) H029 Measurement System

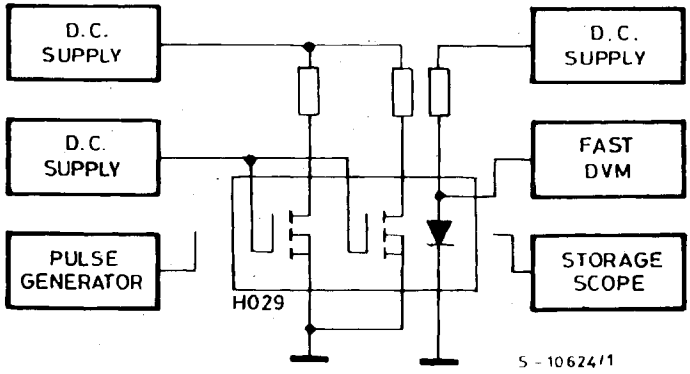
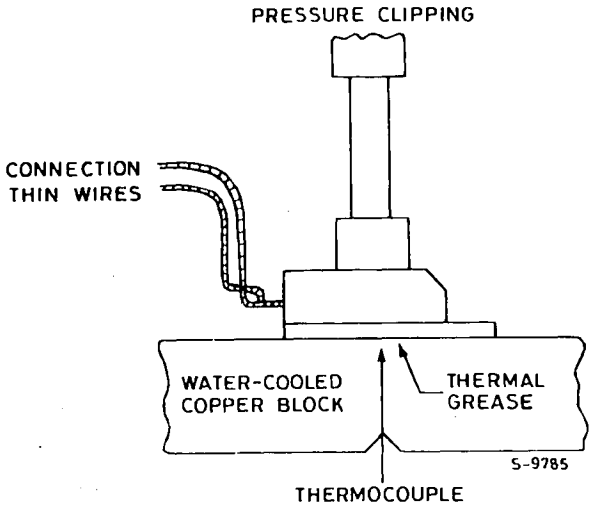


Figure 6 : Set-up for $R_{th\ (j-c)}$ Measurement.

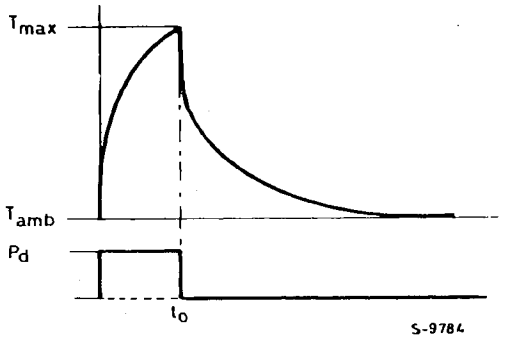


The junction to case thermal resistance measurements were taken using the well known setup shown in figure 6 where the power device is clamped against a large mass of controlled temperature.

The junction to ambient thermal resistance in still air, was measured with the package soldered on standard test boards, described later, and suspensed in 1 cubic foot box, to prevent air movement.

The single pulse transient thermal impedance was measured in still air by applying a single power pulse of duration t_0 to the device. The exponential temperature rise in response to the power pulse is shown qualitetively in figure 7. In the presence of one single power pulse the temperature, ΔT_{max}, reached at time t_0, is lower than the steady state temperature calculated from the junction to ambient thermal resistance. The transient thermal impedance R_o, is obtained from the ratio $\Delta T_{max}/Pd$.

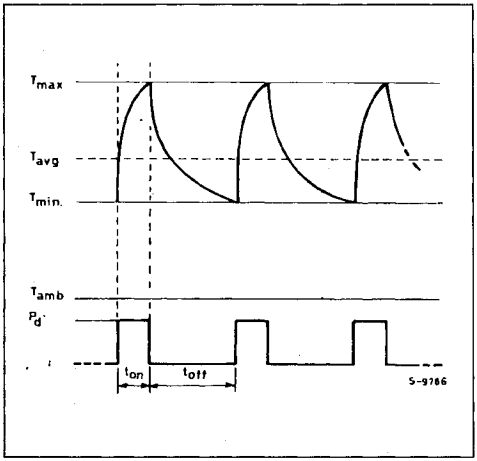
Figure 7 : Transient Thermal Response for a Single Pulse.



The peak transient thermal impedance for a series of repetitive pulses was measured by applying a string of power pulses to the device in free air. When power pulses of the same height, P_d, are repeated with a given duty cycle, DC, and the pulse length, t_p, is shorter than the total time constant of the system, the train of pulses is seen as a contiuous source with mean power level given by the equation :

$$P_{davg} = P_d \, DC$$

Figure 8 : Transient Thermal Response for Repetitive Pulses.



On the other hand, the silicon die has a thermal time constant of 1 to 2 ms and the die temperature is able to follow frequencies of some kHz. The result is that T_j oscillates about the average value :

$$\Delta T_{javg} = R_{th} \, P_{davg}$$

The resulting die temperature excursions are shown qualitatively in figure 8. The peak thermal impedance, R_{thp}, corresponding to the peak temperature, DT_{max}, at the equilibrium can be defined :

$$R_{thp} = \Delta T_{max}/P_d = F\,(t_p, DC)$$

The value of R_{thp} is a function of pulse width and duty cycle. Knowledge of R_{thp} is very important to avoid a peak temperature higher than specified values (usually 150°C).

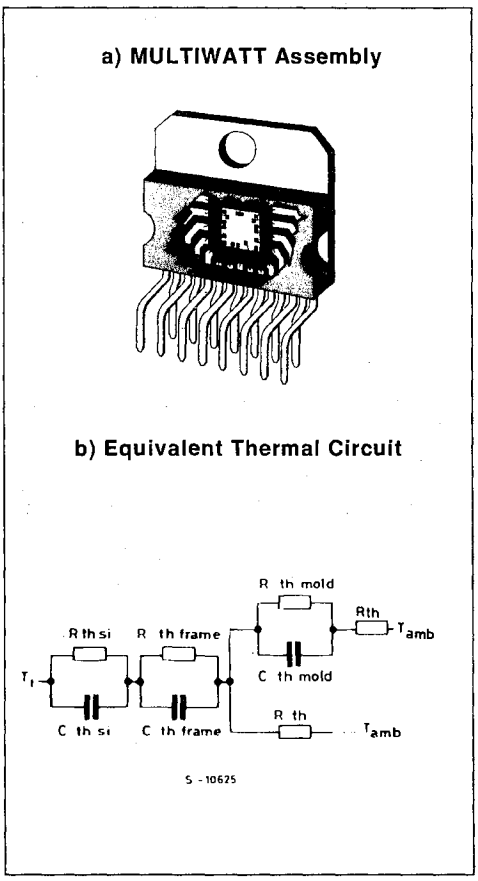
EXPERIMENTAL RESULTS

The experimental measurements taken on several of the packages tested are summarized in the following sections.

MULTIWATT PACKAGE

The MULTIWATT (R) package, shown in figure 9a, is a multileaded power package in which the die is attached directly to the tab of package using a soft solder (Pb/Sn) die attach. The tab of the package is a 1.5 mm thick copper alloy slug. The thermal model of the MULTIWATT, shown in figure 9b, is not much different from that shown in figure 2. The main difference being that when heat reaches the edge of the slug, two parallel paths are possible ; conduction towards the molding compound, and convection and radiation towards the ambient. After a given time, convection and radiation taked place from the plastic.

Figure 9.



Using the two test die, the measured junction to case thermal resistance is :

P432 $R_{th\,(j\,c)} = 2°C/W$

H029 $R_{th\,(j\,c)} = 0.4°C/W$

The measured time constant is approximately 1 ms for each of the two test patterns, but the two devices have a different steady state temperature rise.

The second cell shown in figure 9 is dominated by the large thermal mass of the slug. The thermal resistance of the slug, R_{thslug} is about 1 °C/W and the thermal time constant of the slug is in the order of 1 second.

The third RC cell in the model has a long time constant due to the mass of the plastic molding and its low thermal conductivity. For this cell the steady state is reached after hundreds of seconds.

For the MULTIWATT the DC thermal resistance of the package in free air, $R_{th\,j\,a}$, is 36 °C/W with the P432 die and 34.5°C/W with the H029 die.

Figure 10 shows the single pulse transient thermal impedance for the MULTIWATT with both the P432 and H029 test die. As can be seen on the graph, the package is capable of high dissipation for short periods of time. For a die like the H029 the power device is capable of 700 to 800 W for pulse widths in the range of 1 to 10 ms. For times up to a few seconds the effective thermal resistance for a single pulse is still in the range of 1 to 3 °C/W.

The peak transient thermal impedance for the MULTIWATT package containing the P432 die in free air is shown in figure 11.

POWER DIP PACKAGE

The power DIP package is a derivative of standard small signal DIP packages with a number of leads connected to the die pad for heat transfer to external heat sinks. With this technique low cost heat sinks can be integrated on the printed circuit board as shown in figure 12a. The thermal model of the power DIP, shown in figure 12b accounts for the external heat sink on the circuit board by adding a second RC cell in parallel with the cell corresponding to the molding compound.

In this model, the second cell has a shorter time constant than for the MULTIWATT package, due in large part to the smaller quantity of copper in the frame (the frame thickness is 0.4 mm compared to 1.5 mm). Thus the capacitance is reduced and the resistance increased.

The increased thermal impedance due to the frame can partially be compensated by a better thermal exchange to the ambient by adding copper to the heat sink on the board. The DC thermal resistance between the junction and ambient can be reduced to the same range as the MULTIWATT package in free air, as shown in figure 13.

Figure 10 : Transient Thermal Response MULTIWATT Package.

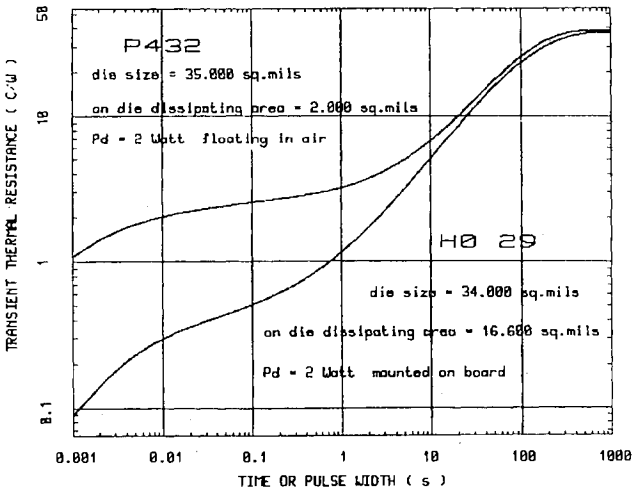


Figure 11 : Peak Thermal Resistance MULTIWATT Package.

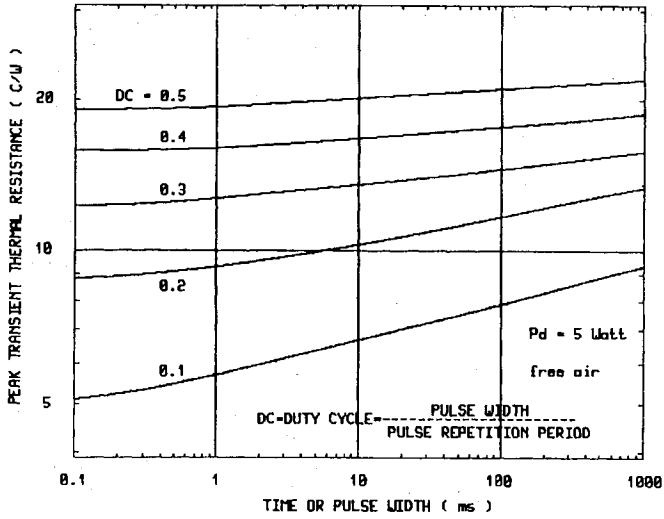
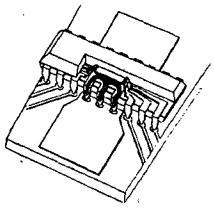
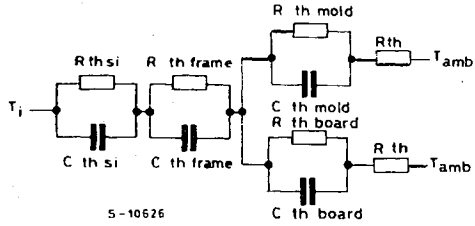


Figure 12.

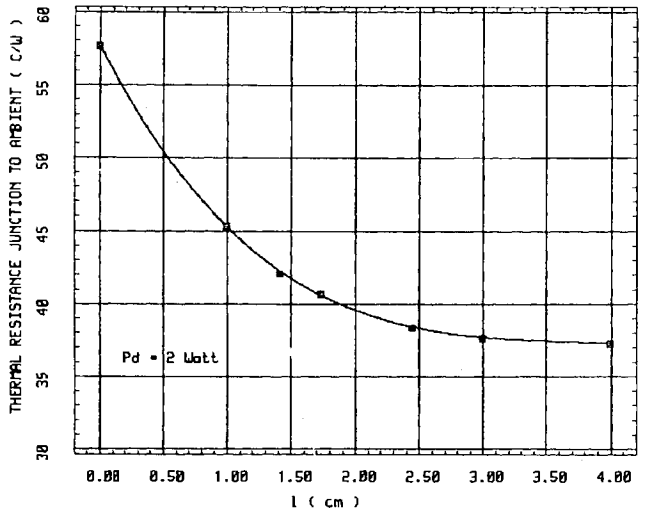


a) Power DIP Package



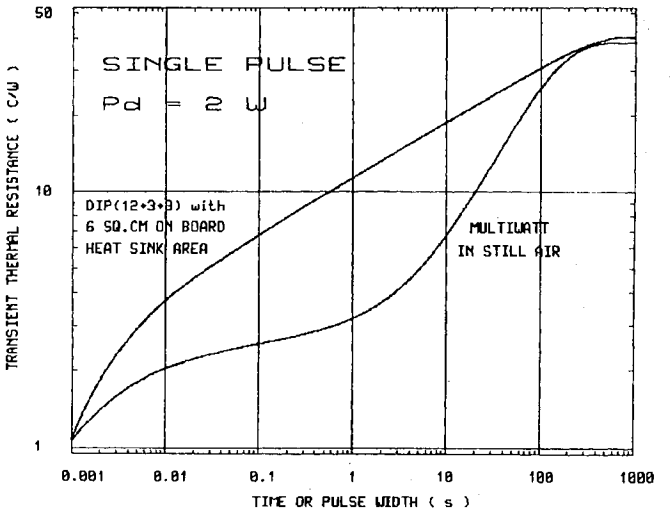
b) Equivalent Thermal Circuit

Figure 13 : Rth (j – a) vs. PCB Heat Sink Size 12 + 3 + 3 Power Dip.



As a comparison, figure 14 compares the thermal performance of the power DIP and the MULTIWATT package. It is clearly seen that even though the DC thermal resistance may be similar, the MULTIWATT is superior in its performance for pulsed applications.

Figure 14 : Transient Thermal Impedance for Single Pulses in Power DIP and MULTIWATT Packages.



STANDARD SIGNAL PACKAGES

In standard, small signal, packages the easiest thermal path is from the die to the ambient through the molding compound. However, if a high conductivity frame, like a copper lead frame, is used another path exists in parallel. Figure 15 shows the equivalent thermal model of such a package. The effectiveness of a copper frame in transferring heat to the board can be seen in the experimental results in DC conditions.

Table 1 shows the thermal resistance of some standard signal packages in two different conditions ; with the device floating in still air connected to the measurement circuit by thin wires and the same device soldered on a test board.

Table 1 : Thermal Resistance of Signal Packages

Package	Frame Thickness & Material	Rth (j-a) Floating	°C/W on Board
DIP 8	(0.4 mm Copper)	125-165	78-90
DIP 14	(0.4 mm Copper)	98-128	64-73
DIP 16	(0.4 mm Copper)	95-124	62-71
DIP 20	(0.4 mm Copper)	85-112	58-69
DIP 14	(0.25 mm Copper)	115-147	84-95
DIP 20	(0.25 mm Copper)	100-134	76-87
DIP 24	(0.25 mm Copper)	67-84	61-68
DIP 20	(0.25 mm Alloy 42)	158-184	133-145
SO 14	(0.25 mm Copper)	218-250	105-180
PLCC 44	(0.25 mm Copper)	66-83	48-72

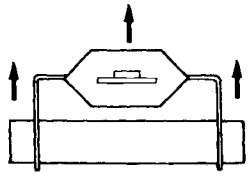
The transient thermal resistance for single pulses for the various packages are shown in figures 16 through 20.

The results of the tests, as shown in the preceding figures, show the true capabilities of the packages. For example, the DIP 20 with a Alloy 42 frame is a typical package used for signal processing applications and can dissipate only 0.5 to 0.7 W in steady state conditions. However, the transient thermal impedance for short pulses is low (11 C/W for t_p = 100 ms) and almost 7 Watts can be dissipated for 100 ms while keeping the junction temperature rise below 80°C.

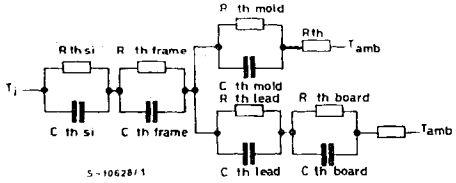
The packages using a 0.4 mm Copper frame have a low steady state thermal resistance, especially in the case of the DIP 20. The thicker lead frame increases the thermal capacitance of the die flag, which greatly improves the transient thermal impedance. In the case of the DIP 20, which has the largest die pad, the transient R_{th} for 100 ms pulses is about 4.3°C/W. This allows the device to dissipate an 18 Watt power pulse while keeping the temperature rise below 80°C.

As with the previous examples the peak transient thermal impedance for repetitive pulses depends on the pulse length and duty cycle as shown in figure 14. With the signal package, however, the effect of the duty cycle becomes much less effective for longer pulses, due primarily to the lower thermal capacitance and hence lower time constant of the frame.

Figure 15.



a) DIP Package Mounted on PCB



b) Equivalent Thermal Circuit DIP Package on PCB

Figure 16 : Transient Thermal Impedance DIP 20 (alloy 42).

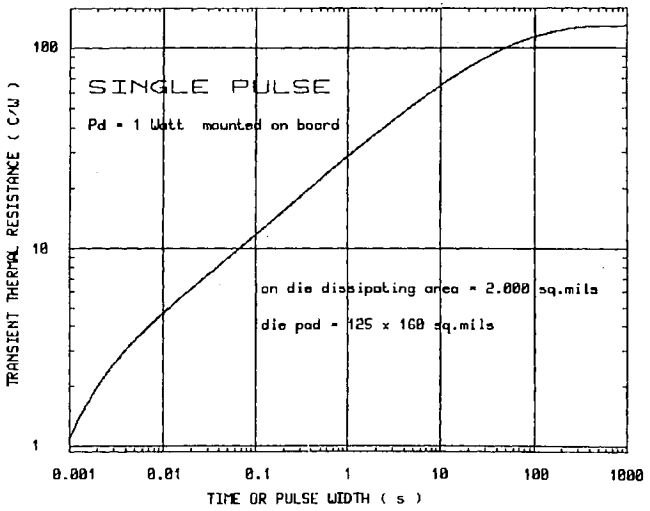


Figure 17 : Transient Thermal Impedance 0.4 mm Copper Frame DIP Packages.

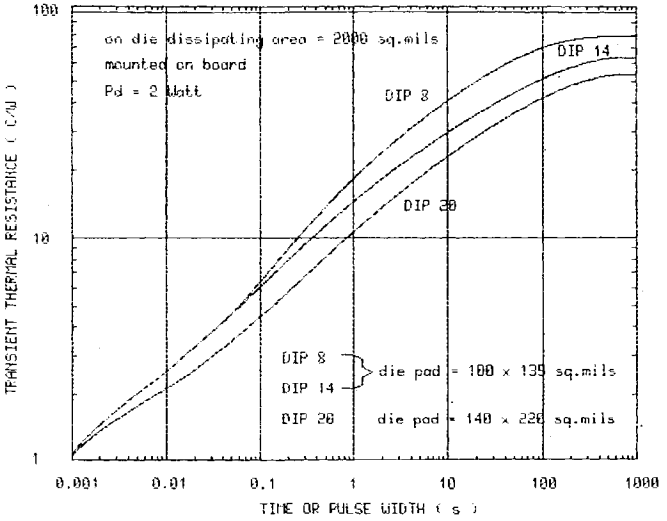


Figure 18 : Transient Thermal Impedance 0.25 mm Copper Frame DIP Packages.

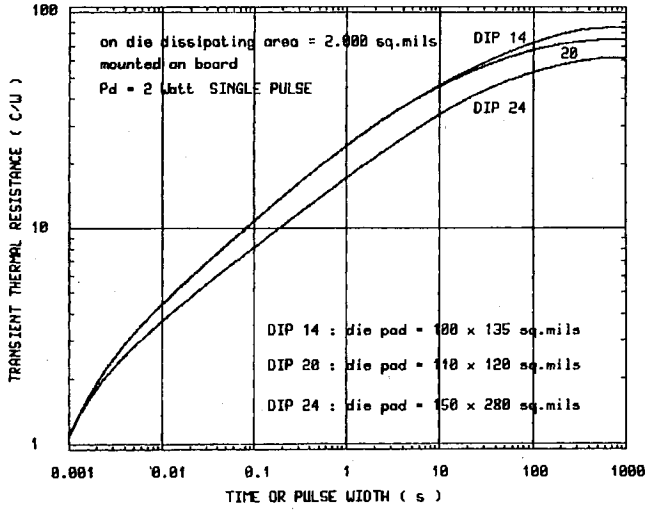


Figure 19 : Transient Thermal Impedance 0.25 mm Frame PLCC Package.

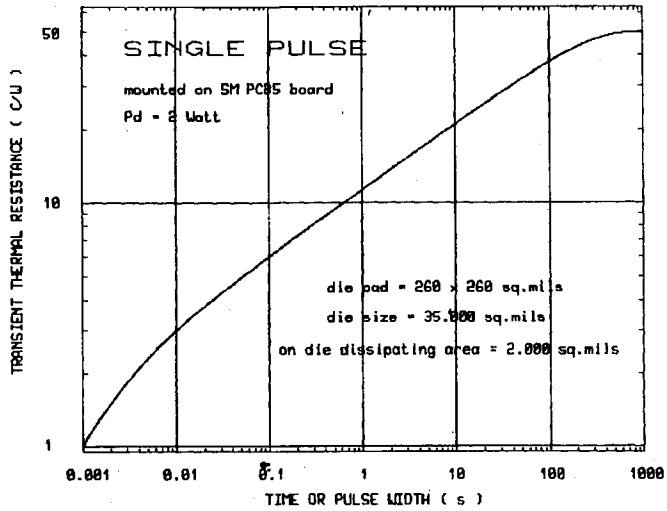


Figure 20 : Transient Thermal Impedance 0.25 mm Copper Frame SO14 Package.

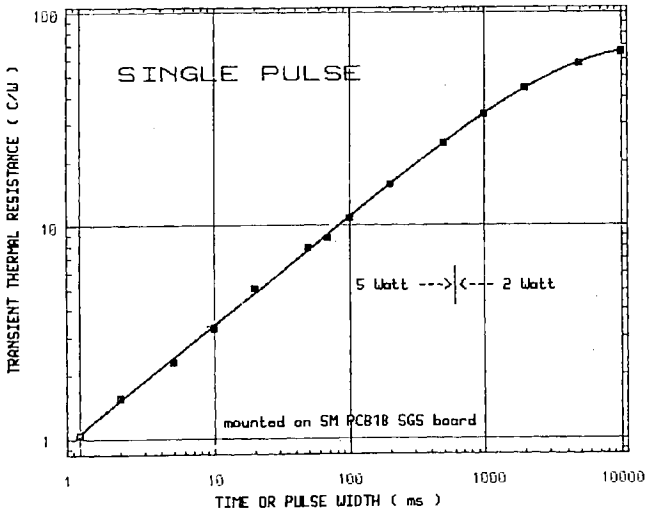
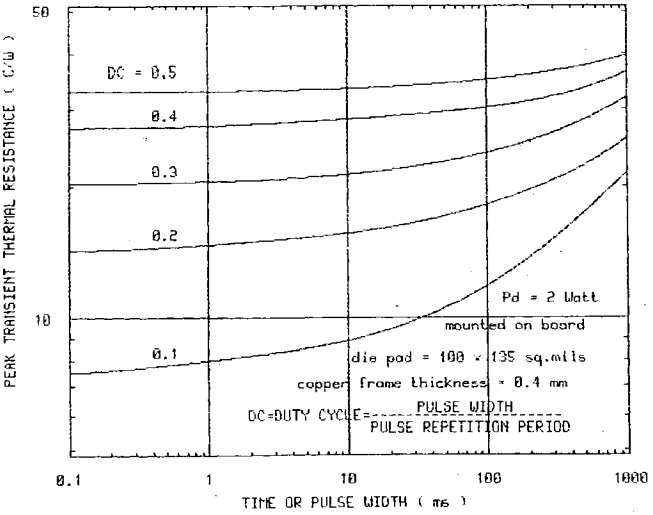


Figure 21 : Peak Thermal Impedance 0.25 mm Copper Frame 14 Lead DIP.



CONCLUSION

This paper has discussed a test procedure for measuring and quantifying the thermal characteristics of semiconductor packages. Using these test methods the thermal impedance of standard integrated circuit packages under pulsed and DC conditions were evaluated. From this evaluation two important considerations arise :

1) The true thermal impedance under repetitive pulsed conditions needs to be considered to maintain the peak junction temperature within the rating for the device. A proper evaluation will result in junction temperatures that do not exceed the specified limits under either steady state or pulsed conditions.

2) The proper evaluation of the transient thermal characteristics of an application should take into account the ability to dissipate high power pulses allowing better thermal design and possibility reducing or eliminating expensive external heat sinks when they are oversized or useless.

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