Switcher adds programmable-PWM-duty-cycle clamp

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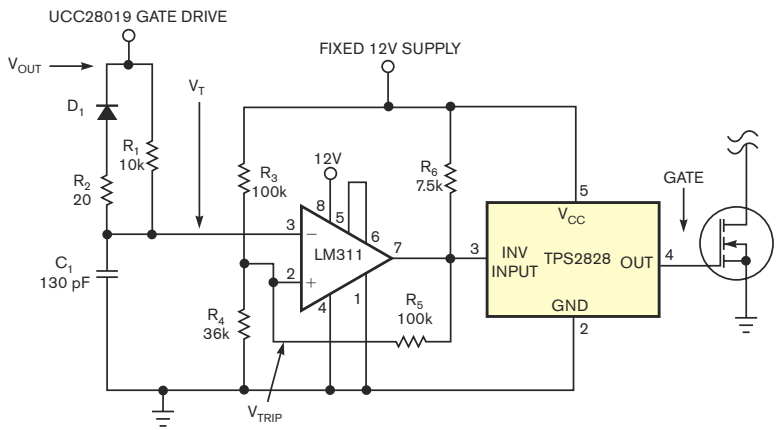

Figure 1 This simple circuit clamps the duty cycle of a switching regulator to 90%.

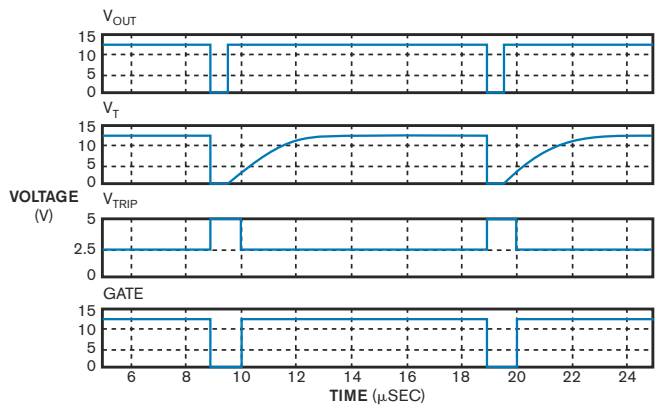

Figure 2 A SPICE simulation of the circuit in Figure 1 shows the clamping action cutting in at 90% duty cycle.

Power-supply applications require the use of a duty-cycle clamp. Such applications include those using current-sense transformers and two-switch forward converters. If a duty-cycle clamp is not present, the transformers could saturate, causing a catastrophic failure in the system. However, to drive down the cost of the design, many power-supply designers use inexpensive, eight-pin PWM controllers that have no duty-cycle clamp. This Design Idea shows how to add an inexpensive duty-cycle clamp to these PWM controllers.

You can add the circuitry to most PWM controllers to provide a programmable duty-cycle clamp (**Figure 1**). The circuitry comprises a few passive components, a hysteretic comparator, and a gate-driver IC. Resistor R_1 and capacitor C_1 program the duty-cycle clamp's dead time. Resistor R_2 and diode D_1 reset the timing circuitry when the output of the PWM controller goes low. Resistors R_3, R_4, and R_5 set the comparator's trip point, V_{TRIP}, at 5V. Resistor R_5 adds −2.5V of hysteresis to the comparator to ensure circuit stability.

The following example shows how to set the circuitry in **Figure 1** for a maximum duty cycle, D_{MAX}, of 0.9. The PWM controller operates at a switching frequency, f_S, of 100 kHz. Most PWM controllers cannot reach 100% duty cycle and have a specified dead time. For this example, the dead time is 300 nsec. To set the timing capacitor also requires knowing the maximum output of the PWM output voltage, V_{OUT}. In this example, the maximum output voltage is 12V. The timing ca-

pacitor is roughly 130 pF. The design uses a standard, 120-pF capacitor. The following **equations** describe the calculations: $t=(1-D_{MAX})(1/f_S)-$dead time$=700$ nsec, and

$$C_1=\frac{-t}{\ln\left(1-\frac{V_{TRIP}}{V_{OUT}}\right)R_1}\approx 130\text{ pF}.$$

A SPICE simulation with the circuitry in **Figure 1** ran to ensure that the duty-cycle clamp works with the circuitry. **Figure 2** shows the results of this simulation. V_{OUT} is the output of the PWM controller, V_T is the voltage at the inverting pin of the comparator, V_{TRIP} is the voltage at the noninverting input of the comparator, and gate is the output of the gate-driver IC. From the waveforms in **Figure 2**, you can see that the duty-cycle clamp appears to be working correctly, clamping the output of the gate driver to 90%.EDN