Single comparator forms frequency doubler

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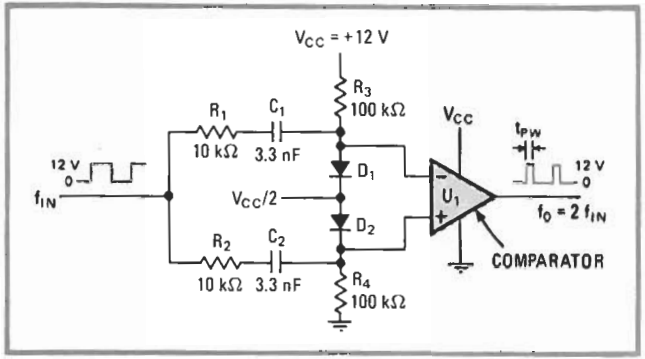
Using just a single comparator chip and a few discrete components, this frequency multiplier produces rectangular pulses at twice the frequency of the input signal. The duration of the output pulses is adjustable and can be made asymmetrical by varying the rising and falling edges of the input signal. Also, the circuit is simple and may be built from off-the-shelf components.

The circuit (see figure) generates a positive pulse of duration t_{pw} on both the rising and falling edges of the input signal. On the rising edge, the inverting input terminal of the comparator is set at $0.5V_{cc}+0.6$ volt by D_1 while the noninverting input terminal rises to the full input voltage. Consequently, the comparator output goes high and remains in that state until C_2 charges to the level where the noninverting terminal is again less than $0.5V_{cc}+0.6$ v. On the pulse's falling edge, the positive terminal of U_1 is set to $0.5V_{cc}-0.6$ v by D_2 and the negative terminal is grounded. Again U_1's output goes high and remains so until C_1 charges to a point where the negative terminal is greater than $0.5V_{cc}-0.6$ v.



Doubler. Single comparator U_1 and a few discrete components yield a frequency doubler that generates a positive pulse of duration t_{pw} on both the rising and falling edges of the input signal. The duration of the pulse (t_{pw}) is adjustable and is given by $K(R_1+R_3)C_1$ for the falling edge and $K(R_3+R_4)C_2$ for the rising edge. For the components shown, t_{pw} measures about 0.31 ms.

Since the input is a square wave and both sections of the circuit are identical, the durations of the output pulse for both the rising and falling edges of the input are the same. In terms of the component values, pulse width $t_{pw} = K(R_1+R_3)C_1$, where K is a constant that is dependent on V_{cc} and the input voltage. □