

Principles of Logic Analysis — 1

This is the first of a short series of articles which give an easy to understand introduction to the basic principles of logic analysis and the use of a logic analyser. It is written for anyone who needs to know more about troubleshooting in digital circuits.

by **WOLFGANG SCHUBERT**

Digital technology has developed dramatically since the first microprocessors were introduced onto the market in the middle of the seventies, and is exerting a continuously increasing influence on all technological areas and thus also on daily life.

Home computers used nowadays as a hobby have a greater performance than the large data processing systems used a few years ago for commercial applications. Traffic lights are controlled depending on requirements and thus contribute to a better flow of traffic. Robots and intelligent manufacturing machines are being used more and more in industry.

The invention of the microprocessor has already been compared with the invention of the wheel, because both products have resulted in revolutionary changes. It is certainly true that digital technology has been developed into a tool just as useful for mankind as the wheel, except that digital technology is far more complex.

The special problems of digital technology result from this complexity — at the time a breakdown occurs. It is easy to see whether a wheel is broken, but in the case of a digital circuit it is necessary to use special test procedures because man is unable to detect the events in such circuits.

Such methods of measurement are referred to as "logic analysis". The purpose of this series of articles is to provide an easy-to-follow insight into the problems associated with measurements on logic circuits and the possible solutions using modern aids such as logic analysers.

Many potential users are not acquainted with the fundamentals necessary to understand logic systems; for this reason logic analysis is considered as "complicated" and "unfathomable". It is hoped that these articles will help to eliminate this deficiency by informing the reader of the principles of logic analysis, thereby enabling him to master complicated measuring problems himself.

The target group includes electronics engineers and students approaching the end of their electrical engineering or computer science studies. The articles are also directed at those in whose fields digital techniques have gained ground (such as mechanical engineers) and who are therefore confronted with measuring problems in logic circuits.

The first article deals with the particular measuring problems associated with logic circuits. Following a discussion of the differences between logic circuits and other electronic circuits and the resulting demands placed on the measuring equipment, the various types of faults in logic circuits will be explained using examples.

The deficiencies of classical instruments such as oscillo-

scopes and voltmeters for measurements in logic circuits will be shown in the second article, by examining where they can be used. The logic analyser proves to be the "made-to-measure" instrument for the special measuring problems associated with logic circuits.

The fundamentals of logic analysis will then be treated in two parts:

- The basic idea of data reduction upon which logic analysis is based.
- Implementation of this basic idea in a logic analyser.

The two basic types of logic analyser, state analyser and timing analyser, will then be presented and their application limits compared.

A basic knowledge of digital techniques is required for understanding these articles; further knowledge of microprocessors is advantageous, but not essential.

Measuring problems in logic circuits

In order to understand what special measuring problems can occur in logic circuits, it is necessary to examine the most important differences between logic circuits (such as microcomputers) and other electronic circuits (such as analog modules). These differences directly result in the demands made on the measuring equipment.

When compared with other circuits the following demands are made on measurements in logic circuits:

There are only very few signals in an analog module such as an amplifier, which are passed on step-by-step (not considering feedback signals) and which depend on one another in a clearly defined manner. Troubleshooting is therefore

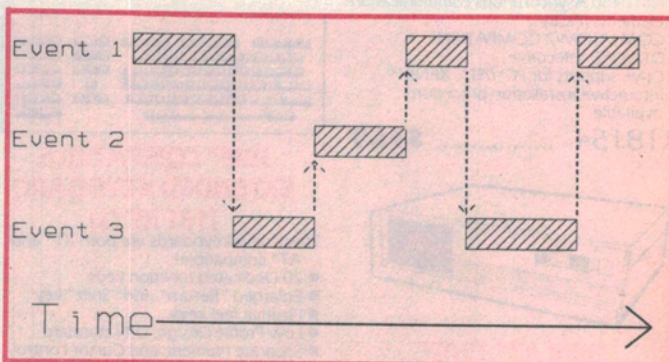
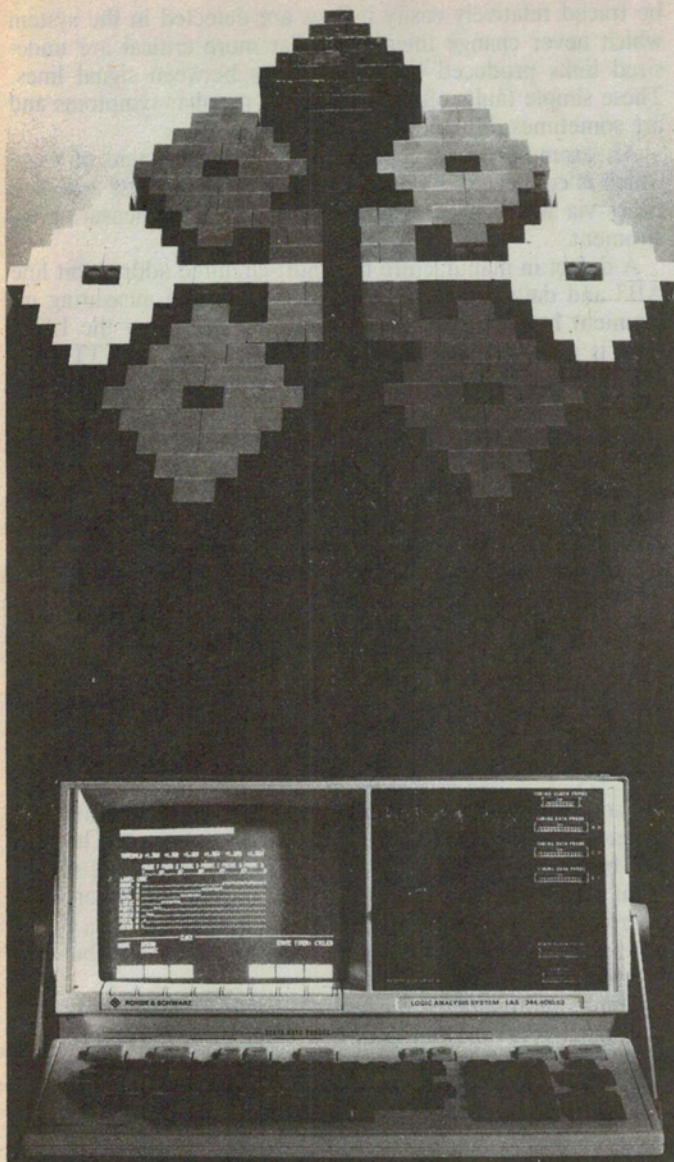


Fig.1: In digital systems, specific processes or events are quite often not continuous.



An example of a modern logic analyser. Like most modern instruments, it is itself based on a microprocessor. (Courtesy Rohde & Schwarz)

relatively simple in such circuits if the circuit is examined starting at its output and then progressing to the input step-by-step until the fault has been found.

In contrast to this there are often very many signals in digital modules which are independent of one another.

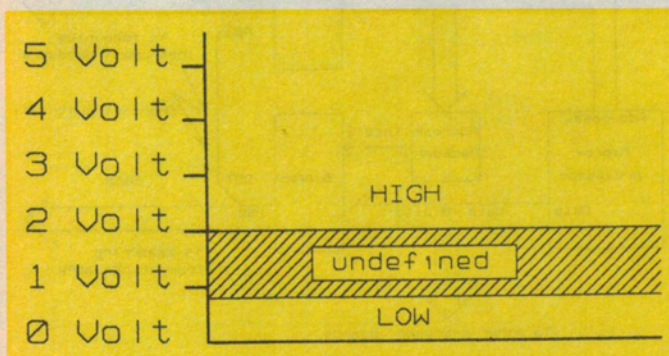


Fig.2: Signal levels in TTL logic circuitry fall into three basic categories: high, low or "undefined".

AB...A15	Eight most significant address bits
AD0...AD7	Eight least significant address bits, multiplexed with data bus
ALE	Address latch enable
S0, S1, IO/M	Machine cycle information
RD/	Read signal
WR/	Write signal
READY	Ready message from peripheral module
HOLD	Hold request from other processor
HLDA	Hold acknowledgement to other processor
INTR	Interrupt input
INTA/	Interrupt acknowledgement
RST5.5, RST6.5, RST7.5	Restart input
TRAP	Non-maskable restart interrupt
RESET IN/	Reset input
RESET OUT	Reset acknowledgement
X1, X2	Crystal connections
CLK	Clock output
SID	Serial data input
SOD	Serial data output

Table 1: Signals associated with the 8085 microprocessor. Although all related to its operation, they are relatively independent.

A standard 8-bit microprocessor such as the 8085 already has more than 30 signals (address bus, data bus and control signals) which are completely independent of one another and must therefore be monitored simultaneously during the measurements.

Another factor adds to the difficulties if this CPU controls a module. All other signals in this module are dependent on the CPU signals, but this dependence is often very difficult to determine because of the storage characteristics of many digital components and the cause of a faulty signal need not necessarily be present when the fault is present, but may already belong to the past.

Initialization belongs to this problem area. If a module is not correctly initialized when switched on, the undefined status of storage components such as flip-flops or RAMs can influence the subsequent response of the module in an unpredictable manner. This effect therefore also depends on the storage characteristics of digital components.

It can be particularly inconvenient when testing computer systems that the examined process is not continuous, but is interrupted at unforeseen times by other processes. This occurs particularly with multi-user or multi-tasking applications. The measuring instrument used must therefore be able to differentiate between the process to be monitored and other processes being executed.

Analog processes can be displayed very well on an oscilloscope if they are periodic. But non-periodic signals are often encountered in computer systems. Some processes important

for fault detection only occur once, and must be immediately detected.

On the other hand, qualitative information on the signal level in logic circuits is often sufficient. Digital circuits operate with only two voltage levels, HIGH and LOW. For example, TTL circuits recognise voltages below 0.8V as LOW and voltages above 2.0V as HIGH. This fact can be used when carrying out measurements in digital circuits by omitting the determination of the exact analog value of a voltage and by simply classifying all voltages into HIGH or LOW level depending on their magnitude relative to a defined threshold value (e.g. 1.4V with TTL).

With this simplification it must always be remembered that the interpretation of an analog signal by the measuring instrument and the device-under-test as LOW or HIGH may be different. Great care is required in the case of signals which lie near the voltage thresholds.

It is usually sufficient to determine the level at discrete points in time. Digital systems are usually clock-controlled. The storage elements in such systems such as flip-flops, memories and processors only accept the data at their inputs at the point in time when a clock pulse or transition "edge" occurs. All changes in signal at the inputs are ignored if those changes occur outside a particular window centred around the active clock edge, with the size of this window being determined by the setup and hold times of the respective circuit components. For this reason it is often permissible to ignore all changes taking place outside this window, when measuring digital circuits.

Troubleshooting

The usual reason for carrying out measurements in a digital circuit is to trace a fault. The most common faults in digital circuits can be divided into two classes: state errors and compatibility errors.

State errors are common to all information processing systems: signals may be faulty without this being recognised by their physical form, i.e., the signals appear to be correct.

The most common faults of this type are stuck-at errors where a signal remains constantly at LOW or HIGH because of a short-circuit or component failure. These faults can still

be traced relatively easily if lines are detected in the system which never change their level. Far more critical are undesired links produced by short-circuits between signal lines. These simple faults often lead to very peculiar symptoms and are sometimes difficult to trace.

An example is the microprocessor in the system of Fig.4 which is connected via a buffer to separate address and data buses via which it accesses the hardware of a measuring instrument.

A defect in manufacture has short-circuited address bit line AB3 and data bit line DB7 on the bus to the measuring instrument hardware. Since the driving capacity for the LOW level is stronger than that for the HIGH level in a TTL circuit, both signals become LOW if either AB3 or DB7 go LOW.

This short-circuit leads to two errors: when writing at particular addresses in the hardware, incorrect data are entered, and when writing particular data, these are applied to incorrect addresses. The following table exemplifies this using four possible write processes.

Address	Data	Response of accessed hardware
51238H	83H	Correct: 83H in 51238H
51237H	23H	Correct: 23H in 51237H
51238H	23H	Incorrect: 23H in 51230H
51237H	83H	Incorrect: 03H in 51237H

These two errors do not always occur, but only if the CPU accesses the hardware of the measuring instrument. The data bus buffer is not switched through to the measuring instrument hardware if the CPU accesses one of the other CPU boards and an interaction between addresses and data therefore does not take place. In this case the system behaves completely normally.

Compatibility errors, the second type of fault are present if the signal level or timing differs from those of correct signals. Such signals are generated for example by crosstalk between lines. Malfunctions may be triggered if the glitches produced exceed the switching threshold of the logic family used.

Level errors may occur because of component failures or mistakes made during circuit development, with the result that the specified HIGH and LOW levels can no longer be

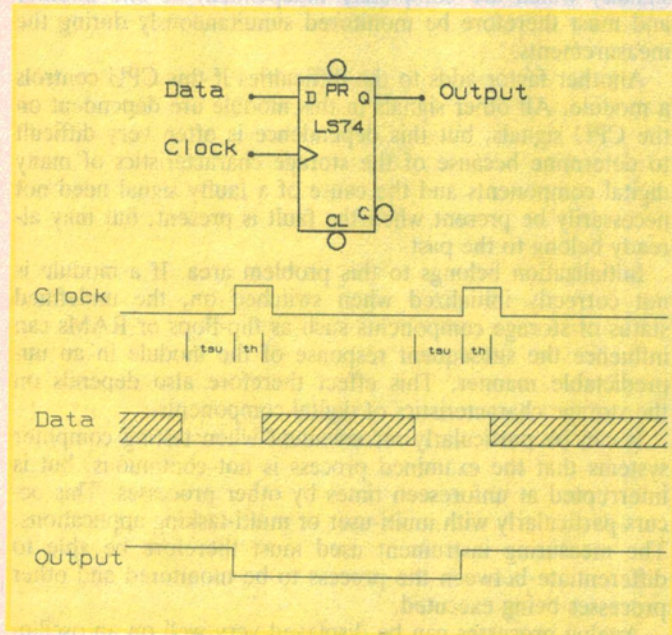


Fig.3: A D-type flipflop as an example of a clock controlled system.

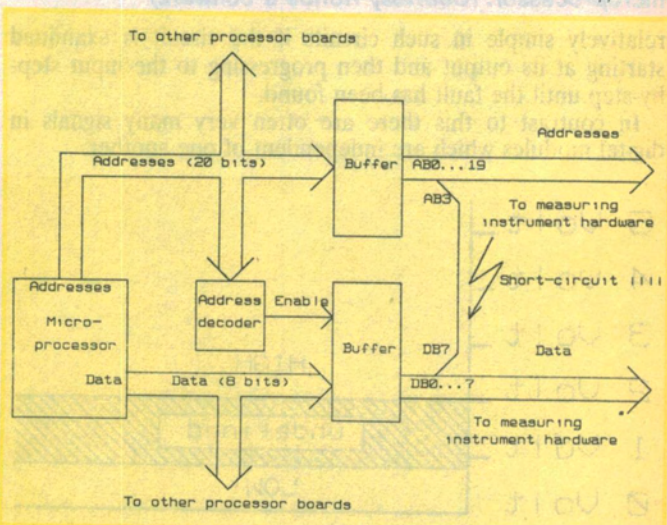


Fig.4: A microprocessor system with a short circuit between address and data lines.

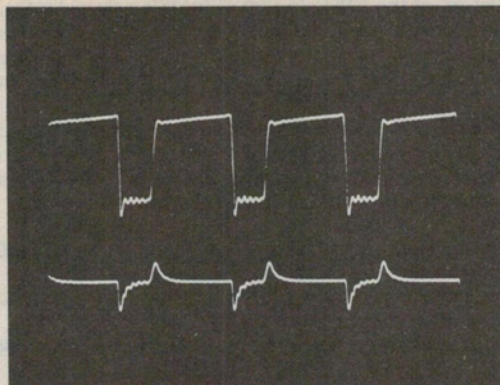


Fig.5: Glitches produced in one signal (bottom) by crosstalk from another (top).

attained on certain lines and other components which use these lines as inputs can no longer respond correctly.

Timing errors where the relationship between several signals is disturbed so that the connected components can no longer operate correctly are very common.

The last two types of error often occur together if the fan-out of the driving circuit is exceeded.

The following example (Fig.6) serves to explain the effects of timing errors when the cross-hatched areas represent undefined status on the address and data buses.

A RAM is written into correctly if the processor first applies the addresses, then the data, then accesses the write-line (see 1) and subsequently removes the data and addresses again. However, if the write pulse is removed too late (see 2 and 3), either incorrect data are applied to the correct address (case 2) or incorrect data are applied to the incorrect address (case 3).

In the last case it can even happen that several undesired write processes are activated simultaneously, because the address bus may be in an undefined level range and the address decoding of the RAM can therefore address several memory cells at once.

Function analysis

It is sometimes necessary to test digital circuits which function fault-free, for example with a view to optimization. A differentiation can be made here between two types of measurements: data flow analysis and performance analysis. With data flow analysis measurements, the data flow is monitored between the source and the acceptor. In a computer-controlled system the processor can be one of the sources or acceptors.

Through measurements on the processor it is possible to analyse the addressing of other system components by the processor, the reading in or outputting of data and the data flow from the program memory to the processor, and thus the program execution.

A further case for measurement is the interface of a computer system to peripheral units. Examples include measure-

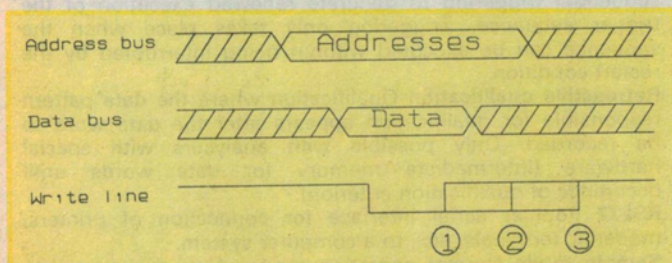


Fig.6: Timing considerations when writing into a RAM.

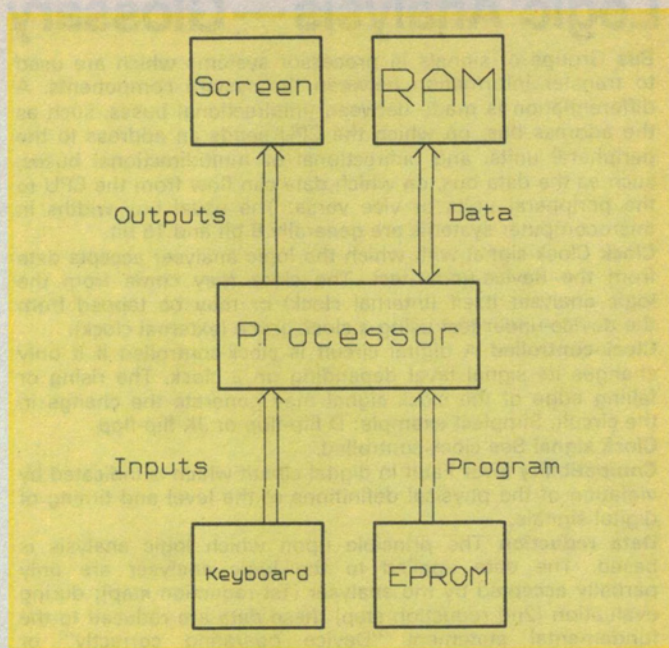


Fig.7: Data flows in a typical computer system.

ments on the IEC bus, RS-232 interface or Ethernet.

With performance analysis, if a qualitative criterion (whether certain data have occurred) is of major importance, this is supplemented in performance analysis by a timing component. The measurement is used to determine whether data have occurred within a specific period. This is important for program optimization where it is necessary to determine the computation time required for certain parts of the program.

All these test functions, which can be grouped together under the term "function analysis", require test equipment able to interpret the data contained in the digital signals and to represent the data to the user comprehensibly. It is therefore clear that the suitability of classical test equipment is very limited for such measurements because the required intelligence is missing, as will be outlined in the next article.

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Glossary of terms overleaf. ►

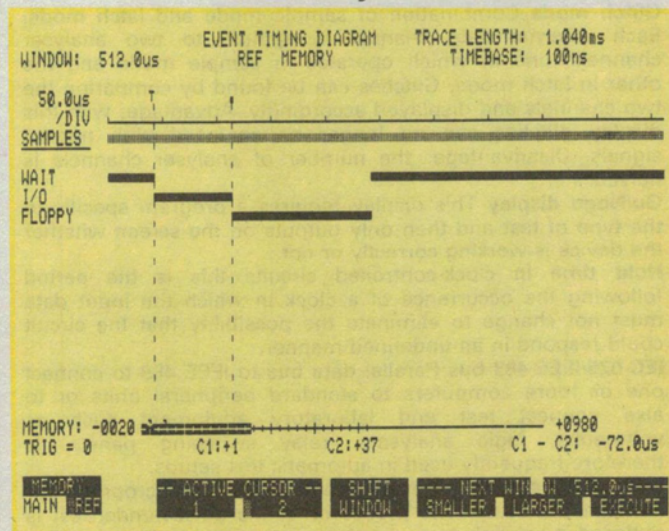


Fig.8: Performance analysis of a computer system using an event timing diagram.

Logic Analysis—Glossary

Bus Groups of signals in processor systems which are used to transfer information between the system components. A differentiation is made between unidirectional buses, such as the address bus, on which the CPU sends an address to the peripheral units, and bidirectional or multidirectional buses, such as the data bus, on which data can flow from the CPU to the peripheral units or vice versa. The usual bus widths in microcomputer systems are generally 8 bit and 16 bit.

Clock Clock signal with which the logic analyser accepts data from the device-under-test. The clock may come from the logic analyser itself (internal clock) or may be tapped from the device-under-test using a clock probe (external clock).

Clock-controlled A digital circuit is clock-controlled if it only changes its signal level depending on a clock. The rising or falling edge of the clock signal may generate the change in the circuit. Simplest example: D flip-flop or JK flip-flop.

Clock signal See clock-controlled.

Compatibility error Fault in digital circuit which is indicated by violation of the physical definitions of the level and timing of digital signals.

Data reduction The principle upon which logic analysis is based. The data applied to the logic analyser are only partially accepted by the analyser (1st reduction step); during evaluation (2nd reduction step) these data are reduced to the fundamental statement "Device operating correctly" or "Device not operating correctly".

Don't care During specification of the data pattern for triggering or qualification, the Don't cares (symbolised by an "X") represent channels which do not affect data qualification, i.e., are not taken into account.

ECL Emitter Coupled Logic, a family of digital circuits for very high speeds (> 100MHz). Disadvantage: high current consumption.

Ethernet Widely used local area network (LAN). Operates with only one coaxial cable, serial transmission with 10Mbit/s and CSMA/CD protocol. Because of its high speed it can be used to generate small computer networks. Since the coaxial cable can be tapped at any position by a transceiver, this network is particularly suitable for widely spaced systems where the installation costs are to be kept as low as possible.

Event timing display Special type of display in the LAS from Rohde & Schwarz. The user can define start and stop criteria for events which are then displayed as bars with a linear time axis.

Glitch Brief change in signal on a line. Malfunctions may occur if this line is a clock signal for a flip-flop or memory. Glitches cannot usually be detected using normal logic analyser sampling because they are of very short duration (in the nanosecond range). In such cases latch mode and glitch mode are used.

Glitch mode Combination of sample mode and latch mode. Each external data channel is applied to two analyser channels, one of which operates in sample mode and the other in latch mode. Glitches can be found by comparing the two channels and displayed accordingly. Advantage: with this display glitches can no longer be confused with normal signals. Disadvantage: the number of analyser channels is halved.

Go/Nogo display This display requires a program specific to the type of test and then only outputs on the screen whether the device is working correctly or not.

Hold time In clock-controlled circuits this is the period following the occurrence of a clock in which the input data must not change to eliminate the possibility that the circuit could respond in an undefined manner.

IEC-625/IEEE-488 bus Parallel data bus to IEEE 488 to connect one or more computers to standard peripheral units or to also connect test and laboratory equipment such as voltmeters, logic analysers, relay switching panels. Is therefore frequently used in automatic test setups.

In-circuit emulator Development aid for microprocessor software/hardware. The processor of the device-under-test is replaced by a link to a development system which enables the user to develop programs, load them into the device-under-test, execute them step-by-step and to observe

the registers of the CPU simulated by this arrangement.

Latch mode Analyser mode to determine glitches between the sampling points. All changes in level are extended by a special circuit such that they can be detected by the next clock.

Level-discrete The logic analyser recording is level-discrete because all analog voltages of the examined signals can be assigned to one of the logic levels LOW and HIGH, where the exact magnitude of the applied voltage is no longer considered.

Level error Level errors are present if the limits for HIGH and LOW levels can no longer be obtained for the logic family used and the response of the components connected to these lines becomes unpredictable.

Long-time evaluation Any type of evaluation which represents the results of several measurements or an extended period of measurements in reduced form. Statistical evaluations are typical examples.

Master/slave mode Common operation of two or more analysers where one is responsible for trigger detection (master) and the other(s) for the actual recording. Useful, for example, to combine the trigger intelligence of a state analyser with the speed of a timing analyser.

Multiple clock Modern analysers are able to use several external clocks simultaneously for recording. This multiple clock is primarily used in the analysis of multiplexed bus systems.

Multiplex bus Bus upon which qualitatively different information, such as addresses and data, can be transferred in sequence. The information is transferred on the bus with different clocks so that the peripheral units connected can differentiate between the different types.

Multi-tasking system Computer system on which several processes can be executed simultaneously. The CPU jumps between the processes time-controlled. Generic term for multi-user systems.

Multi-user system Computer system on which several users can work simultaneously. Since the CPU of such a system can only execute one process at a time, switching is made between the individual users and the executed programs time-controlled. Only intelligent logic analysers can follow individual programs specifically by simply eliminating all unrequired processes.

Parallel monitoring Characteristic of modern analysers in trigger or qualifier sequence. Several conditions can be monitored simultaneously and lead to completely different analyser responses.

Posttrigger Triggering where the posttrigger counter is set (to the depth of the analyser memory) such that all data in the analyser memory occur after the trigger.

Prettrigger Triggering where the posttrigger counter is set (to zero) such that all data in the analyser memory occur before the trigger.

Probe Circuitry detached from the logic analyser for the adaptation of device-under-test. Universal probes for general uses, uP probes and interface probes for processors and interfaces.

Qualification Method to reduce the data applied to the analyser memory: only data corresponding to patterns set by the user are read in; all other data are ignored.

Ranges Numeric ranges which can be specified in intelligent analysers in the data pattern definition. The data pattern is recognised if any value within this range occurs.

Restart Additional criterion which can be defined with sequential triggering to generate renewed execution of the trigger sequence. Triggering only takes place when the sequence can be executed without being interrupted by the restart condition.

Retroactive qualification Qualification where the data pattern responsible for qualification appears after the data word to be recorded. Only possible with analysers with special hardware (intermediate memory for data words until occurrence of qualification criterion).

RS232 Popular serial interface for connection of printers, modems, terminals, etc., to a computer system.

Sample mode Normal operating mode of an analyser: only the input levels present at the time the clock occurs are

transferred to the analyser.

Sampling frequency Important variable for examining signal delay times using a timing analyser. The sampling frequency must be many times larger than the limit frequency of the signals to be analysed to ensure sufficient accuracy.

Selector Freely programmable qualification facility in the Logic Analysis System LAS from Rohde & Schwarz.

Sequencer Freely programmable trigger facility in the Logic Analysis System LAS from Rohde & Schwarz.

Sequential qualification Qualification method with which the qualification criterion can be changed during the measurement depending on the occurrence of preset data patterns.

Sequential triggering Triggering method where several data patterns must occur in an exactly defined sequence before triggering takes place.

Setup time In clock-controlled circuits this is the period prior to the occurrence of a clock in which the input data must not change to eliminate the possibility that the circuit could respond in an undefined manner.

Skew Offset between the logic analyser channels. Different delay times in the analyser channels mean that simultaneous events can no longer be displayed as simultaneous.

Start/stop measurement Means of reducing the quantity of data reaching the analyser memory. Data input is interrupted when a stop criterion occurs and started again by the start criterion.

State analyser Logic analyser for the use of measurements in clock-controlled systems such as computer circuits where the logic data and not the signal times are important. Features: low limiting frequency, high trigger intelligence, many channels.

State display Display of data stored by the analyser in the form of a list where the data for each point in time are displayed numerically (binary, decimal, octal, hexadecimal or ASCII).

State error Faults in a digital circuit where signals are logically incorrect but cannot be physically differentiated

(level, timing) from correct signals. The logic analyser must have an interpretative function in order to trace such errors, i.e., it must be able to differentiate between "faulty" and "correct" signals.

Stuck-at error Short-circuit on a signal line with the effect that this line can no longer change. Can be found most rapidly using the logic analyser timing display.

Time analyser Logic analyser optimised for the use of measurements in systems where the signal times are important. Features: high limiting frequency, low trigger intelligence, few channels.

Time-discrete The logic analyser recording is time-discrete because the voltage levels of the signals can only be observed at particular times. No information is available on the response of the signal lines between these clocks (unless latch mode is used).

Time display Display of data stored by analyser in the form of a multi-channel oscillogram.

Timing error Timing errors occur with signals which must have a defined relationship in time to other signals. Violations in the setup and hold times are the most common errors.

Timing measurement Capability is implied when using internal clocks, provided all data are recorded, because the intervals between data are then multiples of the internal sampling period. In all other cases the analyser must have a hardware time measurement facility in which the time can be stored for each data word.

Triggering Release of the final phase of a logic analyser measurement. The posttrigger counter (adjustable by user) is started and terminates the measurement when the counter has run down. The detection of a data pattern by the analyser is a trigger criterion.

x/y display Type of display with which each possible combination of the displayed channels is assigned a point on the screen which is marked should this combination occur.

y/t display Type of display with which the data are entered on a time axis as quasi-analog variables.