The Modern Electronics Computer Experimenter Lab

(Part 3)

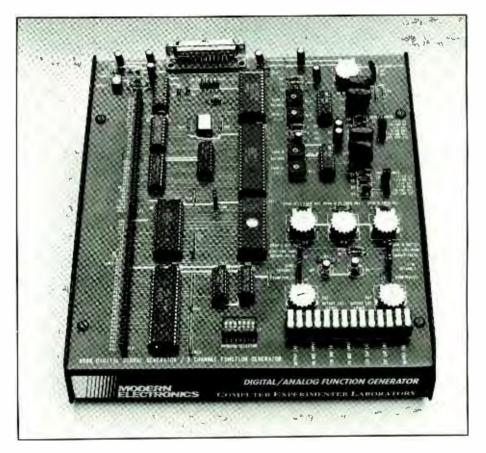
Adding a combination Digital Signal Generator and 8088-microprocessor Computer Experimenter Platform to the Dual-Channel Function Generator

By Martin Meyer

ast month, we gave details for building and using an analog Dual-Channel Function Generator that had room on its pc board for adding a digital signal generator, which is the subject of this installment. This add-on is a continuation of a series begun in the January issue with a build-it-yourself lowcost Digital Storage Oscilloscope and optional eight-channel Logic Analyzer module.

This month's Digital Signal Generator add-on generates up to 23 simultaneous digital signal trains that will be used as signal inputs for upcoming digital experiments. A main feature of this project is that you will be able to start learning about programming the 8088-series microprocessor. A limited understanding of programming, though not necessary for these projects, will allow you to integrate digital parts that require software interfacing into your projects.

An 8088 microprocessor in the Digital Signal Generator comes supplies all the necessary bus signals, permitting the instrument to also be used as a platform to build, test and learn about peripherals and programming of the most popular series of microprocessors ever introduced. In future articles, we will present



projects using the 8088 microprocessor in this project as the base processor. Figure 1 gives an overview on how the various experimenter Labs could be configured.

Next month, we will describe a Prototyping station that connects the equipment together and begin our discussion on theory, applications and experiments of interesting analog, digital and computer circuits.

System Overview

The Digital Signal Generator serves as the stimulus that allows you to examine experiments that involve digital circuits. You wire the circuits to be explored on a solderless breadboard or a Wire Wrap prototyping board, depending on personal preference and complexity and use the Oscilloscope or Logic Analyzer to observe both inputs and outputs.

The advantage of using a Logic Analyzer when working on digital circuits is that you can observe both inputs and outputs simultaneously. If you were to study the operation of a 74LS165 shift register, for example, you would find that you need eight data signals, a signal to load the data into the register and a clock to shift the data out of the registers. The Digital Signal Generator described here produces the needed signals, while the Oscilloscope lets you observe inputs and outputs.

Computer circuits like analog-todigital (A/D) and digital-to-analog (D/A) converters, input and output ports, memory, ROMs, interrupt systems, displays and digital signal processors (DSPs) can be studied using the 8088 test platform included in this project. For example, A/D and D/A converters, wired on the Wire Wrap prototyping board, can be connected to the I/O ports. An analog signal, supplied by the Function Generator, connects to the ANALOG input.

The processor program can invert, filter and limit the range or simply turn the data around and out to the D/A circuit. You monitor circuit responses and actions using the analog and logic analyzer features included in the Digital Storage Scope.

Analog circuits like operational and power amplifiers, comparators, filters, sensors and power-control circuits can be wired on the prototyping station and evaluated using the Function Generator and the Digital Storage Scope. You can use the prototyping station to build hundreds of useful circuits that illustrate basic ac and dc circuit principles, magnetic and transformer principles, power supply operation, and to demon-

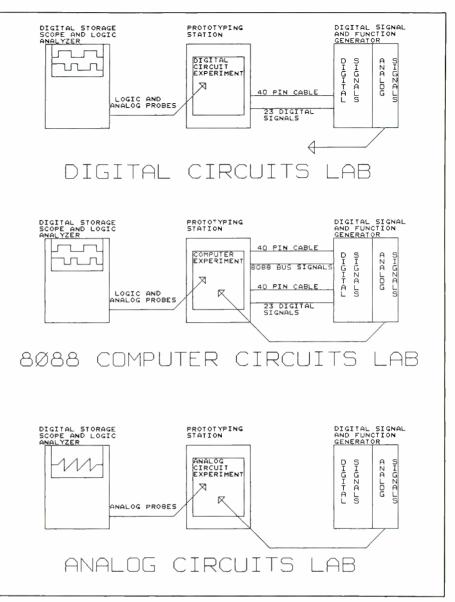


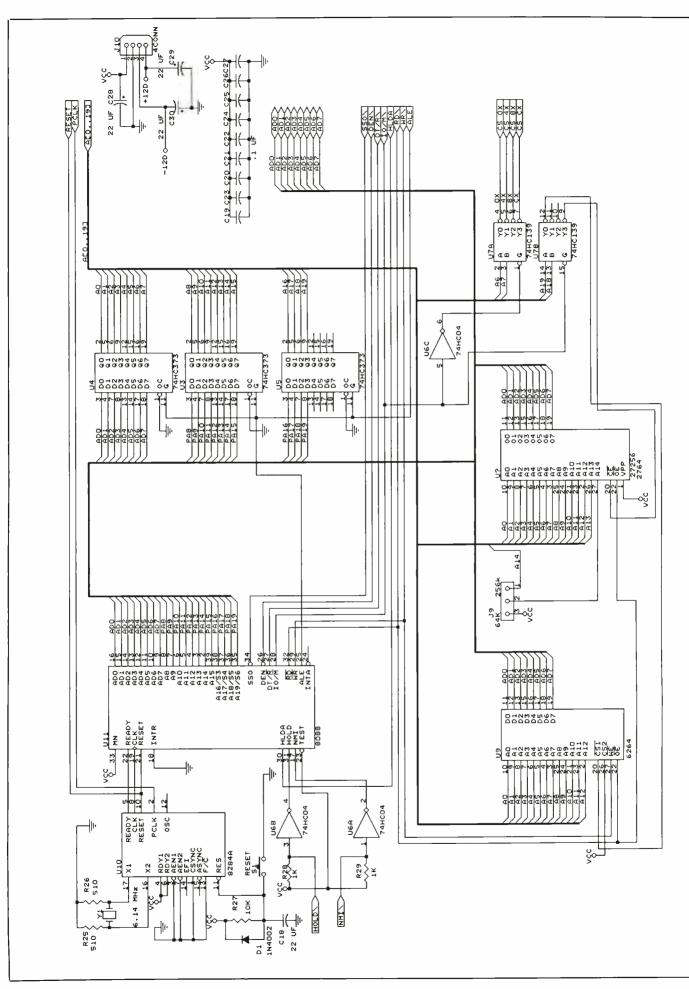
Fig. 1. Overview of how various Experimenter Labs can be configured.

strate how games, voice, video and ultrasonic circuits work, to name just a few of the may things you can do with this system.

The Digital Signal Generator/8088 Computer Experimenter Platform is built on the same circuit-board assembly you used to build last month's Dual Function Generator. This keeps the cost to less than \$140 for the combination Dual Function Generator/Digital Signal Generator/ 8088 Computer Experimenter Platform system.

Circuit Description

To generate the digital signal trains in the Digital Signal Generator add-on, an 8088 microprocessor, 8K of RAM, 8K of ROM, an 8155 I/O port/timer and the required support circuits are used. The circuitry for all this is shown schematically in Fig. 2(A) and Fig. 2(B). With this arrangement, digital signal trains are generated by toggling the *U13* output port signals. The timer can be programmed to produce a variety of



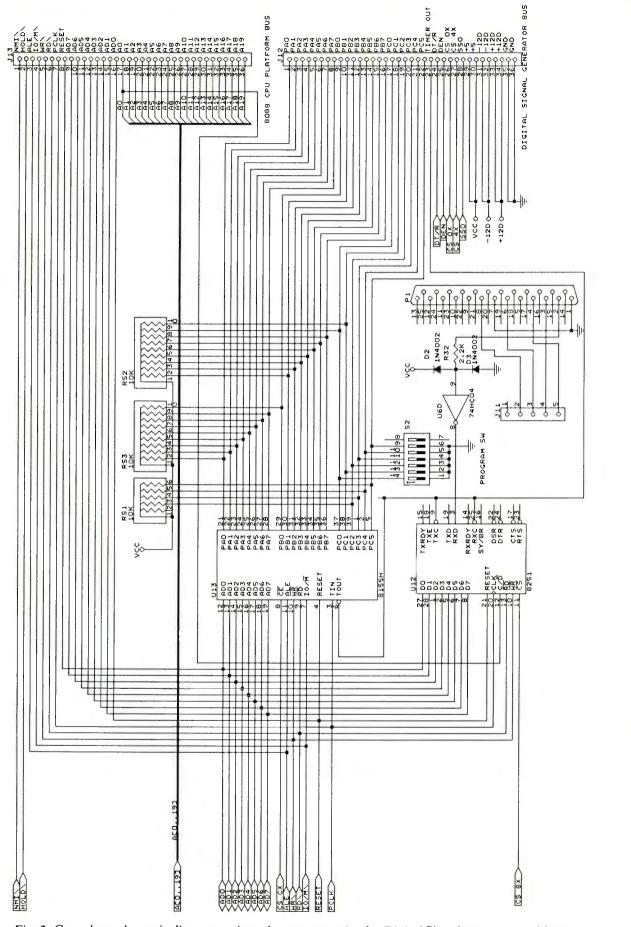


Fig. 2. Complete schematic diagram, minus dc power supply, for Digital Signal Generator add-on.

PARTS LIST

Semiconductors	nents (mount on last month's Dual-
U3,U4,U5—74HC373	Channel Function Generator pc
U6—74HC04	board), \$69.95 + P&H
U7—74HC139	Optional $+5$ - and ± 12 -volt power
U8—27C64	supply kit (one required for both
U9—6264	Generators), \$34.95 + \$4 P&H
U10—8284A	Optional black steel cabinet (for
U11—80C88	combination Function/Digital Sig-
U1282C51	nal Generator), \$37.50 + \$4.50 P&H.
U13—81C55H	Also Available from Netronics R&D
D1,D2,D3—IN4002 diode	Ltd.:
Y1—6.144 crystal	For Digital Storage Oscilloscope
Capacitors	(January 1991):
C19 thru C26—0.1-µF monolithic	Complete set of electronic compo-
C18,C28,C29,C30-22-µF, 16-volt ra-	nents, including pc board but not
dial	cabinet, power supply or probes,
Resistors (¼-watt, 5% tolerance)	\$199.95 + \$6.50 P&H
R25,R26—510 ohms	Optional eight-channel Logic Ana-
R27—10,000 ohms	lyzer, \$59.95 + \$3 P&H
R28,R29—1,000 ohms	Optional $+5$ - and ± 12 -volt power
RS1—Five-resistor 10,000-ohm resis-	supply kit, \$34.95 + \$4 P&H
tor SIP	Optional IC socket kit (contains 33
RS2,RS3—Nine-resistor 10,000-ohm	sockets), \$9.50 + \$1 P&H
SIP	Optional 100-MHz scope probe with
Miscellaneous	10:1 attenuator, \$27.50 + \$3.50
S1—Spst normally-open momentary-	P&H.
action switch	For Dual-Channel Function Genera-
S2—Seven-position DIP switch	tor (February 1991):
J9—Three-position single in-line header	Complete set of electronic compo-
J10—Power connector	nents, including pc board but not
J11—five-position single in-line header	power supply or cabinet, \$69.95 + \$4
J12,J13—40-pin socket strip	P&H
P1—DP-25 connector	Optional ± 5 - and ± 12 -volt power supply kit (one required for both
Printed-circuit board; suitable cab-	Generators), $$34.95 + $4 P&H$
inet (see Note below); etc. Note: The following items are available	Optional black steel cabinet (one re-
from Netronics R&D Ltd., 333 Litch-	quired for combination Function/
field Rd., New Milford, CT 06776	Digital Signal Generator), \$37.50
(tel. 203-355-2659)*:	+ \$4.50 P&H.
For Digital Signal Generator:	*MasterCard and VISA accepted on
Complete set of electronic compo-	all orders.
Complete set of electronic compo-	an oracis.

pulses and square-wave trains.

Programs to produce the signal trains can be written on and downloaded from an IBM PC or compatible computer, or they can be run from fixed programs stored in ROM. The programming mode is selected via DIP switch S2. Simple user programs can be written using the Debug program supplied with DOS. No programming experience is needed for writing these simple programs.

onal +5- and ± 12 -volt power y kit (one required for both (ators), \$34.95 + \$4 P&H;nal black steel cabinet (one red for combination Function/ al Signal Generator), \$37.50 .50 P&H. terCard and VISA accepted on ders. • The Microprocessor. The 8088 CPU (U11) is a member of a family of devices that have become the world's most popular series of microprocessors. If you are going to study any microprocessor, this Lab series is an excellent place to start. Basic system architecture and the instruction set is compatible with all newer processors, except for memory width, address size and added instructions. The 8088 microprocessor used in this project is set to operate in minimum mode. That is, special control and status signals that are necessary for large systems are not used here. The 8088 CPU is a relatively straightforward hardware device. Address/ Data bus lines A0 through A7 are multiplexed so that they share this function with the eight-bit data bus without creating conflicts or collisions. Address pins PA16 through PA19 are also multiplexed with various status signals.

In both cases, the address information is presented on the output pins of the 8088 during the first part of each machine cycle and is latched into U4 through U6 when the CPU issues an ALE (Address Latch Enable) signal. During the remainder of the machine cycle time, the low-order address pins become the eight-bit bidirectional data bus, and address lines PA16 through PA19 become CPU status pins.

All 19 address bits are latched and are connected to the 8088 Platform bus. The bus includes all address, data and CPU control signals that are used as part of the 8088 Computer Experimenter Platform.

• Clock Generator. The 8088 requires the use of 8284A clock generator U10. This circuit supplies the 8088 with a special clock signal that has a 33% duty cycle and is half the crystal frequency. When power is turned on or the system is reset, the 8284 generates a master reset signal that is used to reset all peripherals and the CPU. A symmetrical system clock, labeled PCLK, is generated for the 8088 system bus. The 8284 also has provisions, via the RDY and AEN signals, that support multi-processor operation. These pins are not used in this application.

• Address Decoders. The 8088 can address 1M of memory. The ROM is positioned at the very top of memory, starting at F8000 if a 32K ROM is used or FE000 if an 8K ROM is used. System RAM is positioned at 00000 to permit use of interrupts if needed for Platform applications. Lines A18 and A19 are decoded by U7B. If A18 and A19 are high, the ROM is selected; otherwise RAM is addressed.

Chip U7B decodes the I/O addresses. Provisions have been made for four I/O devices by decoding addresses A6 and A7 when the IO/M pin 28 of U11 is low. I/O decoder U7B generates chip-select lines at locations 0X, 4X, 8X and CX. The Digital Signal Generator uses Port CX for the U13 and Port 8X for UART U12.

• The 8155 I/O Port. In this project, U13 plays a key role. The 8155 device consists of two eight-bit and one sixbit I/O ports that can be configured to be either inputs or outputs. The six-bit port can be programmed to be status pins, the eight-bit ports operate in a handshaking mode.

Also included is a 14-bit timer/ counter that provides either a square wave or terminal count pulse outputs. The six-bit port is used as an input port to read the program selector. If the download mode is selected, the six-bit port is available to produce digital signals or to act as an I/O port. The program toggles the ports to produce the digital signal trains.

The programs simply initialize the 8155 to configure the ports and timer operation. Outputs are then set to the value desired at the beginning of the digital signal train. The system loops until the next change is required, at which time, the ports are changed. This process is duplicated, changing the loop time and the output data to produce the desired signal train.

The counter/timer can also be used to produce digital signals. In squarewave mode, the timer can be turned on and off to produce a predetermined set of pulses. The program then jumps to the beginning or waits for a system reset to begin again.

• *Program ROM*. The program ROM is mapped at FE000. Unlike other processors, the 8088 series

looks for the first instruction at location FFFFO, which is 16 bytes from the top of the 1M address space. The program starts with a jump to the base address of ROM. After running some housekeeping routines, the program checks program selector switch S2 to determine if you want to use a built-in program or download a custom program from an IBM com-

An Example of a Digital Experiment Using the 74LS165

When clocked, the 74LS165 eight-bit serial shift register shifts data toward the serial output pin (QH $\$). Parallel data is entered directly into registers that are enabled by a low level at the SH/LD \ (shift/load) input. (Note: reverse slash symbol \setminus indicates that the load input is active low.) The 74LS165 also features a clock inhibit and a complemented (inverted) serial output. Clocking or shifting data that has been entered into the registers is accomplished via a low-to-high transition of the clock input while SH/LD \setminus is high. Parallel loading is inhibited when the SH/LD \setminus pin is held high. The logic level at the serial input is present at the output after the first eight shifts, provided no additional parallel data has been loaded.

Applications

The 74LS165 is used to convert an eightbit parallel data format into a serial format, which is desirable when sending data over a two-conductor link or when shifting parallel data into serial inputs. This device was used in the Digital Storage Oscilloscope to transfer the data from the eight-bit parallel display memory to the serial display registers inside the LCD. These registers require the data be in serial format.

The 8251A USART used in this project has this type of register embedded in a relatively complex device to transmit eight-bit parallel data to the serial RS-232 output pins. Other shift registers convert serial data to the parallel format, which is required at the receiving end of serial data if data is to be entered into an eight-bit parallel port.

Lab Experiments

The object of this experiment is to generate eight-bit parallel data, a shift clock, clock inhibit and shift/load logic signals to stimulate the 74LS165 and then view the inputs and outputs on an oscilloscope or logic analyzer.

Signals necessary for this experiment are stored in the Digital Signal Generator (Digital Experiments) ROM. Let us look at how simple it is to generate the signals if the program that generates the signals is downloaded from an IBM PC or compatible computer.

The first signal to be generated is a shift clock. The 8155 timer/counter is ideally suited for this task. There is no need to get into the actual programming steps at this time. What follows is a flow chart that indicates the simplicity of the process. Refer to Fig. A as you go along.

(1) Initialize the 8155 ports as outputs
(2) Initialize the timer to produce a square wave

(3) Load the timer divider to divide the 3-MHz timer input to produce a 10kHz square wave

(4) Output AA hex to Port A to make it the parallel data input to the 74LS165

(5) Output C0 hex to Port B to set clock inhibit and $SH/LD \setminus high$

(6) Output 80 hex to Port B to set SH/LD \setminus low

(7) Output 50 hex to Port B to set clock inhibit low and SH/LD $\$ high

(8) Turn on timer for 9 counts

(9) Turn off timer off

(10) Jump to step 4

Connect the signals to the 74LS165 as detailed in Fig. A and start the program. Verify the results shown in the timing diagram with either your scope or logic analyzer.

The program includes some additional code to determine the delay between operations. Other than this, you can see that programming is not complicated and could even be fun to do on your own.

Try changing the data at step 4 and note the results. Check that $QH \setminus is$ the inverted or complemented QH.

patible. If you select a custom program, the program jumps to the one selected and begins generating digital signals as required. It then loops until you press the RESET button. • *RAM*. RAM is principally used to store the programs you download from a PC or compatible computer. After the UART receives the custom program, the system ROM transfers

control to the RAM-based program.

Used in the system is 8251A programmable communication interface *U12*. This device permits downloading of custom programs into the

DATA LINE O FROM 8155 PAO OUTPU	= AA HEX 10101010 BINARY HIG	4
DATA LINE 1 FROM B155 PA1 OUTPU	= AA HEX 10101010 BINARY	
DATA LINE 2 FROM 8155 PA2 OUTPUT	HIG	4
DATA LINE 3 FROM B155 PA3 OUTPUT	- AA HEX 10101010 BINARY	
	LOW HIG	
DATA LINE 4 FROM B155 PA4 OUTPUT	= AA HEX 10101010 BINARY	
DATA LINE 5 FROM 8155 PA5 OUTPUT	= AA HEX 10101010 BINARY	
DATA LINE 6 FROM 8155 PAG OUTPUT	HIGH = AA HEX 10101010 BINARY	4
DATA LINE 7 FROM 8155 PA7 OUTPUT	LOW	
		MER QUT
		CLOCK INHIBIT SIGNAL 8155 PBO
CSH/LD/3 PINWHEN LOW	DATA IS LOADED INTO THE REGISTORS	8155 PB1
TAKES VALUE OF BIT 7 WHEN BIT 7 BIT 6 BIT SL/LD GOES LOW OUTPUT LEVELS		TAKES THE VALUE OF BIT 7 WHEN SH/LDN GOES LO
	PIN 8 GND	
	PIN 16 +5	165 FUNCTION TABLE
	10 U1 11 SER	SH/LDN CLK CLK INH FUNCTION
CONNECTIONS TO DIGITAL PA3	10 SER 12 A 13 B 13 B 14 14 5 5 6 4 5 6 4 5 6 4 5 6 4 5 6 4 5 6 7 7 8 8 8 8 8 8 8 8 8 8 8 8 8	L X X PARALLEL LOAD
SIGNAL GENERATOR PA4		H H X NO CHANGE
PA6 PA7	G QH 9 NORMAL OUTPUT	H X H NO CHANGE
TOUT PB0 PB1	2 CLK QH 7 INVERTED OUTPUT	H L Î SHIFT H Î L SHIFT

Digital Signal Generator/8088 Computer Experimenter Platform. The ROM program initializes the 8251, setting it up to wait for data from the computer. The data format selected is 9,600 baud, eight data bits and one stop bit. The receiver clock signal is generated in the 8155 counter/timer, which is cleared and reset for user applications after downloading.

Downloading of custom programs is another good example of the need to develop basic programming skills. It requires that all operating parameters be set via software initialization. The only way data is removed and tested is via a polled or interrupt program. The system waits for the data stream to begin and then jumps to the downloaded program when the transmission has been completed.

Various jumpers must be connected to meet the requirements of a standard IBM COM format (pins 4, 5, 6 and 20 of *P1* must be connected together). This is easily accomplished by strapping J1. Data output signals from the computer swing between + 12 and - 12 volts. Resistor R32, diodes D2 and D3 and IC U6D condition the input signal so that it is TTLcompatible, which is a requirement of the 8251A.

• Generator Bus. The Digital Signal Generator bus consists of a 40-pin header that accepts 25-mil (0.025inch) diameter wires. These wires connect directly to your prototyping station, as shown in Fig. 2(B).

Next month, we will describe a prototyping station in which two ribbon connectors connect all signals available in the Digital Signal Generator directly to a prototyping station that utilizes popular plug-in breadboards and a Wire Wrap system.

The Digital Signal Generator bus consists of the 22 I/O lines plus the timer and clock signals from the 8155. The power supply is also available to the prototyping station to be used with experiments that draw less than 100 milliamperes of current. You can add a separate power supply to the prototyping station when building projects that draw more than 100 milliamperes.

• Computer Platform Bus. When you conduct experimental computer projects, you want all 8088 CPU signals, plus the 8155 I/O signals, at the prototyping station. The second 40pin connector ties the address, data, control and chip-select signals to your prototyping station. This permits you to perform experiments using the 8088 microprocessor and its RAM, ROM and 8155 I/O as the host. All you must add is the experiment components and the program.

• Power Supply. This project requires a power supply capable of delivering +5 volts at 1 ampere and ± 12 volts at 100 milliamperes.