Common-gate, common-base circuits shift voltage levels

by Peter J. Bunge
Atomic Energy of Canada Ltd., Chalk River, Ontario

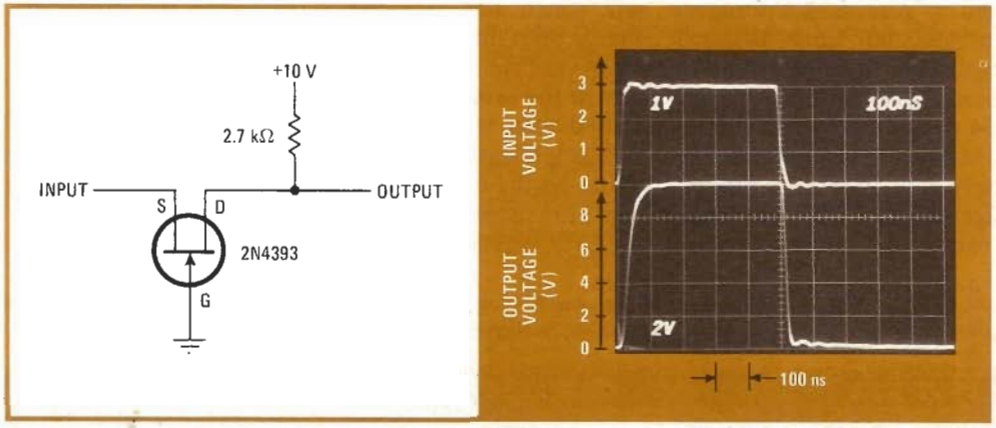
The voltage-shifting interface needed between incompatible logic systems can be quite straightforward—just a field-effect transistor in a common-gate circuit or a bipolar transistor in a common-base circuit. Both circuits are fast, uncomplicated, and economical in both parts cost and power drain.

The common-gate FET circuit shown in Fig. 1 can couple the active outputs from any logic family to a voltage level higher than the V_{CC} of the logic—an impossibility with pullup resistor interfacing or complementary-metal-oxide-semiconductor buffer (4009, 4010) interfacing. It uses much less power than open-collector transistor-transistor-logic interfacing, especially when only one signal is involved, and it is much faster than some commercial level shifters (e.g. 100 nanoseconds versus 900 ns for the Solitron CM410AE). For the 2N4393 FET shown, the input range is 3 to 40 volts while the output range is 0 to 40 V (determined by the pinch-off and breakdown voltages of the device.)

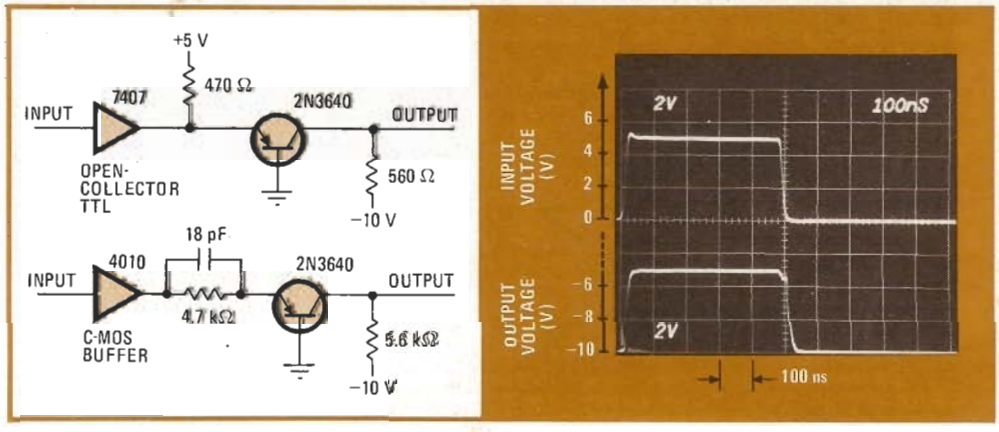
The common-gate circuit provides only positive output voltages. A typical application is in interfacing an n-MOS random-access memory, which has 0-V and 3-V output levels, to C-MOS circuitry. Interfacing is necessary in this case because the 3-V level is just at the operating threshold of C-MOS when it is operating from a 5-V supply.

Common-base transistor circuits are used to interface positive voltage levels to negative-referenced logic. Figure 2 shows arrangements for translating 0-V or +5-V TTL or C-MOS levels to −10 V or −5 V. These methods are simple, require little power, and can be used with either active outputs or open-collector outputs, as shown. □

Designer's casebook is a regular feature in Electronics. We invite readers to submit original and unpublished circuit ideas and solutions to design problems. Explain briefly but thoroughly the circuit's operating principle and purpose. We'll pay $50 for each item published.



1. Level translator. A field-effect transistor in the common-gate configuration can provide output voltages that are higher than the supply voltage of the driving logic. Here the FET voltage-shifter accepts input levels of 0 or 3 V and delivers outputs of 0 or 10 V. The fast transitions and short delays that are demonstrated in the oscilloscope photo are achieved by minimizing the load capacitance.



2. Signal polarity inversion. Common-base level translator interfaces positive voltages to negative-referenced logic. Circuits here accept levels of 0 or 5 V and deliver outputs of −10 or −5 V. Waveforms shown are for circuit driven by open-collector TTL. Speed is sacrificed to conserve power in the circuit driven by a C-MOS buffer. The 18-pF speed-up capacitor charges input capacitance of transistor.