DESIGNING WITH DIGITAL IC'S

This month we'll see how simple gates can be combined to form one of the basic circuits of digital electronics—the flip-flop.

JOSEPH J. CARR

Part 5 IN PAST INSTALLMENTS of this series we have discussed logic families, interfacing methods, and elementary gates. Let's now expand our discussion to include combinations of gates. Such combinations of gates can, of course, perform more complex functions than simple gates alone. The first of such circuits that will be discussed are basic flip-flops, specifically two forms of set-reset flip-flops—the clocked set-reset flip-flop, and master-slave (which is also known as the load-transfer) flip-flop. But first, let's review the two basic gates that are used in these circuits—the NAND and NOR gates.

NAND and NOR gates

The two basic gates used in our flip-flops are the NAND and NOR gates shown in Fig. 1. We've previously looked at how those gates operate, but let's briefly review that here:

For a NAND gate, a low on either input forces the output high. Thus, for the output to be low, a high must be presented to both inputs.

For a NOR gate, a high on either input forces the output low. Thus, a low must be presented to both inputs for the output to be high.

Most IC NAND and NOR gates are "quad" units; that is, there are four such gates in a single IC package. The 7400 TTL device, for example, is a "quad two-input NAND gate," while the 7402 is a TTL "quad two-input NOR gate." Both IC's contain four two-input gates that are independent of each other, except for power supply and ground connections.

Set-reset (S-R) flip-flops

The set-reset flip-flop (also called the S-R flip-flop) is a bistable circuit, which means there are two stable output states. Those states are defined as follows: Set—Q = high, $\overline{Q}$ = low; reset—Q = low, $\overline{Q}$ = high

Unless otherwise specified, the set state always makes Q high, and the reset state makes Q low. Of course, $\overline{Q}$ is always the complement of Q.

Figure 2 shows the NAND gate version of the S-R flip-flop, while Table 1 is the truth table that describes circuit operation. The NAND-gate S-R flip-flop rules are summarized as follows:

A low applied to the set (S) input forces Q high, and $\overline{Q}$ low. A low applied to the reset (R) input forces Q low and $\overline{Q}$ high. A high applied to both R and S inputs simultaneously results in no change in the output state. Finally, a low applied to both inputs simultaneously is a disallowed state that confuses the circuit and produces an unpredictable output state.

Even a momentary low will force a change in the output state. Application of a constant low to either input will hold the commanded output state. That tactic is sometimes used to lock a particular state (set or reset) until some other circuit action is completed. The S-R flip-flop is bistable, so it will remain in either set or reset states until commanded to change by application of a low to the appropriate input.

Figure 3 shows several symbols used to denote S-R flip-flops in schematic diagrams. All three are used for NAND-logic S-R flip-flops, even though only Fig. 3-*a* and 3-*b* are technically correct (the inverted inputs of those figures comply with the active-low nature of the inputs). The symbol shown in Fig. 3-*c* is sometimes seen for NAND-logic S-R flip-flops, but is more properly associated with a NOR-logic S-R flip-flops. In **Radio-Electronics**, the symbol shown in Fig. 3-*a* is always used to denote a NAND-logic S-R flip-flop.

TABLE 1

Inputs		Outputs	
S	R	Q	$\overline{Q}$
0	0	Disallowed	
1	0	0	1
0	1	1	0
1	1	No change	

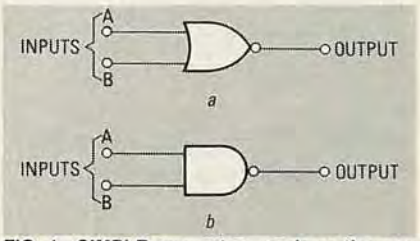

FIG. 1—SIMPLE NOR gates, such as the one shown in *a*, and NAND gates, such as the one shown in *b*, are the basic building blocks of flip-flops.

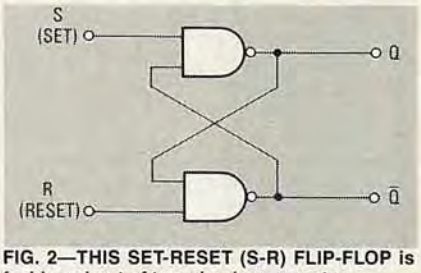

FIG. 2—THIS SET-RESET (S-R) FLIP-FLOP is fashioned out of two simple NAND gates.

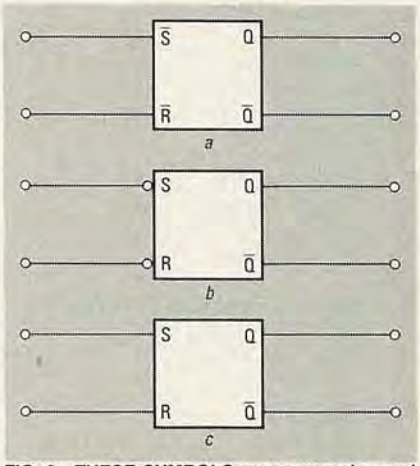

FIG. 3—THESE SYMBOLS are commonly used in schematic diagram to show S-R flip-flops. The symbol shown in *a* is used in this magazine.

An example of a NOR-logic S-R flip-flop is shown in Fig. 4, while the truth table is shown in Table 2. As you might expect, the NOR-logic S-R flip-flop operates in the opposite manner from the NAND-logic version of the circuit. That can be verified by examining the truth tables for the two circuits.

As in the previous case, only a momentary high need be applied to either input to make the NOR S-R flip-flop change output states.

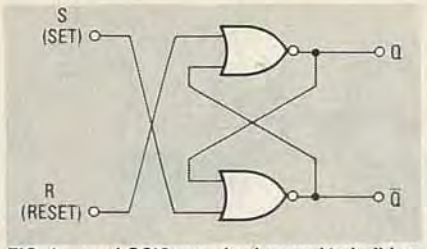

FIG. 4—NOR LOGIC can also be used to build an S-R flip-flop.

TABLE 2

Inputs		Outputs	
S	R	Q	Q̄
0	0	No change	
1	0	1	0
0	1	0	1
1	1	Disallowed	

The S-R flip-flop can be used in a wide variety of applications. One such application is a digital version of a latching switch. Figure 5 shows such a switch based on the NAND-logic S-R flip-flop. The inputs are controlled by pushbutton switches, S1 and S2. Each is a normally-open type that closes when pushed. Since each input is strapped high with a 3300-ohm pull-up resistor, the input will be high as long as its associated switch is open, but will go low when that switch is closed. Once again, due to the nature of the circuit, a momentary low is all that is required for the output to change states.

Note in Fig. 5 that the switches and the outputs are labeled START and STOP. That labeling implicitly assumes that the circuit is used in a machine or instrument that needs "start" and "stop" commands. Assuming an initial state of the STOP output high and the START output low, pressing the START button will cause the

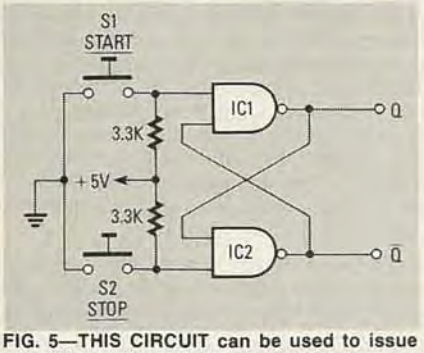

FIG. 5—THIS CIRCUIT can be used to issue "stop" and "start" instructions to a circuit or piece of machinery. Its operation is analogous to a latching switch.

outputs to change states; that is, the START output will go high and the STOP will go low. Those output states will remain "locked-in" even after the switch is released. They will reverse again only when the STOP button is pressed.

Ordinary S-R flip-flops sometimes suffer a problem that besets classical relay circuits: race conditions. In the classical version of the problem, relays that supposedly close simultaneously do not, with unpredictable results. Another problem is that noise impulses can create conditions that may cause the flip-flop to go into the opposite, incorrect state. There may also be a timing problem; that is, we may not want a circuit action to occur until a certain time. All of those problems are either solved or reduced by the use of the clocked S-R flip-flop shown in Fig. 6.

The clocked S-R flip-flop is made from a NAND-logic S-R flip-flop that is gated by a clock signal. Gates IC1 and IC2 are cross-coupled in the manner that is normal for NAND-logic S-R flip-flop circuits. The set (labeled A) and reset (B) inputs, however, are controlled by gates IC3 and IC4, respectively.

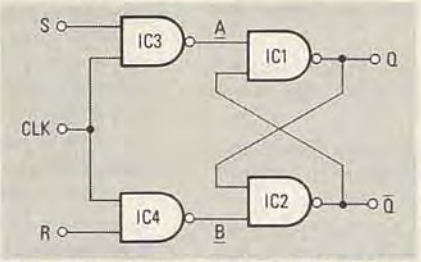

FIG. 6—IN A CLOCKED S-R FLIP-FLOP, the output will change states only when the clock input is held high.

Recall the operation of a NAND logic S-R flip-flop: if point A is momentarily grounded, the flip-flop is set (the Q output is high, the $\overline{Q}$ is low); if point B is grounded, the flip-flop is reset (Q is low, $\overline{Q}$ is high). Point A is controlled by gate IC3, while point B is controlled by gate IC4. But both IC3 and IC4 are controlled by the clock line. When the clock line is low, the outputs of IC3 and IC4 are locked high, and will not respond to changes on the other inputs (S and R). Those inputs are thus active only when clock is high. Note that the sense of the S and R is reversed from normal NAND-logic S-R flip-flops. Here, the those inputs are active-high rather than active-low.

The clocked S-R flip-flop solves some of the problems inherent in the regular S-R flip-flop circuit. In any event, the clocked version of the circuit permits synchronous operation (and changes are allowed to occur only at certain discrete times).

Another alternative for synchronous operation is the master-slave flip-flop (also call the load-transfer flip-flop) shown in Fig. 7. That circuit consists of a pair of clocked S-R flip-flops in cascade; i.e. the Q and $\overline{Q}$ outputs of one S-R flip-flop, IC1, drive the S and R inputs of the second flip-flop, IC2. The clock inputs of the two flip-flops are driven out of phase with each other (one is high when the

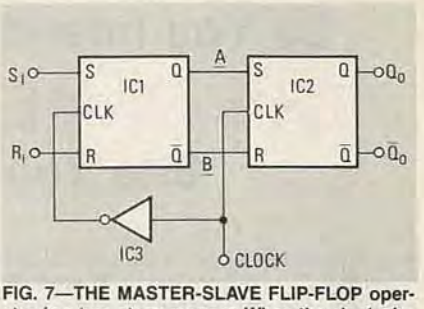

FIG. 7—THE MASTER-SLAVE FLIP-FLOP operates in a two-stage manner. When the clock signal is low, information presented to the inputs is latched into the first flip-flop. When the clock goes high, that information is passed to the second flip-flop, whose outputs change accordingly.

other is low). The CLK input of IC2 is driven directly by the master clock signal (also called load/transfer or L/T signal), while the CLK input of IC1 is driven by the inverted master clock signal.

Recall the operation of the normal clocked S-R flip-flop: The signals applied to either input will only cause an output change when the CLK input is high. Thus, when the master clock signal is low, IC2 is inactive (its CLK line is low) and IC1 is active (its CLK input is high). That situation permits loading of the master-slave flip-flop. State changes at either input of IC1 are reflected by the outputs of that gate.

When the master clock line goes high, the situation reverses—IC2 is active and IC1 becomes inactive. At that time, the outputs of IC1 are "read" by the inputs of IC2. Thus, those outputs will either set or reset the outputs of IC2.

Clocking

Flip-flops are designed to be triggered in one of two ways—either on a leading or trailing edge of a clock signal, or when the clock signal reaches a certain positive or negative level.

Where triggering takes place is important because it tells us where the action of the flip-flop will occur. On a level-triggered flip-flop, the output state changes will occur when the clock is either high or low (according to design), but not during the transition between levels. Thus, a positive-level-triggered flip-flop is active only when the clock input is high; the clocked S-R flip-flop discussed earlier was an example of that type of triggering. Similarly, the negative-level-triggered device becomes active when the clock line is low.

An edge-triggered device acts during either low-to-high (positive edge triggered) or high-to-low (negative edge triggered) transitions. Although edge-triggered devices are not common in the type of circuits discussed thus far, they are used extensively in more complex flip-flops. Those devices will be the subject of our next article. **R-E**