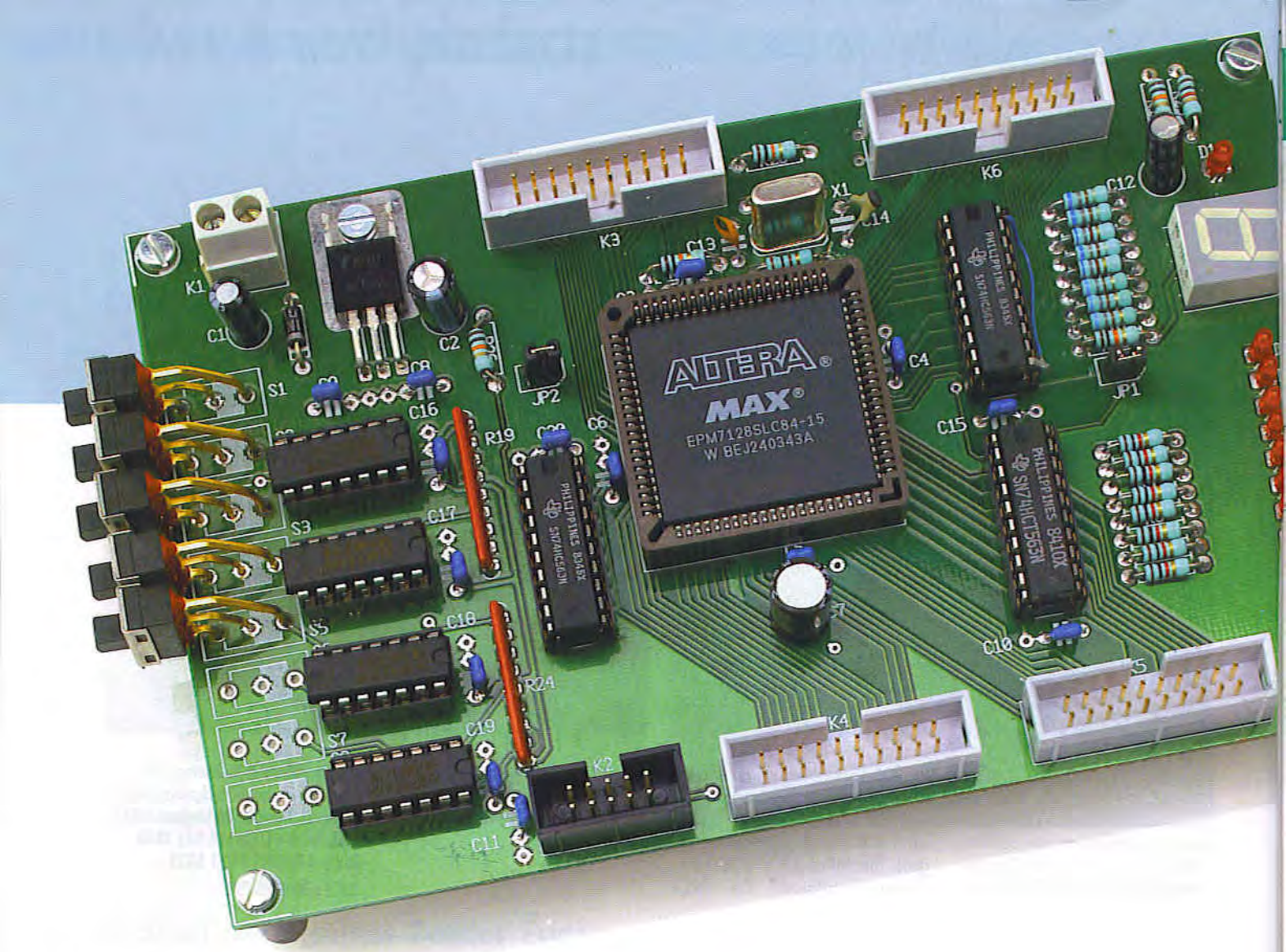

Paul Goossens

Design Your Own IC

Prototyping with CPLDs (part 1)

Designing a circuit always involves several somewhat disagreeable tasks, such as soldering, looking up the pinouts of ICs and laying out a maze of tracks on a printed circuit board. All of this is now no longer necessary, since you can program your own digital circuit in a CPLD.

Experimenter's board features

- CPLD version: EPM7128
- JTAG interface
- all I/O lines available via box headers
- supplementary I/O can be disabled using jumpers
- 7-segment display
- 8 LEDs
- 8 switches with debouncing circuitry
- on-board supply voltage regulator
- Eurocard format
- extensive development environment available free of charge from Altera

The CPLD experimenter's board presented here makes an excellent starting point for sitting down at the keyboard and directly designing your own circuit.

For most people, experimenting with digital logic brings to mind an image of an experimenter's board stuffed full of ICs interconnected by countless wires. Anyone who has ever worked in this manner knows that such an arrangement usually takes many hours to construct, not to mention the modifications that have to be made if the circuit does not work properly right off the bat.

A CPLD can be used to replace such a 'forest' of digital logic ICs. CPLD ICs contain a large number of digital building blocks that can be interconnected in a wide variety of manners simply by programming. Such an IC can actually be considered to be the modern version of an experimenter's board full of ICs.
Instead of soldering all sorts of little wires in place, designers and experimenters can now conveniently design circuits while seated in front of a PC, and then program their latest designs into the IC in a trice.
This clearly saves a lot of time, and it has the advantage that it isn't necessary to document modifications afterwards on paper or in some other manner. This is because the circuit is drawn (or described, as discussed later on) on the computer, after which the PC computes how the design must ultimately be realised in the IC.

CPLD organisation

Our experimenter's board is based on the Altera MAX7000 family of CPLDs. The organisation of these CPLDs is shown in **Figure 1.** At the top of the drawing you can see the four special

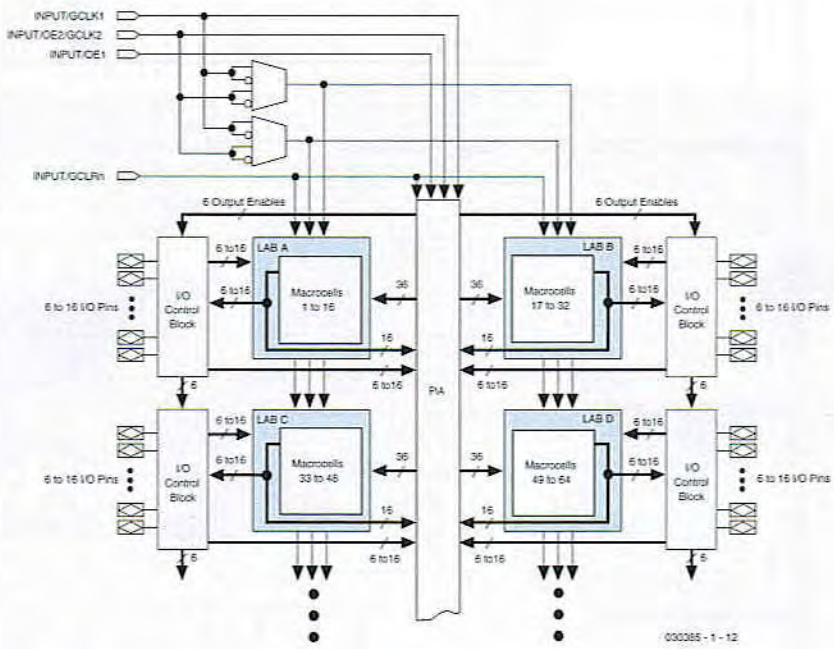

Figure 1. Overall organisation of MAX7000 CPLDs.

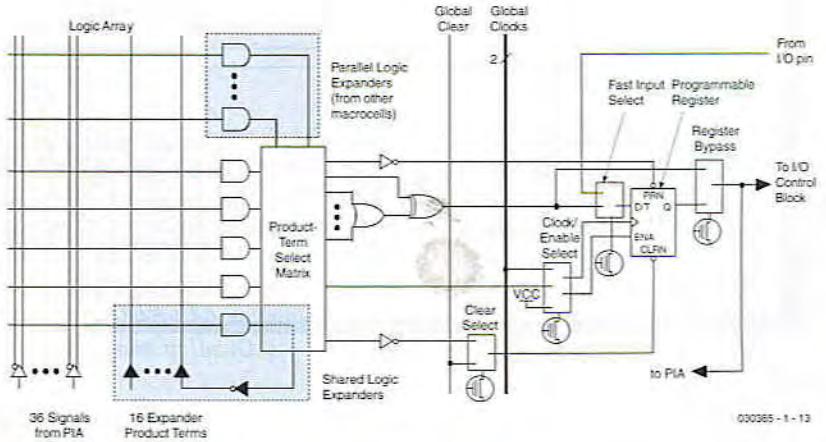

Figure 2. The structure of a MAX7000 macrocell.

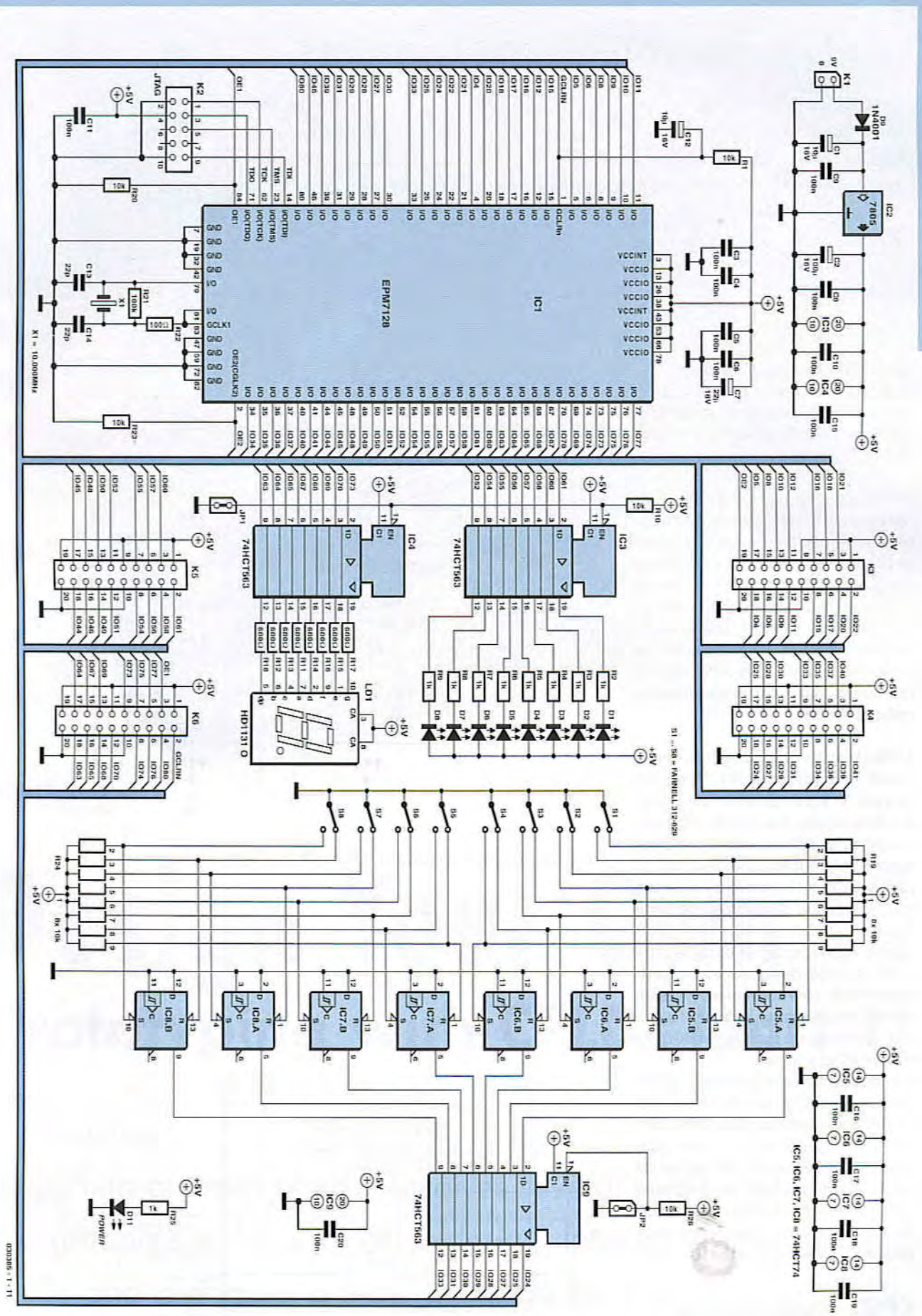

Figure 3. Besides the CPLD, the circuit of the experimenter's board includes several indicators (D1–D8 & LD1) and switches with hardware debouncing (S1–S8 & IC5–IC8).

COMPONENTS LIST

Resistors:
R1,R10,R20,R23,R26 = 10kΩ
R2-R9,R25 = 1kΩ
R11-R18 = 680Ω
R19,R24 = 10kΩ 8-way SIL array
R21 = 100kΩ
R22 = 100Ω

Capacitors:
C1,C12 = 10µF 16V radial
C2 = 100µF 16V radial
C3-C6,C8-C11,C15-C20 = 100nF
C7 = 22µF 16V radial
C13,C14 = 22pF

Semiconductors:
D1-D8,D10 = LED, red, low current
D9 = 1N4001
LD1 = 7-segment-display, common anode, e.g., HD1131 OJ
IC1 = EPM7128SLC84-10 or EPM7128SLC84-15
IC2 = 7805
IC3,IC4,IC9 = 74HCT563
IC5-IC8 = 74HCT74

Miscellaneous:
JP1,JP2 = 2-way header with jumper
K1 = 2-way PCB terminal block, lead pitch 5mm
K2 = 10-way boxheader
K3-K6 = 20-way boxheader
S1-S8 = slide switch, 1 changeover contacts, e.g., APEM A2
X1 = 4.000MHz quartz crystal
84-way PLCC socket
PCB, order code **030385-1**

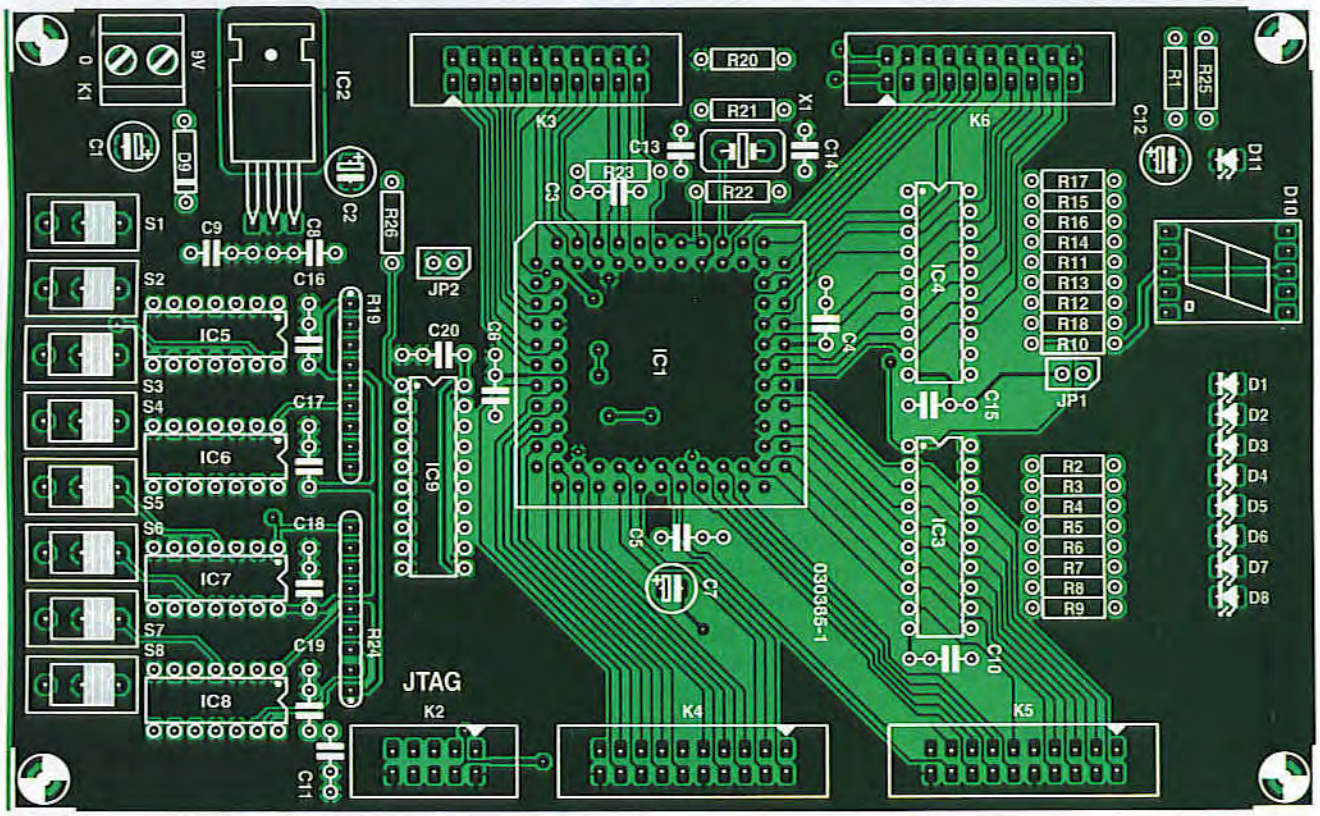

Figure 4. Component layout of the double-sided through-plated PCB for the experimenter's board. The associated copper track layouts can be retrieved from the Free Downloads section of our website (file no. 030385-1.zip).

inputs for the CPLD. These signals are connected to the macrocells in the IC in a manner that allows them to optimally perform their intended functions (CLK, OE, and CLEAR).
The inputs and outputs of the various macrocells are connected to each other as desired via the Programmable Interconnect Array (PIA). There are also inputs and outputs that are connected to the various I/O Control Blocks. Their job is to connect the internal signals to the I/O pins of the IC.

Four Logic Array Blocks (LABs) are also shown in Figure 1. These LABs contain the actual programmable logic. Each LAB consists of 16 macrocells. Various CPLD versions are available in the MAX7000 family. The type number of the IC indicates how many macrocells are present in the IC.

Macrocells

The actual programmable logic is located in the macrocells. The structure of a macrocell is shown in **Figure 2**. Each macrocell has its own Logic Array, which consists of 36 inputs connected using a programmable AND function. Four of these AND functions are combined into a single signal in the Product Term Select Matrix. The capabilities of the IC can be increased by further increasing the number of product terms. If you want to know more about this, we recommend reading the data sheet for these CPLDs.

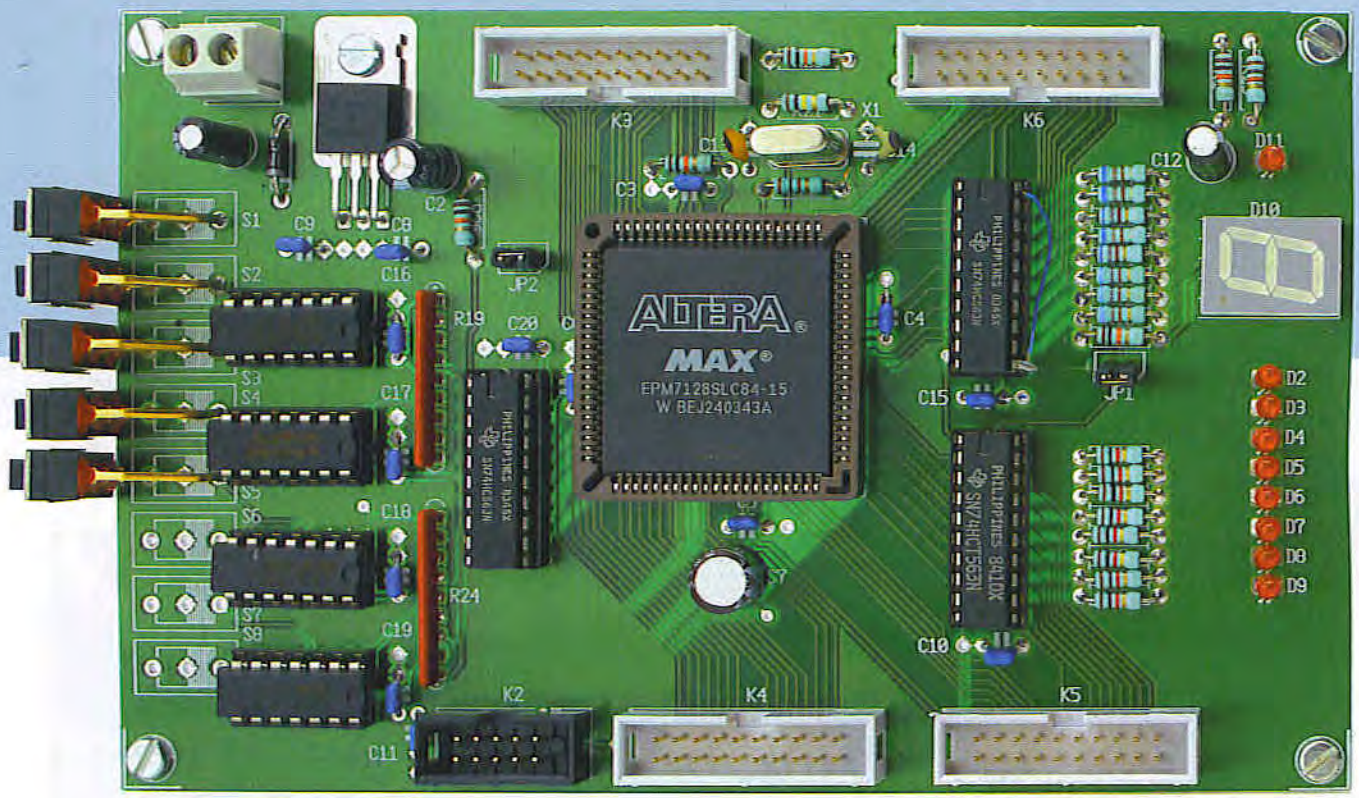

Figure 5. This photo of an assembled prototype of the circuit board shows that the switches can be fitted as desired; in this case five are fitted.

The signal generated by the combination of AND and OR operations then arrives at the register and its surrounding logic. This portion can be used as a D-type, T-type, JK or SR flip-flop, or it can be completely bypassed if no register is needed.

Fortunately, as designers we do not have to be overly concerned about exactly how our designs can be implemented in this manner. This is where the (free) software comes to our aid. But before we delve into the software, let's first take a closer look at the experimenter's board.

Experimenter's board

Our experimenter's board has a reasonably simple design. Nevertheless, it has more than enough I/O for performing our initial experiments with CPLDs. Naturally, all of the relevant pins of the CPLD are brought out via several connectors, to allow external hardware to work together with the board afterwards.

The schematic diagram, which is shown in **Figure 3**, is fairly simple. The supply voltage of approximately 9 V_{DC} is applied to connector K1. IC2 and its surrounding components provide the 5-V operating voltage for the entire circuit. LED D11 and R25 provide a 'power on' indication.

The CPLD is shown in the schematic diagram as IC1. The JTAG programming interface is brought out via K2. The pin layout of this connector is compatible with the Altera ByteBlaster, which means it is also compatible with the *Elektor Electronics* Parallel-to-JTAG interface (see the September 2002 issue, page 34). The reset circuit is formed by RC network R1/C12. Finally, an oscillator is implemented using R21, R22, C13, C14 and X1. The manner in which these components can be used together with the CPLD to make an oscillator is described later on in the examples.

A certain amount of simple I/O is indispensable on every experimenter's board. IC3 is a buffer that boosts several signals from the CPLD and uses them to drive LEDs D1–D8. IC4 performs a similar function for driving a 7-segment display. If these I/O functions are not desired, they can be decoupled from the CPLD by removing jumper JP1.

We decided to use eight switches for the inputs. To make your initial experimenting relatively easy, these eight switches (S1–S8) are equipped with a debouncer circuit. This function is provided by IC5–IC8. These inputs are connected to the CPLD via IC9, but here again this part of the circuit can be decoupled from the CPLD. In this case, JP2 is responsible for coupling the signals to the CPLD.

Finally, connectors K3 through K6 make all relevant CPLD signals available to the outside world.

Construction

The double-sided printed circuit board shown in **Figure 4** is generously dimensioned in order to keep everything readily accessible. All connectors are placed at the edge of the circuit board. Fitting the components to the circuit board should not present any difficulties. Anyone who is interested in CPLDs will certainly have already built other circuit boards. When fitting the components, you primarily have to pay attention to the proper orientation of the ICs, LEDs and electrolytic capaci-

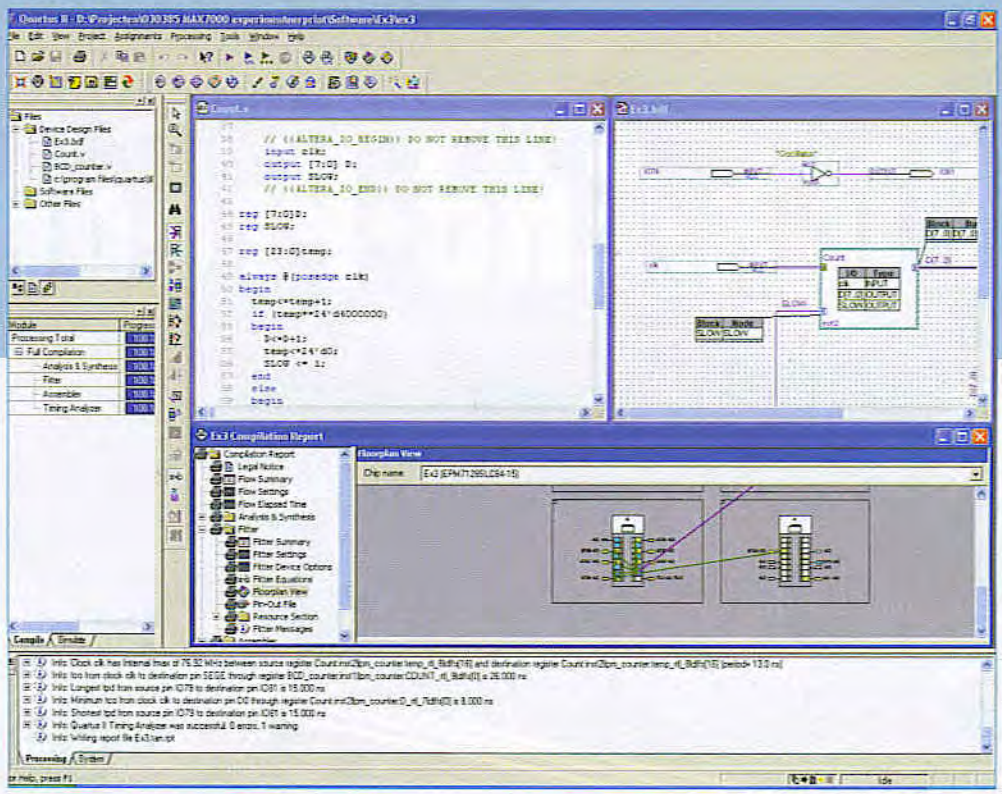

Figure 6. This screen shot gives an impression of Altera's free Quartus software.

tors. Sockets are definitely recommended for the ICs, and a suitable 84-pin PLCC socket is essential for the CPLD. Make sure that the bevelled corner of the PLCC socket is correctly positioned on the circuit board (refer to the component overlay), since it can also be fitted incorrectly into the holes in the circuit board. Incidentally, the CPLD fits into the socket in only one orientation.

Portions of the circuit that are not used can be disconnected from the CPLD by means of jumpers JP1 and JP2. Naturally, you can also simply omit the unneeded components. For instance, IC4 along with LD1 and R11–R18 can be omitted if the 7-segment display is not necessary. The same holds true for IC3 together with D1–D8 and R2–R9 if you don't need any LED indicators. As for the switches, you only need to fit the ones that are needed for the initial experiments.

The voltage regulator (IC2) is fitted flat against the board and secured using a small screw and nut. An additional heat sink is not necessary, at least as long as any additional hardware connected to the board does not draw too much current.

The supply voltage can be provided by a mains adapter that supplies approximately 9–15 V at a current of at least 100 mA. This value applies to the experimenter's board by itself and must be increased by the amount of current drawn by any additional hardware that may be present.

Software

PC software that can generate the necessary programming files and program them into the IC is required for programming the CPLD. Fortunately, the manufacturer of the CPLD has a nice (and free) software package for this purpose (see **Figure 6**). This software is called Quartus, and it can be downloaded from the manufacturer's website (http://www.altera.com/).

On the home page of this site, select *Design Software* under the *Products* heading. This will cause a new window to appear, where you should select *Quartus II Web Edition*. After this, follow the instructions displayed on the screen. However, you shouldn't overlook the size of the download. The file is a hefty 144.9 MB, so if you have a dial-up link, it might be more convenient to have someone else with a faster Internet connection download this file! After installing the software, you must request a free license. Exactly how to do this is clearly explained on the Altera website.

Next month

Next month we will use several examples to explain how you can design a circuit using Quartus, and of course we will describe how to try out these examples using the experimenter's board. For programming the CPLD, you will need a JTAG interface in addition to the experimenter's board. The previously mentioned Parallel JTAG Interface from the September 2002 issue of *Elektor Electronics* is suitable for this purpose.

While you're waiting for the next issue of *Elektor Electronics*, we recommend that you read the Quartus tutorial. It can be found under the Help menu. Using this tutorial, you can already familiarise yourself with the organisation of the software and examine the features of the software.

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