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Power Management Considerations for FPGAs and ASICs

— By David Baba, Staff Application Engineer

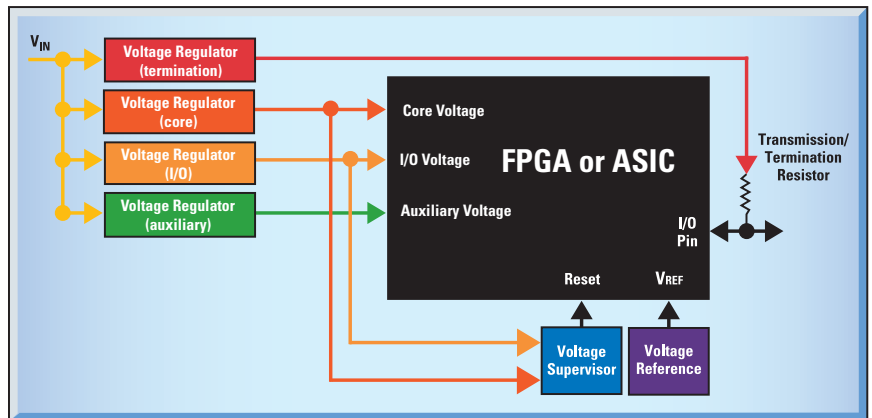


Figure 1: Typical FPGA or ASIC power management requirements

In today's hypercompetitive markets with increasing time-to-market pressures for electronic sub-systems, the importance of FPGAs and ASICs has been elevated to the point that they frequently contain the critical functionality of the new system. One of the most critical factors in an FPGA system design is power management. To power an FPGA effectively, a detailed system overview is needed. These same techniques often apply to ASICs.

Power supply requirements are important because of the complex initial conditions, transient behavior, turn-on, and turn-off specifications, among many others. Bypassing or decoupling the power supplies at the device (in the context of the device's application) also requires careful attention. *Figure 1* shows typical power management requirements for an FPGA. Usually a minimum of two voltages are needed to power FPGAs: one for the "core" (1.0V to 2.5V typ.) and one for the "I/Os" (3.3V typ.). Many FPGAs also require a third low-noise, low-ripple voltage to provide power to the auxiliary circuits. Typical voltages are 2.5V or 3.3V depending on the individual FPGA family.



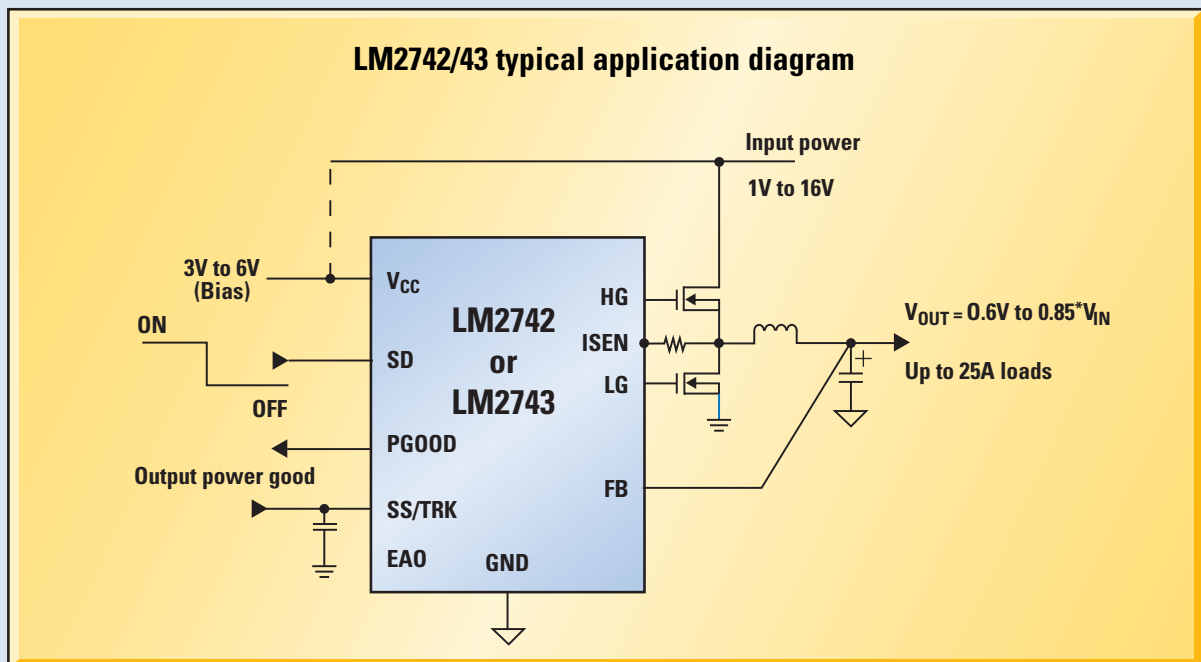
NEXT ISSUE:

Powering Portable Devices

 **National
Semiconductor**
The Sight & Sound of Information

Up to 2 MHz, 95% efficient synchronous buck controllers

LM2742/43/44 PWM controllers with adjustable output voltage down to 0.6V



Features:

- Input power from 1V to 16V
- Drives 1A to 25A output current with high efficiency
- Switching frequency from 50 kHz to 2 MHz
- Ceramic or electrolytic output capacitors
- High bandwidth error amplifier
- Reference accuracy $\leq 1.5\%$ (-40°C to $+125^{\circ}\text{C}$)
- Power Good flag and output enable for easy sequencing
- Current limit without sense resistor
- Adjustable soft start and tracking
- V_{CC(IN)} from 3V to 6V (LM2743/44) or 5V (LM2742)
- Available with external reference (LM2744)
- Available in TSSOP-14 packaging

Product Highlight:

Provides 1A to 25A output at up to 95% conversion efficiency

Ideal for low output voltage FPGAs, ASICs, and Point-Of-Load applications

Power Management Considerations for FPGAs and ASICs

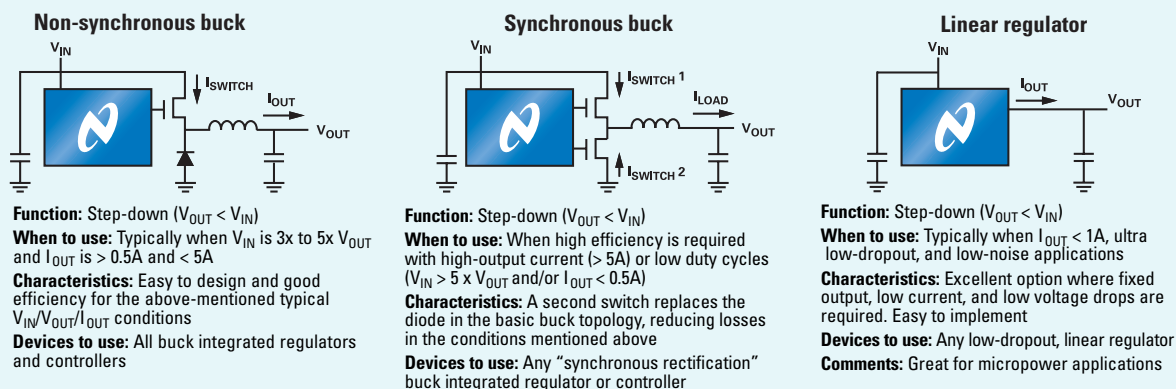


Figure 2: Step-down configurations

Operating current for each of these voltages is not fixed and depends upon many application-related factors, such as FPGA speed, capacity utilization, and the like. Operating current can vary from as low as 100 mA to as high as 20A. Usually in these systems the input voltage is higher than any of the voltages supplied to the FPGA and hence needs to be stepped down and regulated. *Figure 2* shows the three most commonly used step-down configurations for FPGAs. They are the synchronous buck, the non-synchronous buck, and the linear regulator. Consideration of the system specifications and the regulator operation will determine the type of regulators to use. The following aspects also need to be considered to achieve successful designs.

Input voltage (V_{IN})

The input power to the FPGA is supplied by a silver box, backplane, or intermediate rails. Typical input voltages range from 3V to 15V or as high as 30V in some industrial applications. The input voltage may exclude a part from being used; this is because a regulator has a maximum rating on the V_{IN} pin for powering the IC.

Output voltage (V_{OUT}) and output current (I_{OUT})

The function of the regulator is to maintain constant output voltage against variations in input voltage and load current variations. As mentioned previously, operating currents can vary from as low as 100 mA to as high as 20A. The combination of input voltage, output voltage, and output current will decide the type of regulator to be used. As a rule of thumb:

- Use a linear regulator if the power dissipated within it is less than 1W
- Use a non-synchronous buck regulator if the input-to-output voltage ratio is less than 2:1 and the output current is less than 3A
- Use a synchronous buck regulator if the input-to-output voltage ratio is greater than 2:1 with the output current exceeding 5A

A regulator regulates the output voltage by comparing a reference voltage to a fraction of the output voltage appearing at the feedback pin. The reference voltage usually sets the minimum output voltage achievable.

Some controllers have a minimum on-time. This will limit the ability of the regulator to step down large amounts relative to the input. The minimum on-time (T_{ON} min.) of the controller limits also sets the minimum output voltage achievable at a given frequency. For example, the minimum on-time being exceeded will make the output voltage rise above the desired level.

$$V_{in} = 12V$$

$$V_{out} = 1.2V$$

$$D = \frac{1.2V}{12V} = 0.1$$

$$F_s = 300kHz$$

$$T_{on_{min}} = 0.1 \times \frac{1}{300kHz} = 333ns$$

Industry's first 1A SOT-23 buck regulators

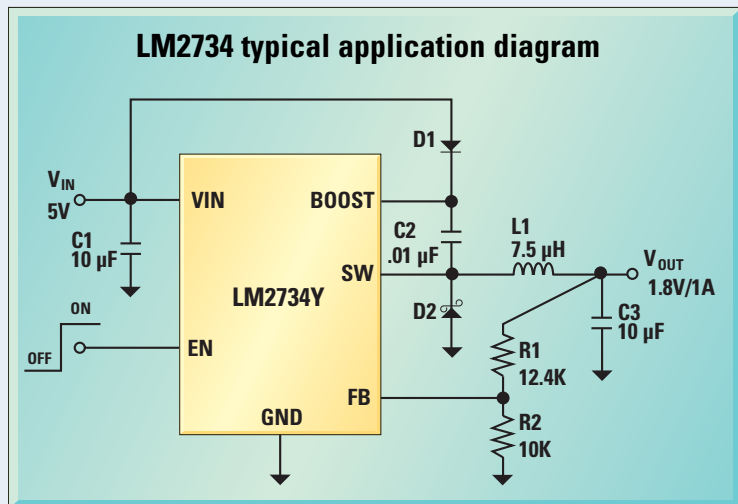
LM2734/36 buck converters with internal compensation simplify design

Features

- Complete, easy-to-use switcher solution in the smallest footprint
- Highest power-density
- High-frequency version prevents the switcher from interfering with signal-processing circuits
- Choice of switching frequencies allows designers to trade off efficiency, size, noise, and system performance
- Current mode allows improved transient response, current limit accuracy and more predictable regulation performance over the wide input voltage range
- PWM provides a predictable, easily filtered switch frequency for reduced noise

Product Highlight:

1A SOT-23 switchers with up to 3 MHz operating frequency and fast transient response



Product ID	Clock Hz	I _{LOAD} (max)	V _{OUT} (min)
LM2734X	500 kHz	1A	0.8V
LM2734Y	1.5 MHz	1A	0.8V
LM2734Z	3 MHz	1A	0.8V
LM2736X	500 kHz	750 mA	1.25V
LM2736Y	1.5 MHz	750 mA	1.25V
LM2736Z	3 MHz	750 mA	1.25V

Ideal for systems that need to convert 3.3V, 5V, 12V or 16V intermediate rails to 1.5V or less where size is critical or when wall-transformer powered systems need significantly reduced size

Power Management Considerations for FPGAs and ASICs

Decreasing the switching frequency will allow a greater step-down ratio.

Operating frequency of switching regulators

The switching frequency dictates several critical parameters including the size of inductors and capacitors, efficiency, ripple voltage, and ultimately the footprint of the solution. Higher switching frequency allows the designer to use smaller inductors as well as a smaller output capacitance to obtain a lower ripple voltage. Higher switching frequency also facilitates the design of high-bandwidth systems. Additionally, the designer may need to operate outside a specific frequency band to prevent spurious interference. Using a buck regulator with adjustable frequency setting renders flexibility to the design.

Efficiency

The efficiency is the ratio of output power to input power and is an indication of the amount of wasted power. This is often a misunderstood parameter among system designers. If available input current is not limited or battery life is not critical, then the power dissipation—and not the efficiency alone—is what matters. The power dissipated in the system will directly affect the temperature rise of the system components, including the IC, MOSFETs, capacitor, and inductors. Also important is the power dissipated in a given area. As a general rule, with no airflow, 1W dissipated on one square inch of copper will have a temperature rise of 40°C.

For example, suppose:

$$V_{out} = 1.5V$$

$$I_{out} = 15A$$

$$\text{Efficiency} = 90\%$$

$$\text{Power Dissipation} = 2.5W$$

If this power is dissipated on one square inch of copper it will give a 100°C temperature rise.

Also consider the following example:

$$V_{out} = 1.5V$$

$$I_{out} = 1.5A$$

$$\text{Efficiency} = 81\%$$

$$\text{Power Dissipation} = 0.53W$$

This figure relative to the 90% efficiency in the previous example does not look so impressive. But power dissipation of only 0.53W on a one-inch square gives a temperature rise of only 20°C compared to 100°C in the previous example.

The power loss is more significant than the efficiency figure. Understanding this principle can help the designer optimize his or her efficiency demands and reduce the overall cost of the system.

Footprint

Reduction in area or height requirements will negatively impact both cost and efficiency for a particular design. For example, smaller inductors usually have a higher effective series resistance (ESR) than larger inductors. Low-profile inductors or low-profile electrolytic capacitors are generally more expensive. A multi-layer board minimizes the footprint, but generally increases overall cost.

Some designers may increase the switching frequency to reduce component sizes as discussed previously, but increasing the frequency will increase power losses. Making the board unnecessarily small usually costs more and may necessitate keeping the power losses lower than they need to be.

System costs

One aim of the designer is to optimize the cost of the FPGA power supply, but minimum supply costs does not necessarily equate to using the lowest cost regulator. For example, designers are sometimes quick to dismiss regulators with integrated FETs as being expensive, but in certain situations these can prove more economical than regulators with external MOSFETs.

Moreover, regulators with external FETs are more sensitive to board layout. A simple integrated switching regulator with internal MOSFETs can eliminate most of the noise sensitivity issues. Another example is dismissing the use of a dual buck converter in place of two single switching converters. Significant savings can be realized on the number of input capacitors required. Because

4.5V to 36V input bi-phase synchronous buck controller

LM5642 Dual buck converter with oscillator synchronization

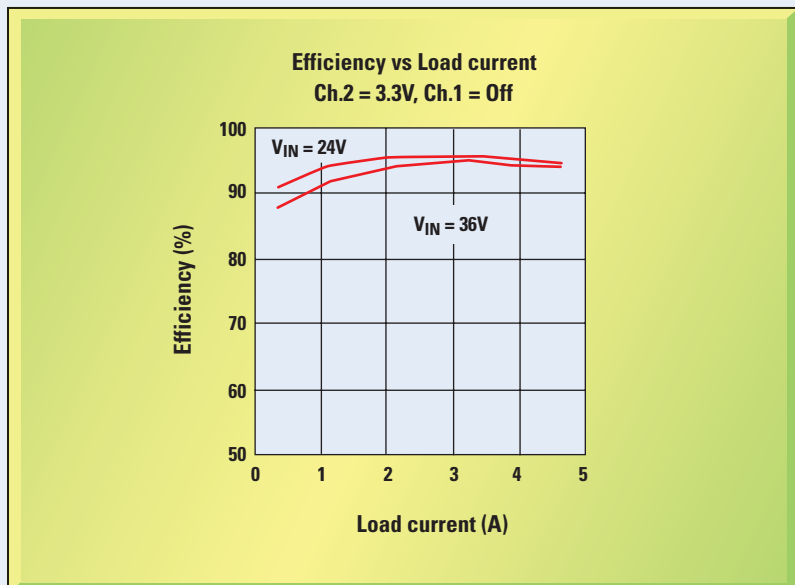
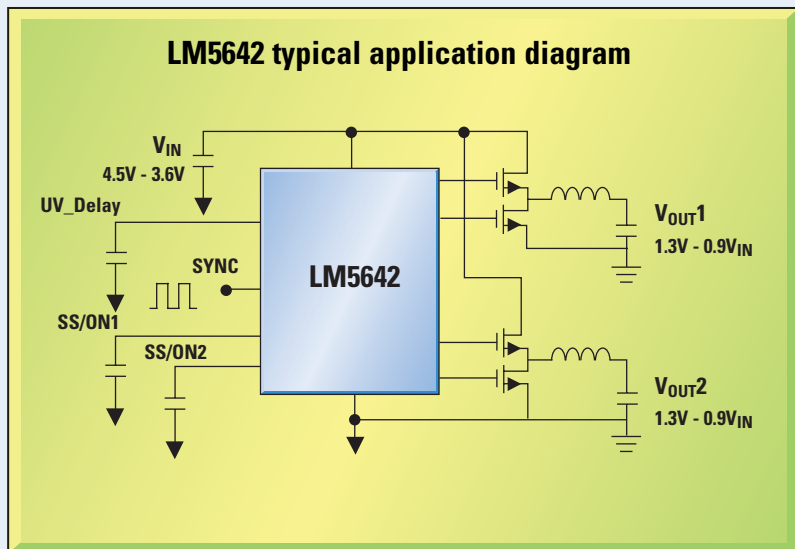
Features

- Two synchronous out-of-phase current-mode Buck controllers
- Synchronizable switching frequency up to 250 kHz
- 50 μ A Shutdown current
- Up to 96% efficiency
- Requires no additional 5V bias supply
- 0.04% (typical) line and load regulation error
- Independent enable/soft-start pins allow simple sequential startup configuration
- Configurable for single output bi-phase operation
- Adjustable, loss-less cycle-by-cycle current limit
- Available in TSSOP-28 packaging

Ideal for powering core and I/O voltages in FPGA systems and other POL power architectures

Product Highlight:

Out-of-phase buck controllers offer frequency synchronization and up to 96% efficiency



Power Management Considerations for FPGAs and ASICs

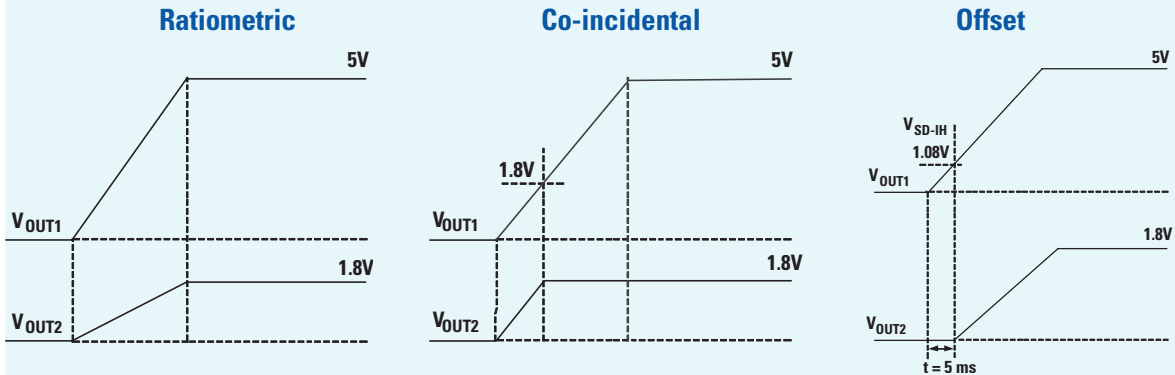


Figure 3: Types of sequencing and tracking options

the two phases can be made to operate out-of-phase, the RMS ripple current in the input capacitor is greatly reduced. Using a dual-phase controller can also eliminate beat frequencies that occur with non-synchronized switchers running at slightly different frequencies. Remember that true cost is the system Bill-of-Material (BOM) cost, not individual components alone. Beyond these requirements FPGA systems may have one or more of the following specific requirements:

Transient response

The core voltage of the FPGA can produce extremely high slew rates on the operating current. This requires the controller to deliver large step-load current while minimizing perturbation on the output voltage. The ability of the controller to respond to these loads is also known as transient response. The transient response requirement dictates the operating bandwidth in conjunction with the output capacitance and its ESR.

Sequencing and tracking

During start up, it may be necessary for one supply to ramp up before the other. If sequencing is ignored, the supply can “latch up” and the FPGA may be damaged or may malfunction. Some FPGAs have sequencing and/or tracking requirement between I/O and core voltages. (Refer to *Figure 3* for different types of sequencing and tracking options.) Sequencing and tracking can be

simply or flexibly implemented if the regulators have integrated power good, enable, soft-start and tracking functions. If not, external circuitry will need to be included to ensure correct sequencing.

Start-up requirements

If the FPGA voltage requires a specific ramp rate, this can be implemented using a soft-start capacitor. Also, the rising voltage at start-up usually needs to be monotonic (not droop). If the supply output capacitances are small, this can cause the voltage at start-up to droop. Adequately sized capacitors store enough charge to supply the start-up load transient of the FPGA.

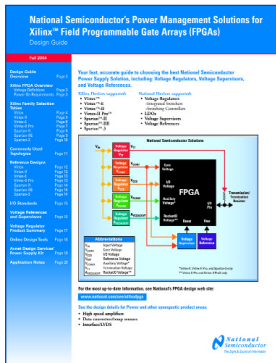
Synchronization

Synchronization enables two or more regulators to be locked together to one frequency. This eliminates the beat frequency that will otherwise be present if synchronization is not applied.

Summary of considerations

The best power supply configuration varies with the system requirements, as well as the complexity and capacity utilization of the FPGA or ASIC. Apart from the input voltage, output voltage, and output current, special requirements such as sequencing, tracking, and start-up conditions should be considered. Finally, power dissipation, footprint, and cost will influence the design. ■

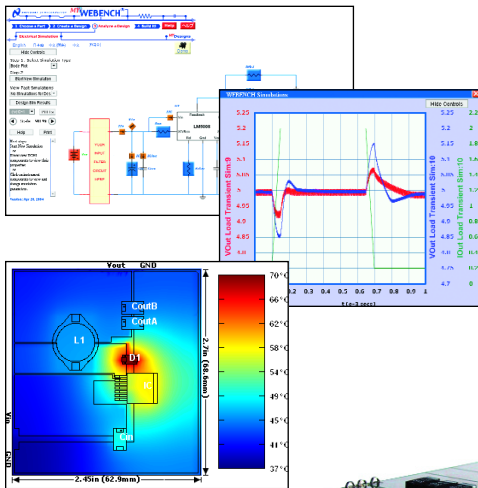
Power design tools



Xilinx FPGA Design Guide

This design guide features National's device solutions in voltage regulators, voltage supervisors, and voltage references by part number for various Xilinx product families. Parametric tables and block diagrams guide engineers toward solutions for their Xilinx-based designs.

View the guide online at:
www.national.com/see/xilinfpga



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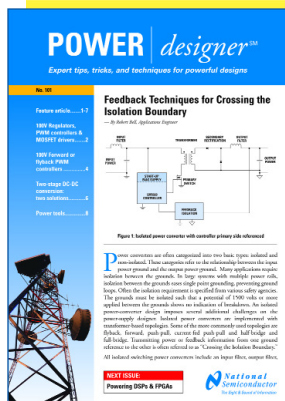
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