Hands-on CPLDs

Part 1: Experimental rev counter

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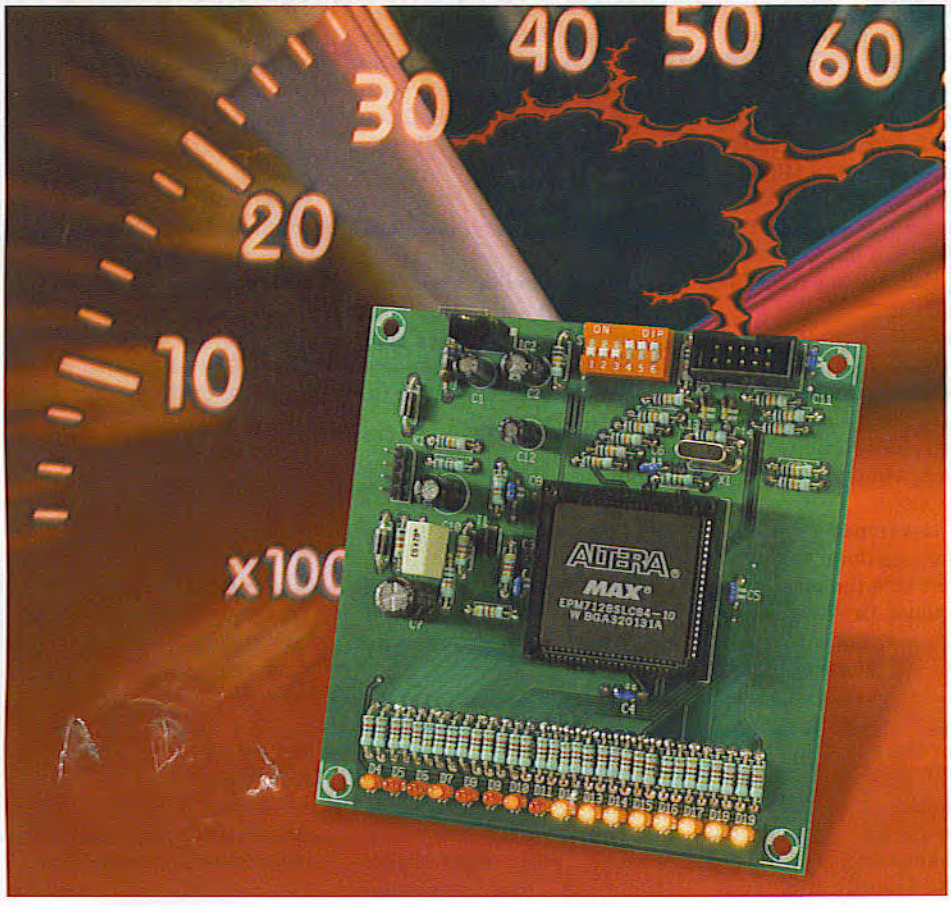
In the past Complex Programmable Logic Devices (CPLDs) have been something of a closed book to most semi-professional electronics enthusiasts but this hands-on series should go some way to help dispel that myth.

Times change. It wasn't long ago that programmable logic devices (PLDs) were thought to be the preserve of the specialist designer who with the help of expensive development environments and unwieldy software emulators took months to cram large digital designs onto a single PLD. Nowadays the whole process has been simplified to such an extent that the only expensive bit of kit you are likely to need is a PC. An interface adapter is also necessary to connect to the in-circuit programming socket of the CPLD circuit board but its cost is relatively low. When you add to this the fact that the price of the chips themselves have tumbled greatly and the development software is now freely available, these devices start to look attractive even to the hobbyist.



Programmable Logic – An overview

Lift the lid on any piece of modern-day electronic equipment and you will be lucky to find any discrete components from say the 74' family of logic gates used in the design. Occasionally you may see a clock circuit or bus driver but these are essentially used for driving or buffering and do not have a logic function. High volume consumer products such as computer boards have all the logic functions implemented in ASICs (Application Specific Integrated Circuits). The per-unit cost of an ASIC is quite low but there is also the expensive (one off) mask cost to consider. The equipment manufacturer must be sure of the potential market before a commitment to use ASICs in a design is made.

In the equipment development

phase and also for low-volume production ASICs are not cost effective; here the favoured technology is the Programmable Logic Device or PLD. These devices started to appear back in the 80's and since then many more companies have got in on the act to offer bigger and better devices in all sorts of package outline and more recently with lower operating voltages.

The first examples had relatively few registers (flipflops), required a lot of external buffers/drivers and consumed quite a lot of power. On top of this there was also special equipment necessary to program the device. Most of these chips were one-time programmable so that if a mistake was made in programming or some function required modification then the programmed devices could not be reused. On cost alone (development and simulation software together with the programmer device) PLDs were never considered suitable for the hobbyist.

As we said at the beginning times change, PLDs now offer far more gates per package and have become reusable. The real breakthrough came with the 'in system programmable' devices. As the name suggests these chips are fitted permanently into the finished equipment and can be reprogrammed via a 10-pin JTAG interface connector fitted somewhere on-board. The interface allows several devices to be daisy-chained and programmed from just the one connector. The devices do not require a socket so this has led to an increase in the device pin density right up to the BGA package outline. A few manufacturers still offer devices in the more user-friendly PLCC outline which is more suited to a typical hobbyist project.

The necessary development software from practically every chip manufacturer is now freely available for download from the Internet. A simple piece of hardware like the ByteBlaster from Altera is all that you need to connect a PC to the JTAG connector on the PCB. Regular readers will remember the ByteBlaster compatible 'Parallel JTAG Interface' design featured in the September 2002 edition of *Elektor Electronics*.

CPLDs (Complex PLDs) evolved from PLDs and the next step along the way is FPGAs (Field Programmable Gate Arrays). The main difference besides the increased complexity is that CPLDs (mostly using EEPROM technology) do not lose there programming data when the device is powered down.

In contrast FPGAs must be reprogrammed every time they are switched on. Reprogramming is performed automatically from a 'boot device' (either a serial EEPROM or flash memory) fitted to the PCB. The reason for this is that it is not yet possible to fabricate high-speed EEPROM technology at the necessary cell density required for an FPGA.

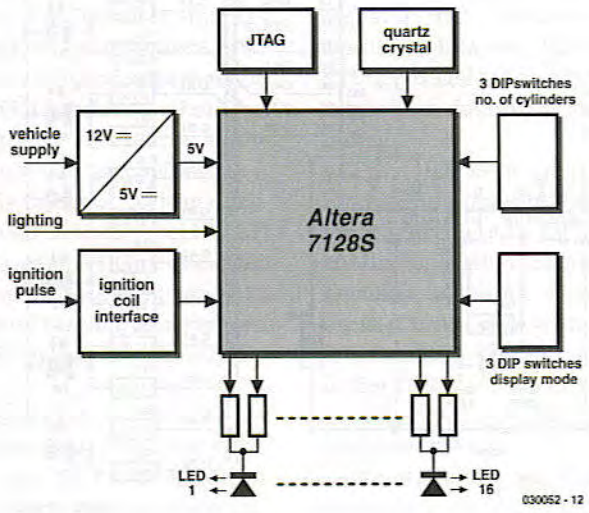


Figure 1. Block diagram of the digital rev counter.

The clock speeds of FPGAs can be several hundred megahertz and some manufacturers are offering SERDES technology that pushes the data rate up to 3.7 Gbps (10 Gbps will no doubt be available by the time you read this) these devices include complete processor cores (ARM, NIOS). Dropping the supply voltage down from 5 V to around 1.5 V has also led to reduced power dissipation in the device.

Around 90% of all FPGA's sold are supplied by three manufacturers: Xilinx, Altera and Lattice. FPGAs have an enormous capacity of gates and can be used in thousands of applications. They also do not have the expensive one-off mask costs of an ASIC.

Hands-on

This article and its follow-up does not concentrate too heavily on a theoretical textbook approach to the use of CPLDs in digital designs instead we use a practical hands-on method. Here we build a digital rev counter (tachometer) suitable for use in most cars or motorbikes.

The rev counter design is quite straightforward and should make a good introduction to the use of CPLD technology. This article takes you through the complete process of construction and programming and will give a good foundation and insights into the advantages of this type of technology.

The project is described using a top-down approach; first we will take a look at the block diagram and point out the features of the CPLD at the hardware level. Next we will consider the peripheral circuitry and finally (in the second part) the internal structure of the CPLD and the programming process is described.

Figure 1 shows the block diagram of the digital tachometer circuit. The central component is the CPLD 7128S from Altera, this chip does all the work and is surrounded by some peripheral circuitry.

An interface is required to convert the ignition pulse from the low-tension connection on the ignition coil to TTL levels and remove any noise spikes that may be present on this signal. The 'lighting' input signal controls the light intensity of the LED column (the 12 V to 5 V interface is not shown on this diagram but can be seen in detail in **Figure 2**). Under daylight viewing the intensity can be at maximum but at night it needs to be dimmed to avoid dazzling.

The chip is programmed over the JTAG interface using a ByteBlaster interface adapter from Altera (or a ByteBlaster compatible interface) which connects to a PC parallel port.

A quartz crystal together with a few discrete components generates the chip clock. This clock is sufficiently accurate to ensure that the circuit will not require calibrating. The setting of three DIP switches allows the tachometer to be used on vehicles with different cylinder counts and ignition systems. Without reprogramming the circuit can be configured for one, two, three, four, six or eight cylinder engines using either single or double spark ignition. Three more DIP switches are used to change the display mode. This allows the range of displayed revs to be changed to suit the performance of the vehicle engine:

1000 to 6000 rpm with a resolution of 3 LEDs per 1000 rpm.

750 to 4500 rpm with a resolution of 4 LEDs per 1000 rpm (Diesel mode).

2000 to 10000 rpm with a resolution of 2 LEDs per 1000 rpm (motorcycle engines).

4000 to 6000 rpm high resolution mode with 8 LEDs per 1000 rpm.

5000 to 7000 rpm (the so called 'Schumacher mode').

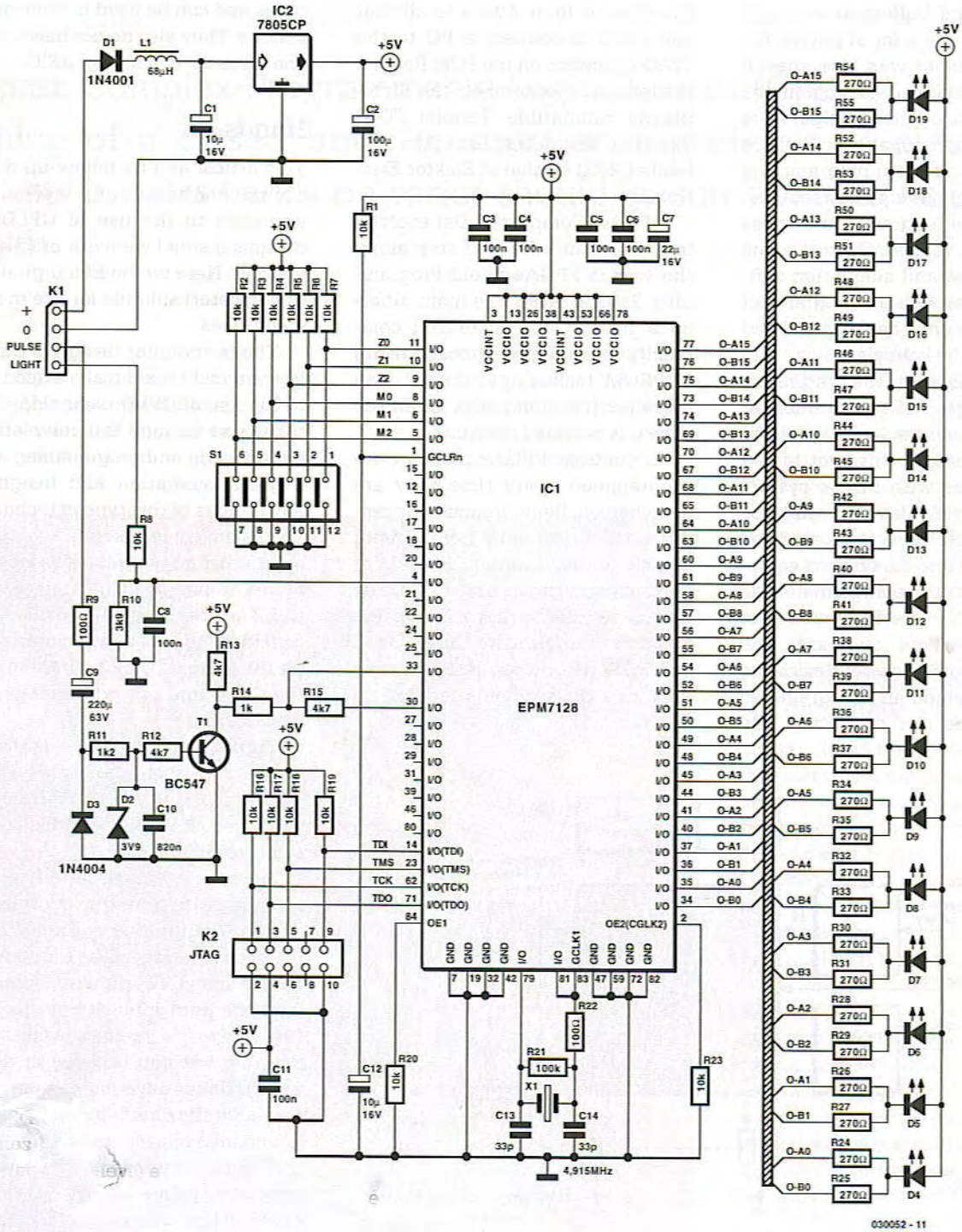


Figure 2. The complete circuit.

Almost any type of display representation including non-linear can be programmed into the CPLD and selected by three DIP switches. To make programming easier there is an Excel spreadsheet available that calculates the frequency scaling necessary in the program given the oscillator frequency and the required display resolution.

The tachometer display consists of a single line of 16 LEDs. Each LED is driven by two outputs from the IC and through two series resistors. The reason for this is that the data sheet indicates that the maximum output current is limited to 12 mA; most standard LEDs require around twice this current if they are to be visible under daylight conditions. Low power LEDs could be used to solve the problem but here the use of two outputs to drive one LED gives us a simple method to indicate not just the rpm but also each 1000-rpm graduation that glow differently.

The peripheral circuitry

Figure 2 shows the detail circuit diagram of the tachometer. IC1 is the CPLD type EPM7128S from Altera packaged in a 84-pin PLCC outline. The chip has a total of eight ground pins that must all be connected to GND.

There are also two types of VCC connection on the chip. Two of these connections (both called VCCINT) are connected to the core of the chip while the other six (VCCIO) supply power to the I/O buffers. This supply can be connected to either 3.3 V or as in our case 5 V. For other applications it would be useful to be able to use 3.3 V if it was found necessary to reduce the EMI produced when the buffers switch or it would greatly simplify interfacing to 3.3 V logic.

For supply decoupling it is good practice to use at least one 100 nF capacitor for each VCC connection sited as close as possible to the pin and one or two tantalum capacitors (10 to 22 µF) to reduce any supply rail noise.

Four connections are used for the JTAG programming interface (TDI, TMS, TDO and TCK). TCK is the clock input used during programming. TDI is not as you may have thought some kind of diesel engine but in this case the data input signal. This signal together with the data output (TDO) allows several CPLDs to be daisy chained by connecting TDO to TDI of the next chip. The TDO of the last chip is then connected to the JTAG interface. TMS is used to configure the JTAG interface for reset, data, command, boundary scan and so on. All four pins are fitted with a 10 kΩ pull-up resistor.

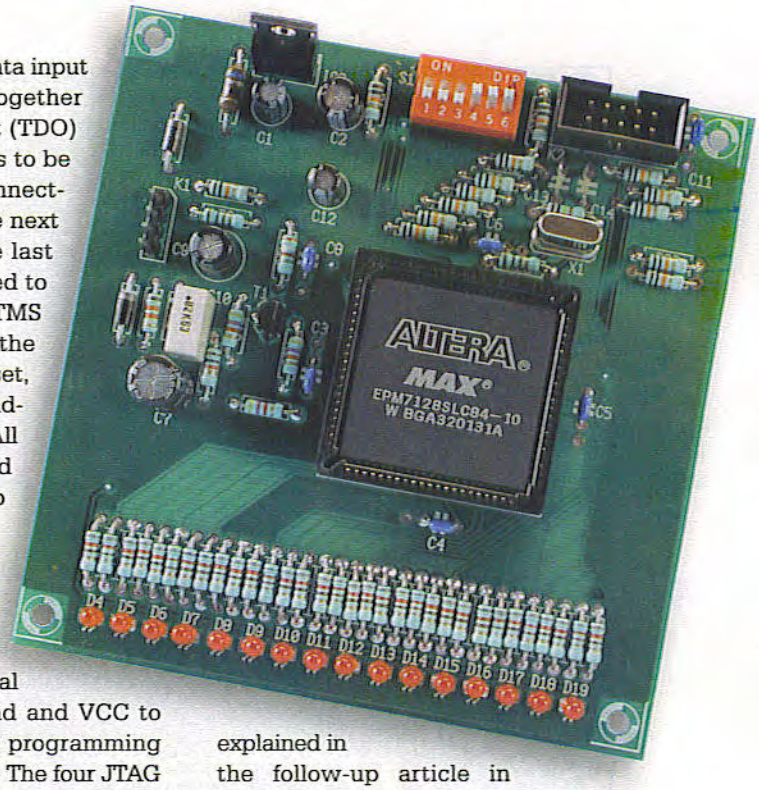
The connector for the JTAG-Interface (K2) is a 10-way header plug. Along with the four signal wires are also ground and VCC to supply power to the programming adaptor (ByteBlaster). The four JTAG connections can also be used as general-purpose I/O pins but this is only advisable if there are no other I/O pins available.

R1 and C12 provide a reset pulse to the active low Global CLeaR input (GCLRn) during power-up. This reset clears all the chips internal registers.

GCLK1 is the first of the two global clock inputs. It is important to ensure that the first system clock for the CPLD is connected to this input and not to some general purpose I/O pin which is not internally wired to the cells and registers. Two I/O pins close to the GCLK1 input are used as a buffer to interface to the crystal. The output from the buffer is connected directly to GCLK1 input. Resistor R22 reduces the output loading while the 100 KΩ resistor R21 in parallel to the crystal provides a positive feedback path for the buffer.

Pin OE1 is a general Output Enable, and must be defined in the programming data. OE2 (GCLK2) is another special function pin and can be used as either a second clock input (for designs with two clocks) or as a second output enable input. In the tachometer design described here both of these functions are not required.

All other components and external signals are connected to general-purpose I/O pins. The criteria used to allocate these pins will be explained in the follow-up article in *Elektor Electronics*.



The remainder

Power for the circuit is supplied by the 12 V vehicle battery via connector K1. Diode D1 prevents damage to the circuit if the supply polarity gets mixed up. L1 filters noise spikes on the supply to the 5 V regulator IC2 while C1 and C2 are also used to provide noise decoupling. The complete circuit takes about 0.5 A worst case so power dissipation in the voltage regulator is given by:

$$P_v = 0.5\ A \cdot (14.4\ V - 5\ V) \approx 5\ W$$

It is important to ensure that the heatsink for IC2 can dissipate this amount of energy.

The six way DIP switch S1 is used to select the vehicles engine cylinder count and the display mode. When a switch position is open circuited a 10 kΩ resistor pulls the line up to 5 V. R8 and R10 reduce the voltage on the 'light on' signal to TTL levels while C8 reduces any noise spikes on this input.

The signal from the ignition coil is conditioned by the circuitry around transistor T1, it produces a filtered TTL compatible output signal for IC1 from the 'raw' ignition signal. C9 AC couples the signal. The negative transition of the pulse is clamped to -0.7 V by diode D3 while R9 protects D3 from excess power dissipation. R11 and zener diode D2 limit the positive level of the pulse to 4 V. C10 filters out high frequency noise while R12, T1 and R13 form a transistor switch which produces a clean TTL compatible output pulse to the IC from the noisy ignition signal.

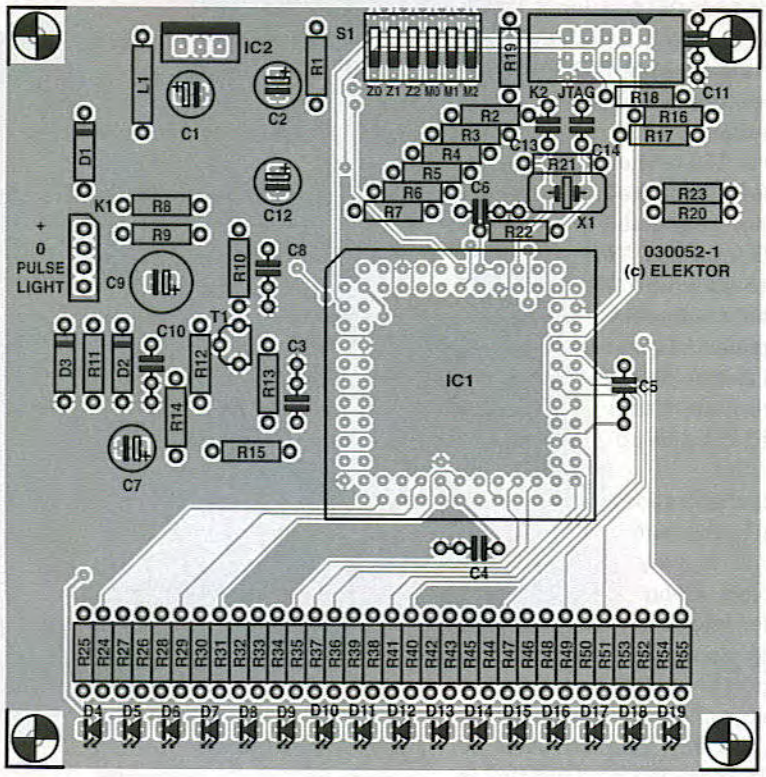


Figure 3. Component mounting plan for the double-sided PCB.

COMPONENTS LIST

Resistors:
R1-R8,R16-R20,R23 = 10kΩ
R9,R22 = 100Ω
R10 = 3kΩ9
R11 = 1kΩ2
R12,R13,R15 = 4kΩ7
R14 = 1kΩ
R21 = 100kΩ
R24...R55 = 270Ω

Capacitors:
C1, C12 = 10µF 16V radial
C2 = 100µF 16V radial
C3-C6,C8,C11 = 100nF
C7 = 22µF 16V radial
C9 = 220µF 16V radial
C10 = 820nF
C13,C14 = 33pF

Semiconductors:
D1,D2,D3 = 1N4001
D2 = zener diode 3V9, 500 mW
D4...D19 = LED, green, 3 mm
IC1 = EPM7128SLC84-15
IC2 = 7805CP
T1 = BC547A

Miscellaneous:
K1 = 4-way SIL pinheader
K2 = 10-way pinheader
L1 = 68µH choke
S1 = 6-way DIP switch
X1 = 4.9152MHz quartz crystal
PCB, available from The PCBShop
Disk, order code **030052-11** or
Free Download

Web Addresses

www.xilinx.com
www.coolpld.com

www.altera.com

www.latticesemi.com

Resistors R14 and R15 control the hysteresis of a Schmitt trigger input. This is quite important because any noise on the ignition input signal would cause the tachometer to give a false reading. R15 provides the feedback from the output side of the input buffer. When the buffer changes state a small proportion of its output is fed back out from pin 30 on IC1 to reinforce the input signal via R15. This has the effect of shifting the voltage threshold at which the buffer can switch back (hysteresis) and so masking the effects of noise on the input.

Free Downloads

Excel spreadsheet.
File number: 030052-11.zip
PCB layout in PDF format.
File number: 030052-1.zip

www.elektor-electronics.co.uk/dl/dl.htm,
select month of publication.

The PCB and future developments

A double-sided PCB has been produced specifically for this tachometer project. The PCB and component placement diagram is shown in **Figure 3**. Component mounting should be fairly straightforward but take care not to allow any solder debris to enter underneath the PLCC socket where it could short between PCB tracks. Correct orientation of the IC is important so ensure that the clipped corner of the package outline corresponds to the corner of the socket and silk-screen printed IC outline on the PCB. Ensure correct polarity of the LEDs, capacitors and diodes when they are fitted to the board.

When any circuit uses a line of discrete LEDs the finished project always looks a bit amateurish if the LEDs are not uniformly in-line. A good tip here is to firstly solder just a single leg of each LED in place. The board can now be flipped over and all the LEDs carefully bent or re-soldered into exactly the right position before the second leg of the LEDs are soldered.

The layout is not too cramped so there is no reason why this PCB could not also be used as a development platform to prototype other CPLD designs. Those of you however who are looking for the flexibility of a true evaluation board should not be disappointed by our EVA-board that we shall be featuring in a forthcoming article in *Elektor Electronics*.

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In the second part of this article we will take a closer look at the CPLD internals and device programming.