Pulse-width monitor flags poor timing

by T. G. Barnett and J. K. Stothers, *Neonatal Research Group, London Hospital Medical College, London, England*

Pulse intervals can be monitored to ensure they fall within a specified range by using two complementary-MOS 4098 dual monostable multivibrators. The original application of this circuit was to monitor biologically produced pulse trains. However, the principle can be applied to any case where it is necessary to know if the limits of a pulse interval have been exceeded.

The 4098 is two independent one-shots in a single package and each one-shot has leading- and trailing-edge triggering, retriggerable and nonretriggerable modes as well as a reset and complementary outputs. These facilities have been incorporated within a monitor that senses whether a pulse train has intervals longer or shorter than those of a chosen range.

The period of each one-shot may be obtained from its data sheet or approximated by:

$$T(\text{time}) = 0.5 \times RC$$

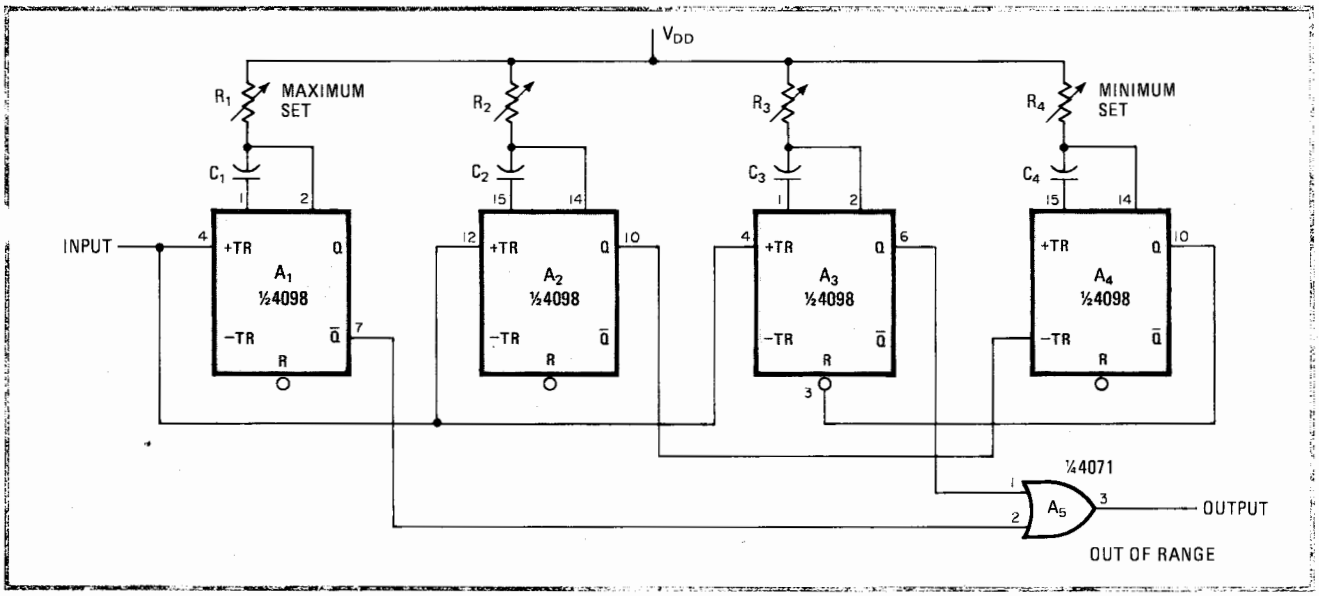
for values of $C \geq 0.01$ microfarad.

The value of the capacitor should be as small as possible and the resistor should not be more than 10 megohms. All unused inputs must be connected to either the drain- or source-supply voltage in accordance with the data-sheet instructions.

As the circuit in the figure shows, monostable A_1, operated in the retriggerable mode, is triggered on the leading edge of an input pulse. The $\overline{Q}$ output is normally low unless the input-pulse interval is greater than the duration of the monostable's pulse-width value, set by resistor R_1 and capacitor C_1. If the pulse interval exceeds this value, then $\overline{Q}$ will go high, resulting in the output of the 4071 OR gate going high. Thus the maximum interval time is set by this monostable.

The leading edge of the input pulse also triggers monostables A_2 and A_3, both of which are operated in the retriggerable mode. Output Q of A_2 acts as a delay and is fed into the trailing-edge–trigger input of A_4, whose Q output drives the reset pin of A_3. The delay that is caused by A_2 is a few microseconds and prevents A_3 from being triggered on receipt of the leading edge of the input pulse, as its reset pin is low until A_4 is triggered. A_4 is operated in the nonretriggerable mode and sets the minimum-pulse–interval time.

The Q output of A_3 will go high only if its reset pin is set high by A_4, whose Q output will go high only a short time after A_3 has received a trigger pulse. However, if a further input pulse is received within the time the Q output of monostable A_4 is high, then monostable A_3 will be triggered, its Q output will go high, and the 4071 OR gate will go high. The actual pulse width of A_3, set by R_3 and C_3, can be chosen to suit any application. □



1. Watching it. Out-of-bounds time intervals between a train of pulses are detected at OR gate A_5 because one-shot A_1 stays triggered unless the time between pulses is too great. Meanwhile one-shot A_3 triggers if it receives successive pulses too soon. It also drives the OR gate