Pulse-frequency doubler requires no adjustment

by Thomas McGahee
Don Bosco Technical High School, Boston, Mass.

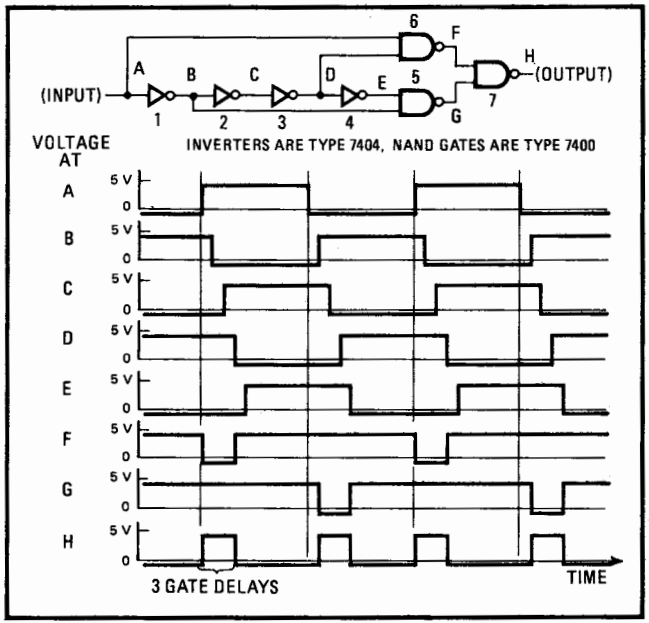
Sometimes a frequency doubler is needed in a digital system, and unfortunately most doubler circuits have to be adjusted for a particular operating frequency. However, this circuit, which has operated successfully in a specially designed divide-by-N counter, requires no adjustment over a range from near dc to 10 megahertz.

When a signal pulse passes through the circuit, each inverter introduces a small delay, typically of 20 nanoseconds, in addition to inverting the pulse. For example, the signal at point D inverts 60 ns after the input signal at point A has inverted; thus, gate 6 continues to have high signals at both of its input terminals for 60 ns after the input at point A changes from low to high. As a result, the output from gate 6 (i.e., point F) will go low for 60 ns after a positive-going transition at the input to the circuit.

Somewhat the same thing occurs at gate 5, except that it develops a 60-ns low output after a negative-going transition at the input. In the circuit diagram, inverters 1, 2, and 3 all serve double duty in producing these 60-ns low pulses at points F and G. This design reduces the number of gates needed.

The pulses from gates 5 and 6 are fed to the terminals of gate 7, which produces a positive pulse 60 ns wide every time either one of its input terminals goes low. Since one terminal goes low on the leading edge of each input pulse at point A, and the other terminal goes low on the trailing edge of each input pulse at A, the frequency of the output pulses at point H is twice the frequency of the input pulses at point A.

The output is in the form of positive pulses that are 60 ns wide. There is a 20-ns difference in the spacing between successive output pulses because the portion of the circuit that comprises the negative-going edge-detector has one more inverter stage than the positive-going edge-detector section does. This slight asymmetry is noticeable only at the highest frequencies. If particularly slow input signals are used, it is a good idea to place a Schmitt trigger just before the input. □



Frequency doubler. Propagation delays through inverters cause NAND gates 5 and 6 to go low for 60 nanoseconds following the rising and falling edges, respectively, of input pulse. Therefore output goes high twice as often as input.