Synchronous counters provide programmable pulse delays

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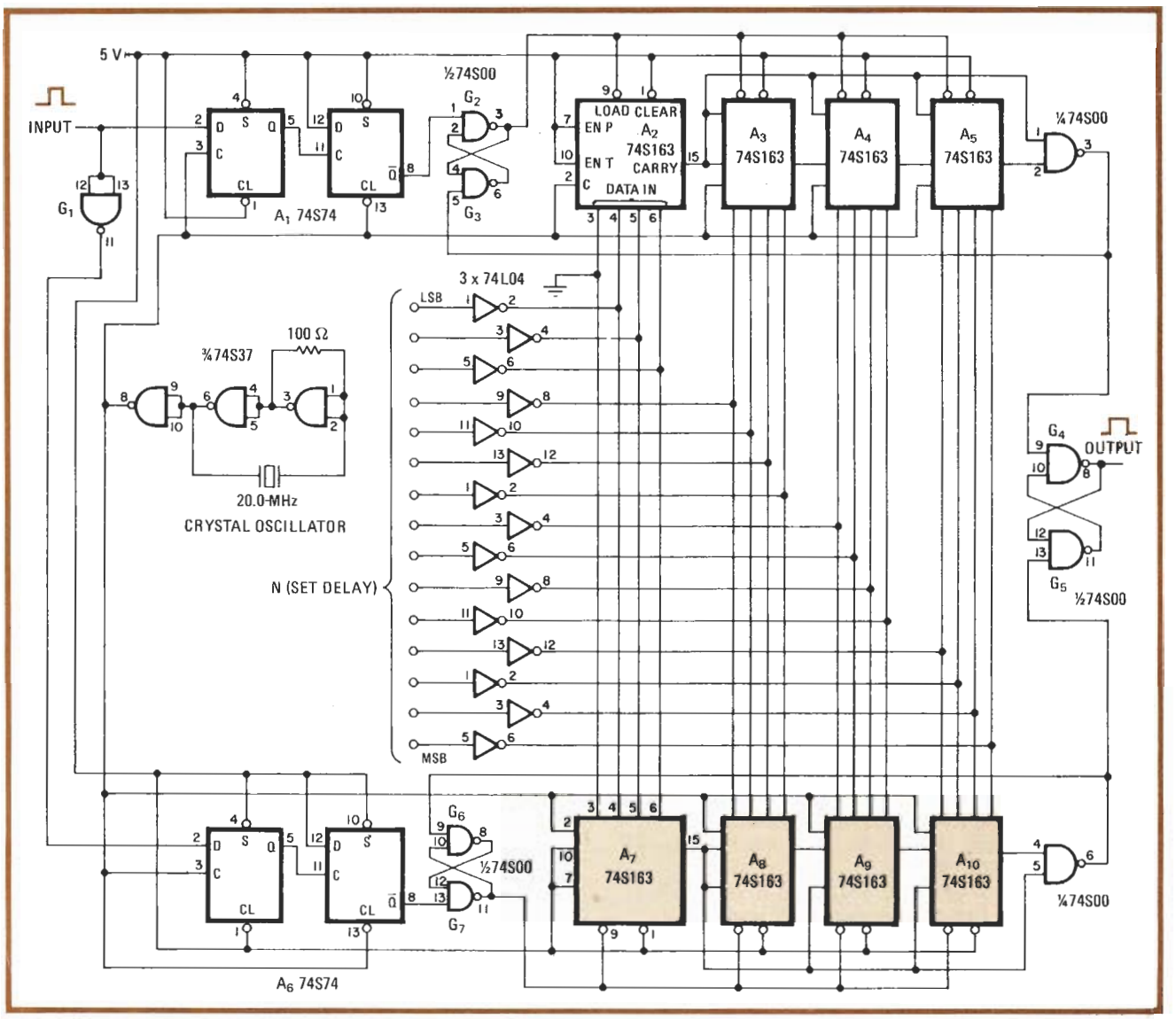
In this circuit, cascade counters are digitally programmed to provide pulse delays of 50 nanoseconds to 3.25 milliseconds, accurate to within 50 ns. Selected by a 15-bit binary number, N, the delays can be ordered in 100-ns steps.

Two chains of synchronous counters, driven by a 20-megahertz clock, delay the input pulse's leading and trailing edge separately. Input pulses, which are asynchronous, are first applied to a dual D flip-flop, A_1, as shown. A_1 generates a single negative-going clock pulse when triggered by the 20-MHz clock. The pulse is used to set the bistable latch, G_2–G_3, thus enabling counters A_2–A_5 to delay its leading edge.

A_2–A_5 are wired to perform a fast look-ahead operation for the high-speed multistage counting required. To eliminate glitches that might upset the counter, the carry outputs of both A_1 and A_5 are brought to a NAND gate and then to G_2–G_3. This ensures the latch will be reset and the desired N value loaded into the counter only after the previous delay period is ended, despite the differential delays that exist in the signal path.

The input pulse is inverted by G_1 and applied to flip-flop A_6 for the counters that provide delay on the trailing edge of the pulse, A_7–A_{10}. G_6–G_7 and A_7–A_{10} perform the function identical to G_2–G_3 and A_2–A_5.

In actual operation, both counter chains are programmed by the set-delay lines, which are connected to their data-in ports. The delay time is given by $T = 50(1 + 2N)$ ns. At the end of the delay period, N is



Two-edge retardation. Counter chains, of which one starts counting on arrival of the positive edge of an input pulse, the other on its negative edge, use a 20-MHz clock to provide repeatable delays of 50 ns to 3.25 ms on both edges of signal. Delays produced are accurate to within 50 ns. Amount of delay is selected with 15-bit word (M). Width of input signal to be processed must be at least 60 ns.

loaded into both counter chains. Note that the circuit is wired such that the N inputs must be active high, ensuring that maximum delay will correspond to a value of N that, when read as a number in standard binary form, is maximum.

Upon the arrival of the leading edge of the input pulse, A_2–A_5 count up, starting from the number loaded. Similarly, A_7–A_{10} count up on the trailing edge of the pulse. The carry pulse generated by A_5 signifies the end of the delay period. This signal is united with the carry pulse generated by the trailing-edge counter A_{10}, at flip-flop G_4–G_5. The signal at the output of G_4–G_5 thus has the same width as the input pulse, but is delayed by a period of time proportional to the number N. □