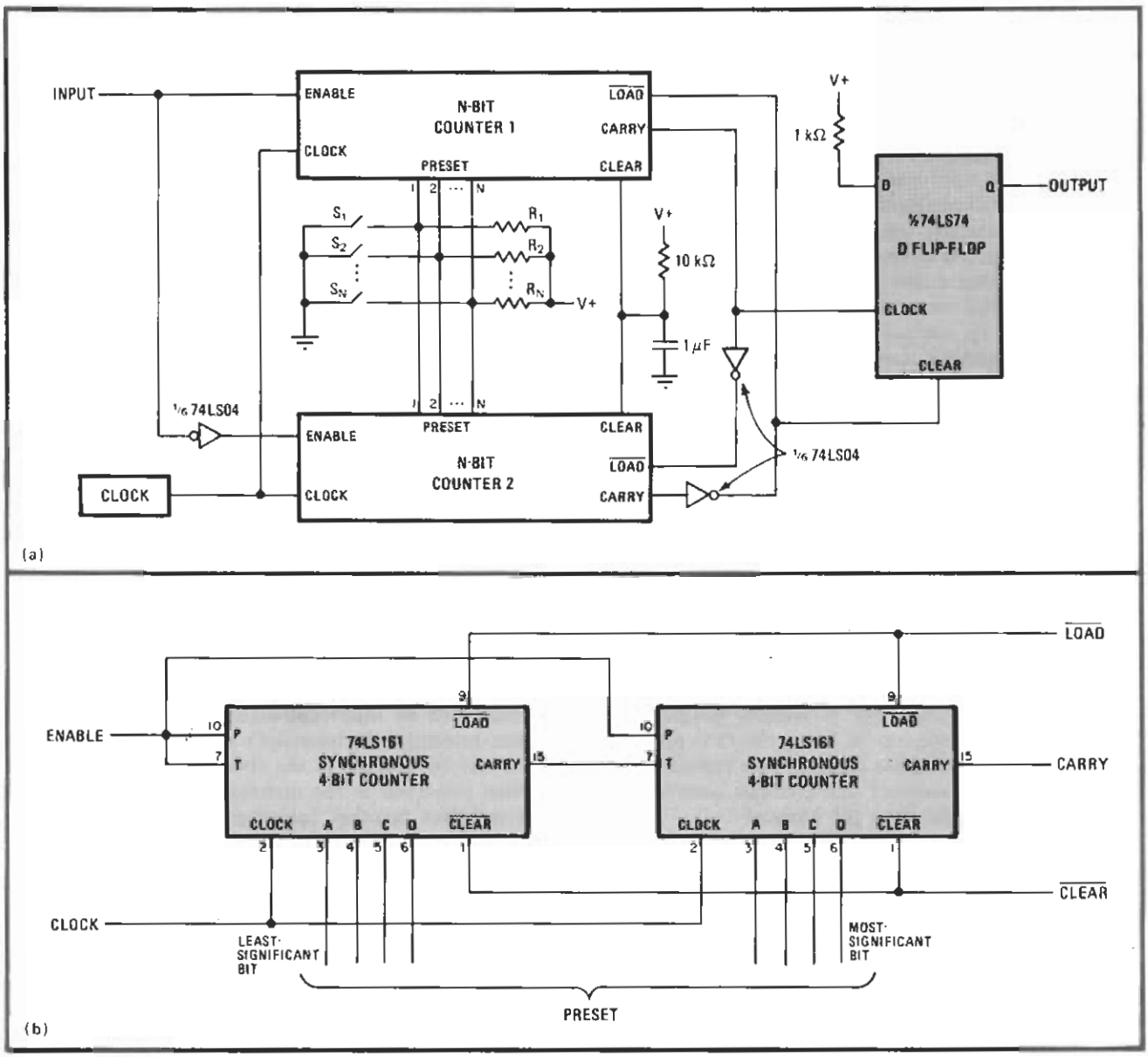
Counters and clock control phase shift

by Samuel Creason
Beckman Instruments Inc., Fullerton, Calif.

Although instruments often need phase shifters that offset signals by varying amounts, most shifters increment waveforms only in multiples of 90°. By using readily available counters and a simple clock, this inexpensive digital phase shifter offsets the phase of a square wave by any amount up to 180°. For different waveforms or if the input signal has a duty cycle other than 50%, the offset will be less than 180°. In addition, for precise applications, the input clock circuit may be used to fine-tune the phase shift.

The fundamental phase shifter (a) consists of a pair of cross-coupled preset counters, each of which is driven by the same clock. A waveform is applied directly to the enable input of counter 1, and the inverted input signal is applied to the enable input of counter 2. Counter outputs are then applied to a D-type flip-flop that provides the desired phase shift. When the input waveform is high,



Offset. This digital phase shifter can adjust the phase of the reference square-wave signal by any amount up to 180°. The fundamental circuit (a) uses a pair of cross-coupled counters; each counter is driven by the same clock and a D-type flip-flop to provide the desired phase shift. The hardware (b) is based on a pair of 74LS161 counters. The flip-flop uses a 74LS74 chip, while the clock is derived from a 555 timer.

counter 1 starts counting clock pulses and consequently generates a carry pulse. This carry pulse presets counter 2 for the next half cycle of the input signal and sets the flip-flop. As a result, a phase-shifted output is initiated.

When the input waveform goes low, counter 2 begins counting and generates a carry pulse, which presets counter 1 and clears the flip-flop, thereby terminating the output pulse. The amount of phase shift is determined by the number of clock pulses counted before a carry pulse is generated by the preset counter. Also, the clock frequency and preset count are selected to produce a carry pulse from each counter during each half cycle of the input.

A typical hardware implementation (b) shows a fundamental preset counter that is composed of a pair of 74LS161 4-bit synchronous counters. The clock uses a 555 timer and associated circuitry and is designed for a 10-hertz square-wave input, while the D-type flip-flop uses one half of the 74LS74 chip. □

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Outputs of op-amp networks have fixed phase difference

by Richard K. Dickey
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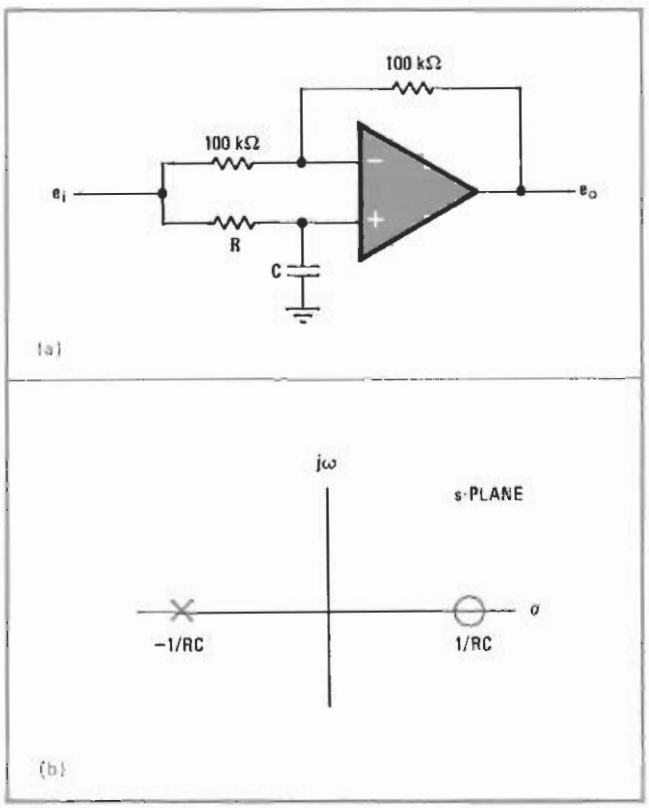
In the phasing method of single-sideband generation, two modulating signals are derived from the audio input. The two signals must have equal amplitudes, but must differ in phase by 90° at all frequencies in the audio band. A differential-phase-shift system that provides these two signals can be made from resistors, capacitors, and operational amplifiers.

The basic section of the constant-phase-shift system is the op-amp circuit shown in Fig. 1. The transfer function of this circuit is

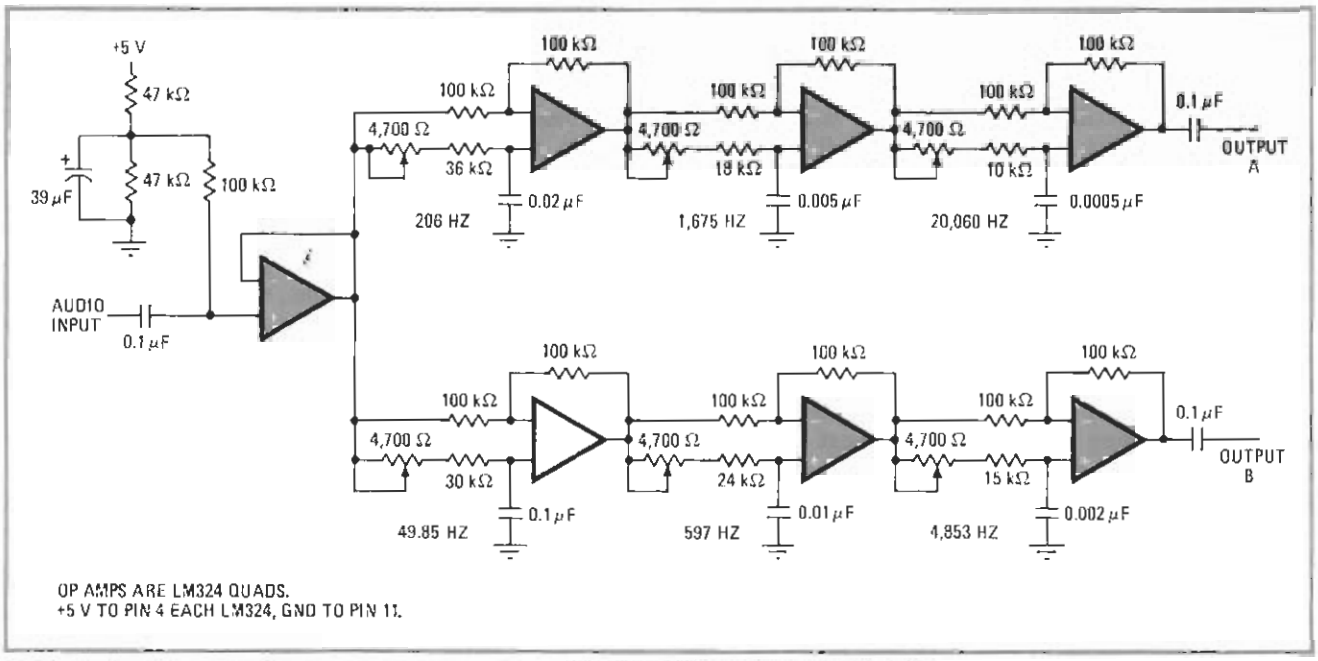
$$e_o/e_i = (1 - j\omega RC)/(1 + j\omega RC)$$
$$= 1 \angle -2 \arctan \omega RC$$

Thus the gain is always unity, and the phase shift decreases from 0 to -180° as frequency increases from zero to infinity. The shape of the phase-shift curve depends upon the time constant RC, i.e., upon the locations of the singularities in the s-plane plot that is included in Fig. 1.

If three of these basic sections are cascaded, the over-all gain remains constant at unity, and the over-all phase shift through the network falls from 0 to -540° at



1. Basic section. Op amp connected as shown (a) is a unity-gain phase shifter. Singularities of circuit are shown (b) in s-plane plot. Phase shift ranges from 0 at dc to -180° at infinite frequency; however, gain is unity at all frequencies.



2. Quadrature. Differential phase shifter converts audio-frequency input signal to two outputs, 90° out of phase, for SSB modulation. Simple transformerless circuit uses quad op amps driven by a single-ended 5-volt supply. The individual sections are adjusted for 90° phase shift at the frequencies indicated on the figure; the two outputs are then in quadrature to within 2° from 100 Hz to 10 kHz.

a rate that is determined by the three RC products.

Two such phase-shift networks, fed from a common input (as shown in Fig. 2), can be designed so that the phase shift through one lags behind the phase shift through the other by 90° over a substantial frequency range. The time constants are chosen so that the singularities of the two networks interlace.

The all-pass system in Fig. 2 provides two equal-amplitude outputs that differ in phase by (90 ± 2)° over the frequency interval from 100 hertz to 10 kilohertz. The various R and C values were calculated from the table published by S.D. Bedrosion, "Normalized Design of 90 Degree Phase Difference Networks," IRE Transactions on Circuit Theory, June 1960, pp. 128–136. In each section, $RC = \frac{1}{2\pi f}$, where f is the 90° frequency for that section as shown in Fig. 2. An exception is the 20,060-Hz stage, where R was decreased to compensate for the inherent phase shift in the op amp.

Each section of each network should be individually adjusted to an exactly 90° phase shift at the indicated frequency. This adjustment can be made by connecting the input and output of that section to the horizontal and vertical inputs of an oscilloscope, and then varying the 4,700-ohm potentiometer until the Lissajous figure is a circle. Alternatively, a phasemeter can be used.

Each op amp is one quarter of an LM324 quad amplifier. The input biasing network allows operation from a single 5-volt supply. □

Frequency doubler and flip-flop make adjustable phase shifter

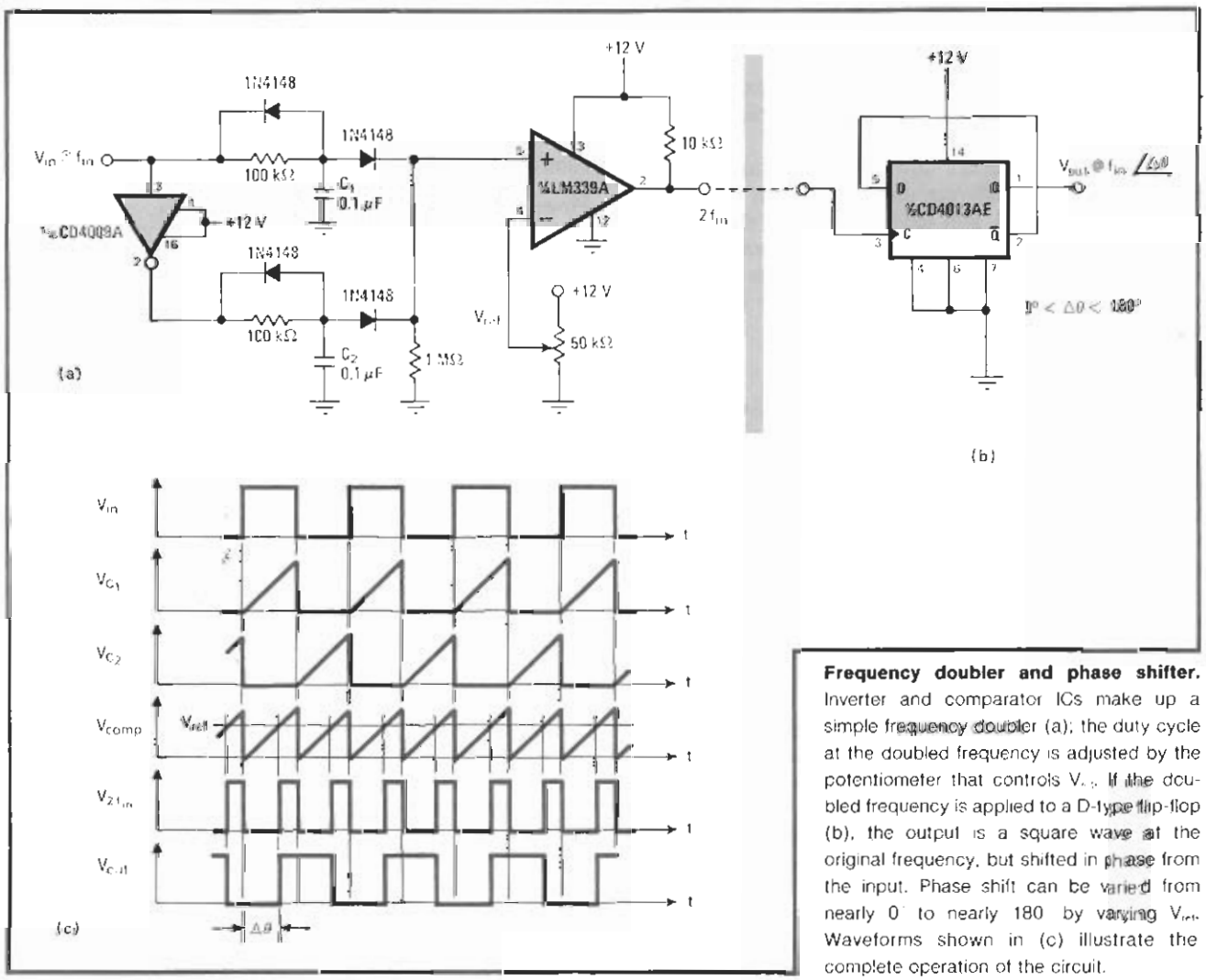
by Vladimir Brunstein
Nova Electric Mfg. Co., Nutley, N.J.

A frequency doubler for operation at the voltage levels of either complementary-MOS or transistor-transistor logic can be built with an inverter and a comparator. And if the doubled signal is then fed into a flip-flop, the output has the original input frequency, shifted in phase by an amount that depends on the reference voltage applied to the comparator. This shifter has been used to adjust the phase of the output from a phase-locked-loop device.

In the doubler circuit (a), the rectangular input signal and its inverted form are applied to capacitors C_1 and C_2. Their triangular ramps, which are 180° out of phase, are added through diodes to produce a sawtooth wave at twice the input frequency. This sawtooth is applied to the noninverting input of the comparator, producing a output at $2f_{in}$ with a duty factor that depends on the setting of the reference voltage at the inverting input.

Adding an edge-triggered D-type flip-flop to the circuit (b) yields an output signal of frequency f_{in}, phase-shifted with respect to the input signal. Varying the reference voltage V_{ref}, the phase shift between the output and the input signal can be set at any value between 0° and 180°. However, the duty factor of the output is always 50%. The frequency limit is set by the frequency band of the comparator used.

The component values shown were used for 60-hertz operation in a circuit that phase-locks the output of an uninterruptable power supply to the ac line. Connecting the output of the power supply back into the line provides a load that is inductive or capacitive, depending on the phase shift that is set by the reference-voltage potentiometer. □



Frequency doubler and phase shifter. Inverter and comparator ICs make up a simple frequency doubler (a); the duty cycle at the doubled frequency is adjusted by the potentiometer that controls V_{ref}. If the doubled frequency is applied to a D-type flip-flop (b), the output is a square wave at the original frequency, but shifted in phase from the input. Phase shift can be varied from nearly 0 to nearly 180 by varying V_{ref}. Waveforms shown in (c) illustrate the complete operation of the circuit.

Bucket-brigade shift register generates constant phase delay

by F.E. Hinkle
University of Texas, Applied Research Laboratories, Austin, Texas

A digitally programable constant-phase-delay network makes an interesting application for a bucket-brigade analog shift register. The circuit generates a phase delay, in degrees, that is independent of the frequency of the signal to be phase-shifted.

The analog shift register works in conjunction with a phase-locked loop so that the input frequency forms the time delay needed for a constant phase delay. The register delays the input by:

$$\tau = M/2f_v$$

where M is the number of register-delay elements or bits, and f_v is the frequency of the bit shift (biphase clock).

Since the frequency for shifting the analog bits is a function of the input frequency, the delay time will also be a function of input frequency. A phase-locked loop is used as a frequency multiplier, with a divide-by-N network in its feedback path. During lock, the frequency of the phase-locked loop will be an integral multiple of the input signal being applied to the shift register:

$$f_v = Nf_{in}$$

where N is the divide-by integer in the phase-locked loop, and f_{in} is the input frequency. When the frequency of the phase-locked loop is applied to the shift register as the bit-shift frequency, the new time delay of the register is:

$$\tau = M/2Nf_{in}$$

The delay time-to-angle conversion for the input sine wave can be defined as:

$$delay\ angle = (\tau/T_{in}) \times 360^\circ = (\tau f_{in}) \times 360^\circ$$

where T_{in} is the period of the input waveform. Substituting for τ in this equation yields:

$$delay\ angle = (M/2N) \times 360^\circ$$

The delay angle of the input waveform, therefore, is independent of that waveform's frequency. By using a programable divide-by-N circuit, the amount of the delay angle can be adjusted in the desired increments. For this circuit, when M = N = 185, the delay angle is 180° for all frequencies within the range of the phase-locked loop. The circuit's major limitation is the lock-on range of the phase-locked loop. □

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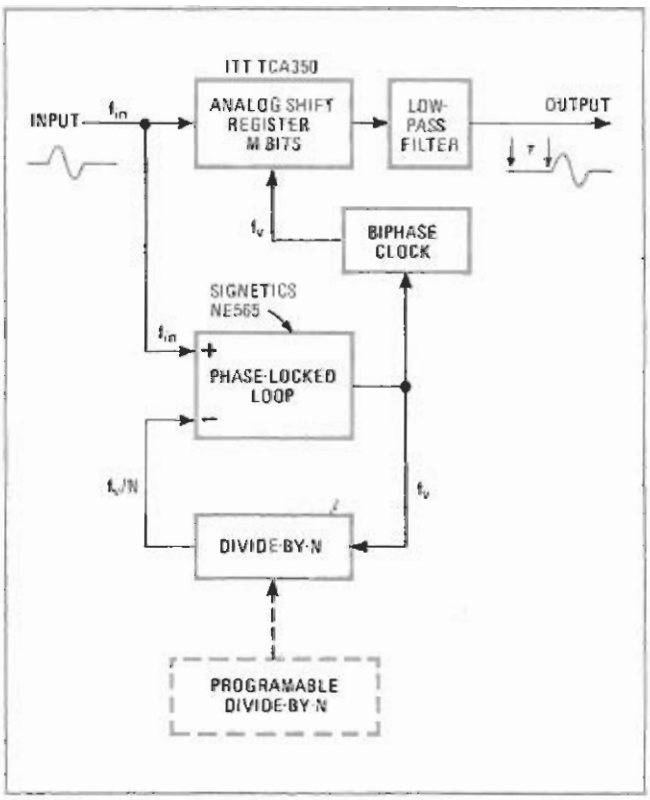

Controlled phase shift. Bucket-brigade analog shift register and a phase-locked loop provide a constant phase delay that is independent of the input frequency. The phase-locked loop determines the bit-shift frequency of the register, and a divide-by-N circuit sets the frequency of the phase-locked loop. The delay can be made variable by adding a programable divide-by-N circuit as indicated.

The analog shift register

Not too long ago, *Electronics* reported on the MOS bucket-brigade approach to building a charge-transfer device [Dec. 6, 1971, pp.86–91, and Feb. 28, 1972, pp.62–71]. One of the practical hardware functions of the bucket-brigade technology is an analog shift register [Nov. 22, 1971, pp.112–114]. Such a device is a rather unusual circuit that will store bits of analog data and delay them as a function of the input clock frequency.

The register used here, in the constant-phase-delay network, is made by ITT Semiconductors in Palm Beach, Fla. It will delay the input waveform by 185 stages. All that is required is a biphase clock, which can be as fast as 500 kilohertz, plus a low-pass filter at the output to remove the clocking waveforms. The register's output waveform will be an accurate sampled replica of the input, delayed by 185 clock pulses.

Since the shift register runs from negative voltages, some form of voltage-level conversion is necessary when TTL digital circuits are used to generate the biphase symmetrical clock signals. Another method of clock generation is to use C-MOS integrated circuits with the drain supply tied to ground and the source supply connected to a negative voltage. (A C-MOS decade counter can then be wired as a divide-by-four circuit and two of its outputs taken for the biphase clock.) The clock circuitry can be used to drive a number of registers simultaneously.

The type TCA350 shift register employed in the phase-shift network is housed in a TO-77 metal can. It costs less than $10.

until all the subframes have been scanned.

The location representing subframe 12 should be programmed so that a logic 1 appears at pin 11. This resets the counters and selects the first memory location in A_1, as before. The system generates the main-frame sync pulse again and the entire process is repeated. □

Phase-locked generator converts, filters most inputs

by Peter Reintjes
Research and Design Ltd., Morehead City, N. C.

Replacing the voltage-controlled oscillator in the RCA 4046 phase-locked loop with the popular Intersil 8038 waveform generator forms a circuit that produces sine, square, and triangular wave voltages capable of tracking almost any input signal. Besides performing its prime function of waveform conversion, the circuit serves as a high-Q filter. With a harmonic distortion of only 0.5%, it finds the fundamental frequency of any signal.

The performance of this circuit far exceeds that of a conventional filter, which always adds a phase shift to the incoming signal. Also, traditional filtering methods are often of little use when the fundamental frequency must be recovered from an unpredictable input signal.

Connecting the 8038, which is itself a voltage-controlled oscillator, to the 4046 as shown in the figure does not affect the normal operation of the phase-locked loop. The only difference in the basic PLL circuit is that the 8038 generates sine, triangular, and square waves and drives the 4046 in place of the loop's internal VCO. The output waveshapes are unaffected by the harmonic distortion present on the input signal. Capacitor C sets the center frequency of the 8038 (a value of 0.047 microfarad corresponds to a frequency in the audio range). The frequency-capture range of the circuit, which is determined by the 4046, remains 1,000 to 1. The generator's maximum operating frequency is about 700 kilohertz.

To secure precise locking, the comparators in the 4046 should be driven by the square-wave output of the 8038. If the input waveform is a pulse, phase comparator I should be used. For unpredictable or high-noise signals, phase comparator II is more suitable.

Any phase difference between the square-wave output of the 8038 and the input signal is amplified by two 741 operational amplifiers and then fed back to the VCO to increase or decrease its frequency, as the case may be. Although the internal VCO of the 4046 is not used, it must be enabled by grounding pin 5 of the device so that its voltage-follower will be active. If matched resistors are used at pin 4 and 5 of the 8038, the sine-wave output distortion can be reduced to 0.5%. Potentiometers R_1 and R_2 aid in minimizing the distortion. □

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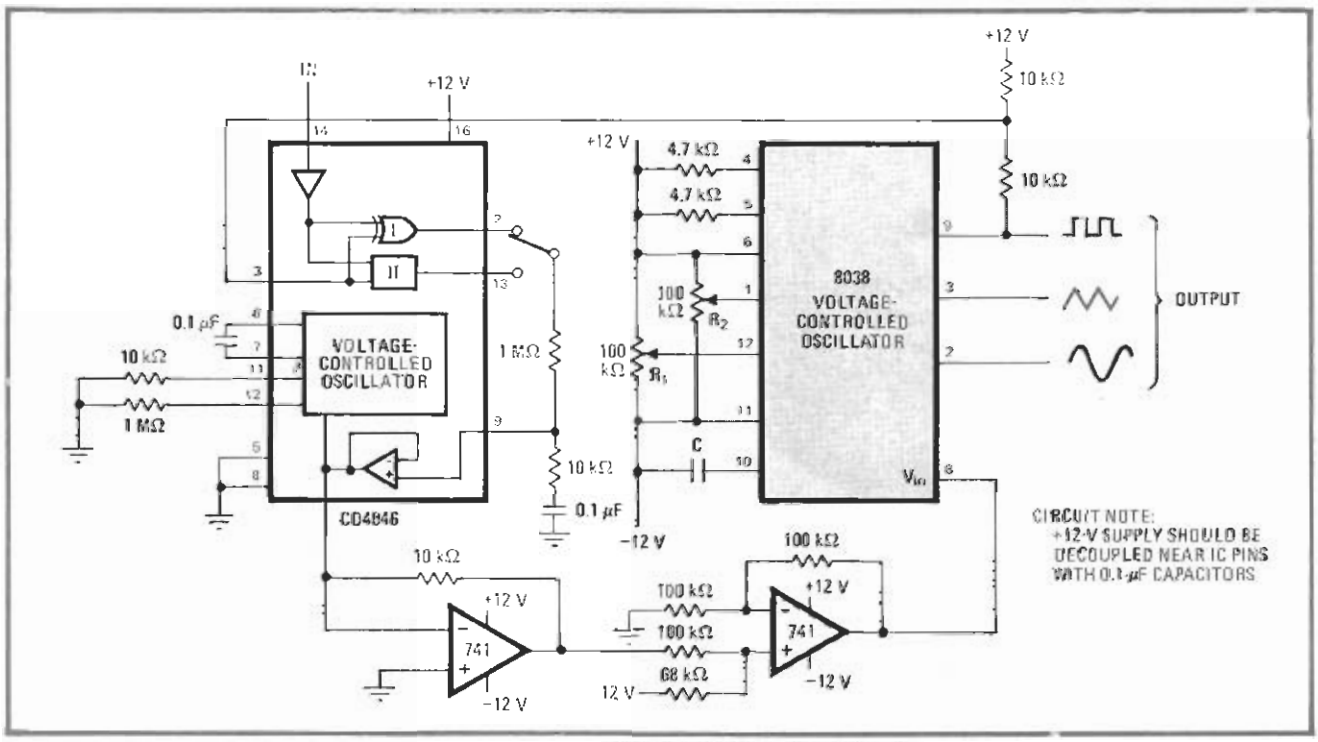

Tracking waveforms. ICL 8038 and two op amps replace internal VCO in 4046 to form phase-locked-loop waveform generator that can be used to recover fundamental frequency of any input signal or to convert the control signal to sine, square, and triangular waves. The generator's maximum output frequency is about 700 kHz. R_1 and R_2 are adjusted for minimum output distortion.