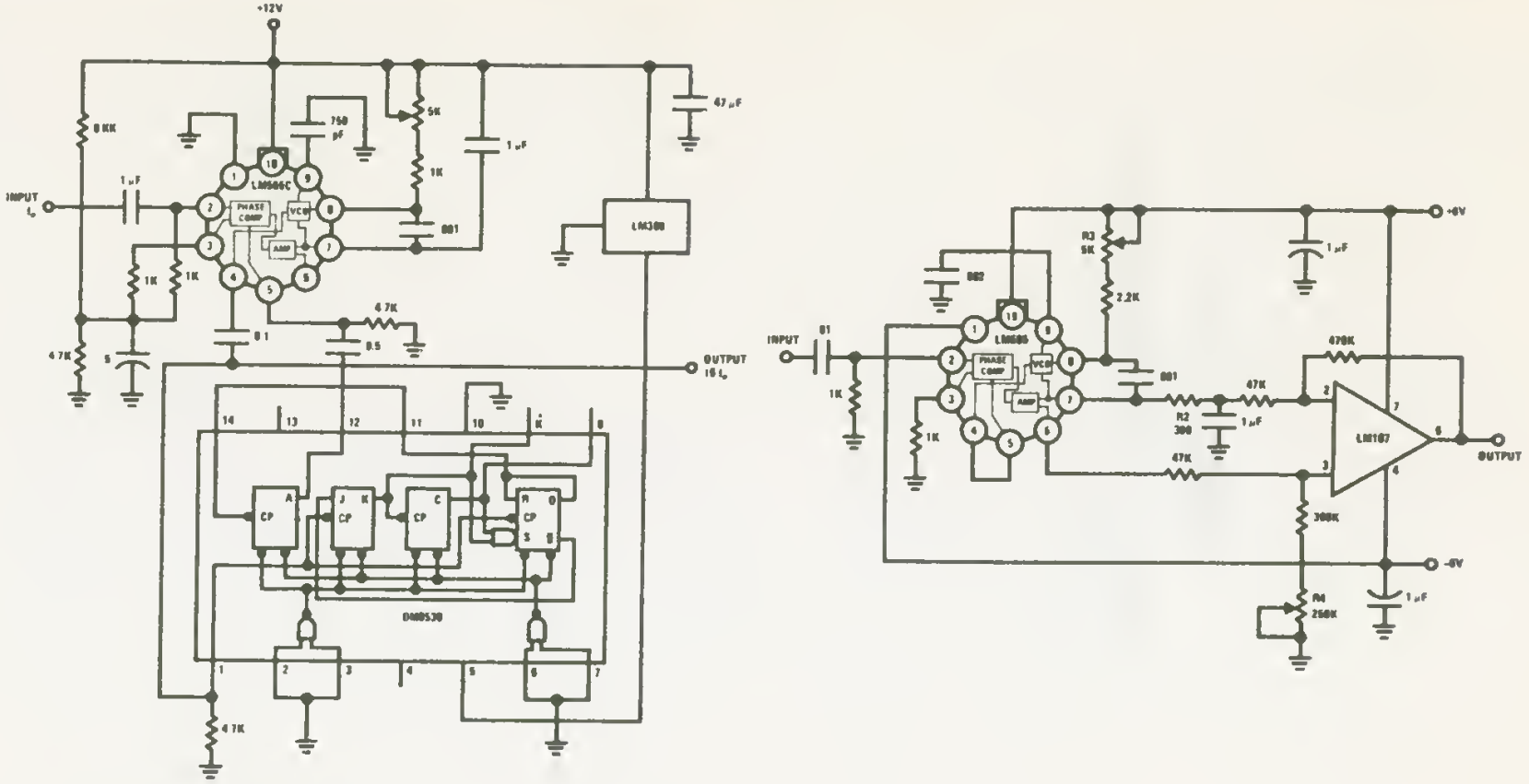


Fig. 23-1. Frequency multiplier (x10) (NS).

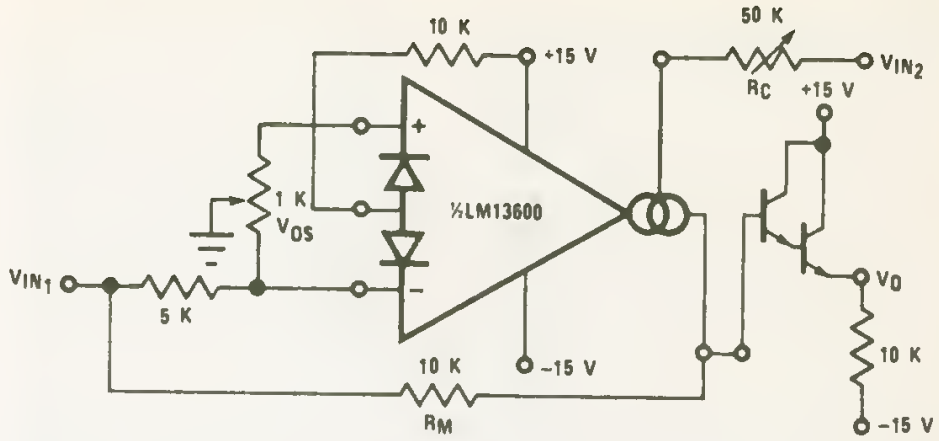
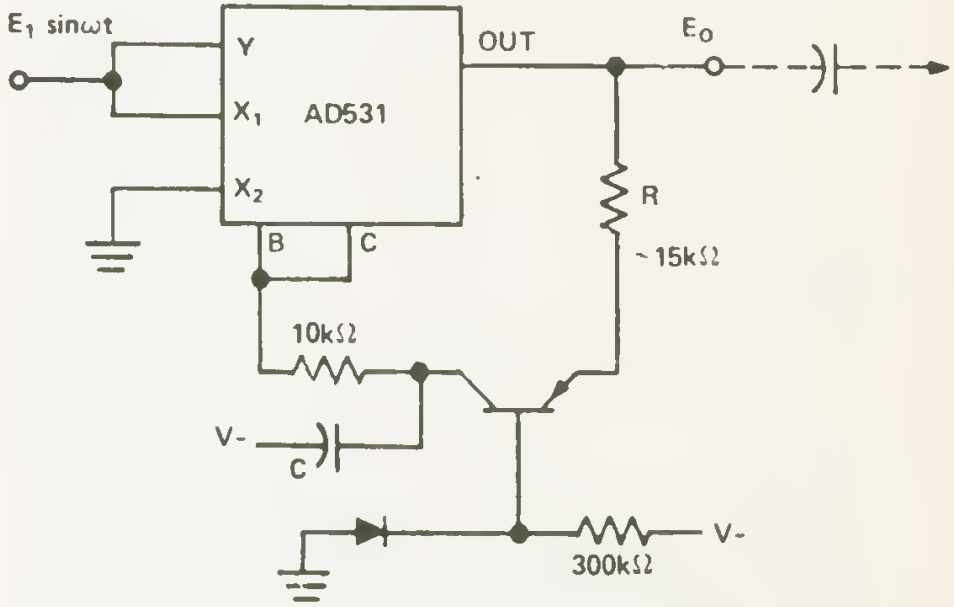


Fig. 23-2. Four-quadrant multiplier (NS).



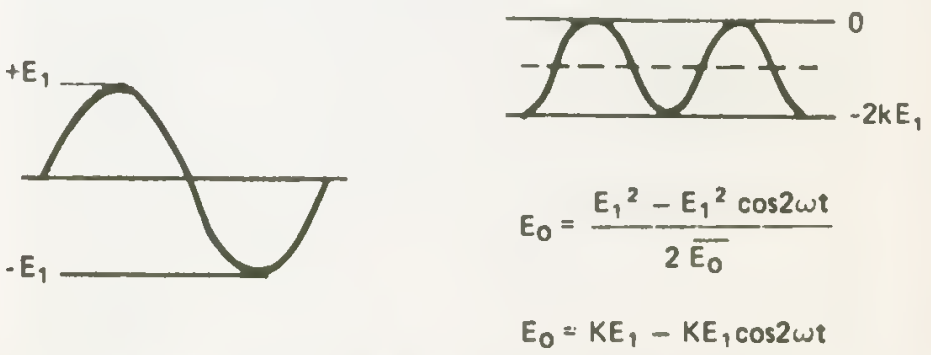


Fig. 23-3. Frequency doubler with linear amplitude response (AD).

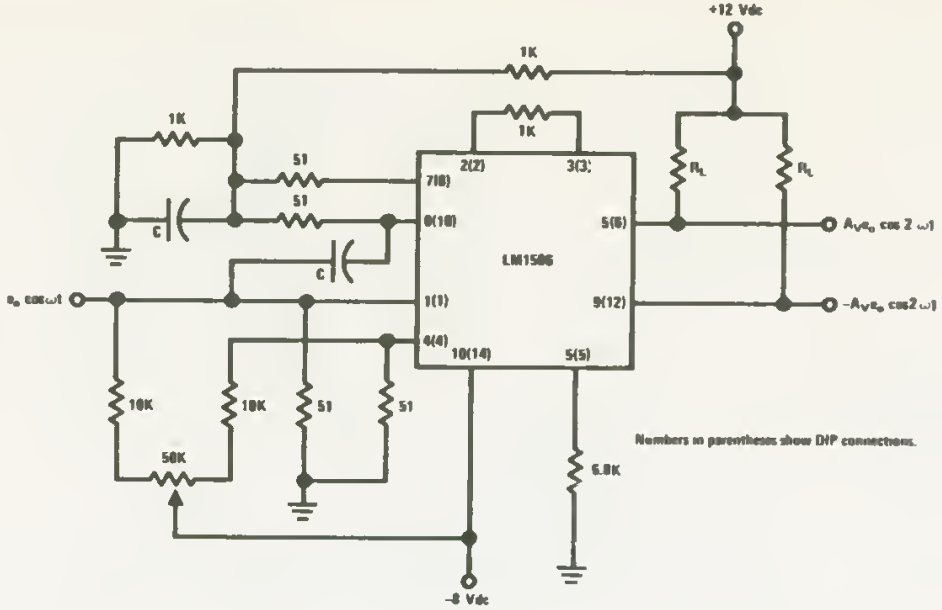


Fig. 23-4. Broadband frequency doubler (NS).

The frequency doubler circuit shown will double low-level signals with low distortion. The value of C should be chosen for low reactance at the operating frequency.

Signal level at the carrier input must be less than 25 mV peak to maintain operation in the linear region of the switching differential amplifier. Levels to 50 mV peak may be used with some distortion of the output waveform. If a larger input signal is available a resistive divider may be used at the carrier input, with full signal applied to the signal input.

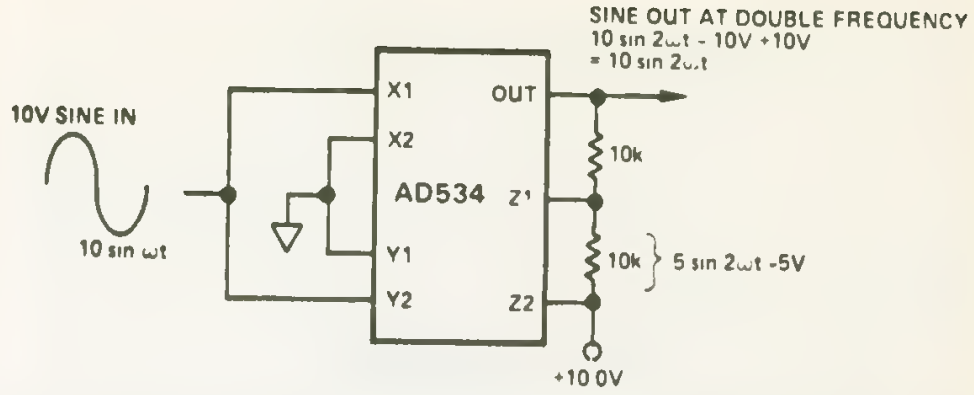


Fig. 23-5. Frequency doubler. This circuit accepts a sinusoidal signal with a 10-volt amplitude and produces a double-frequency signal also having a 10-volt amplitude with no DC offset (AD).

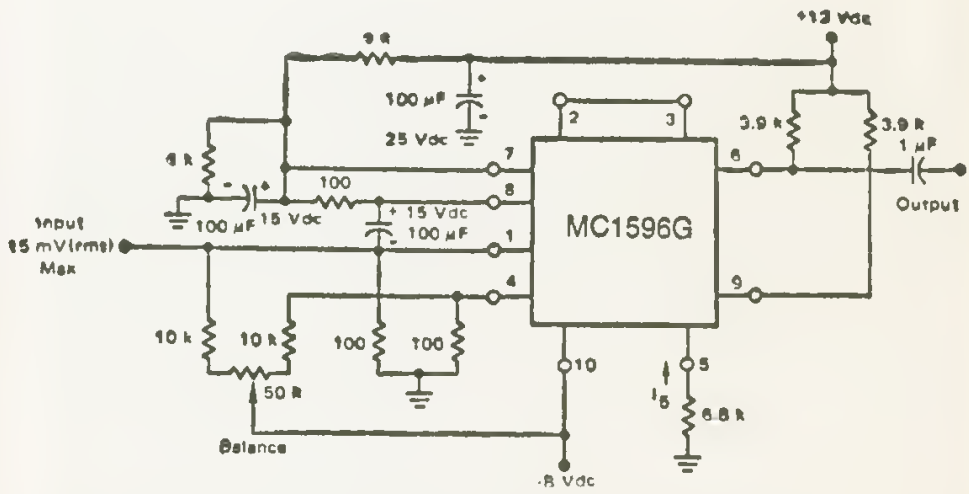


Fig. 23-6. Low-frequency doubler using an MC1596G. This circuit works well in the low-frequency and audio range below 1 MHz (M).

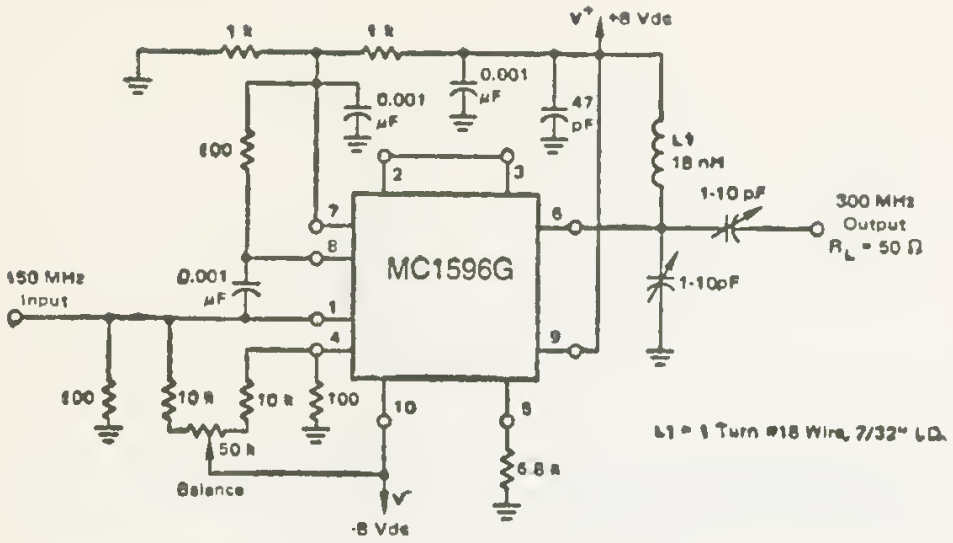


Fig. 23-7. A 150-MHz to 300-MHz frequency doubler using an MC1596G. Spurious outputs are 20 dB below the desired output (M).