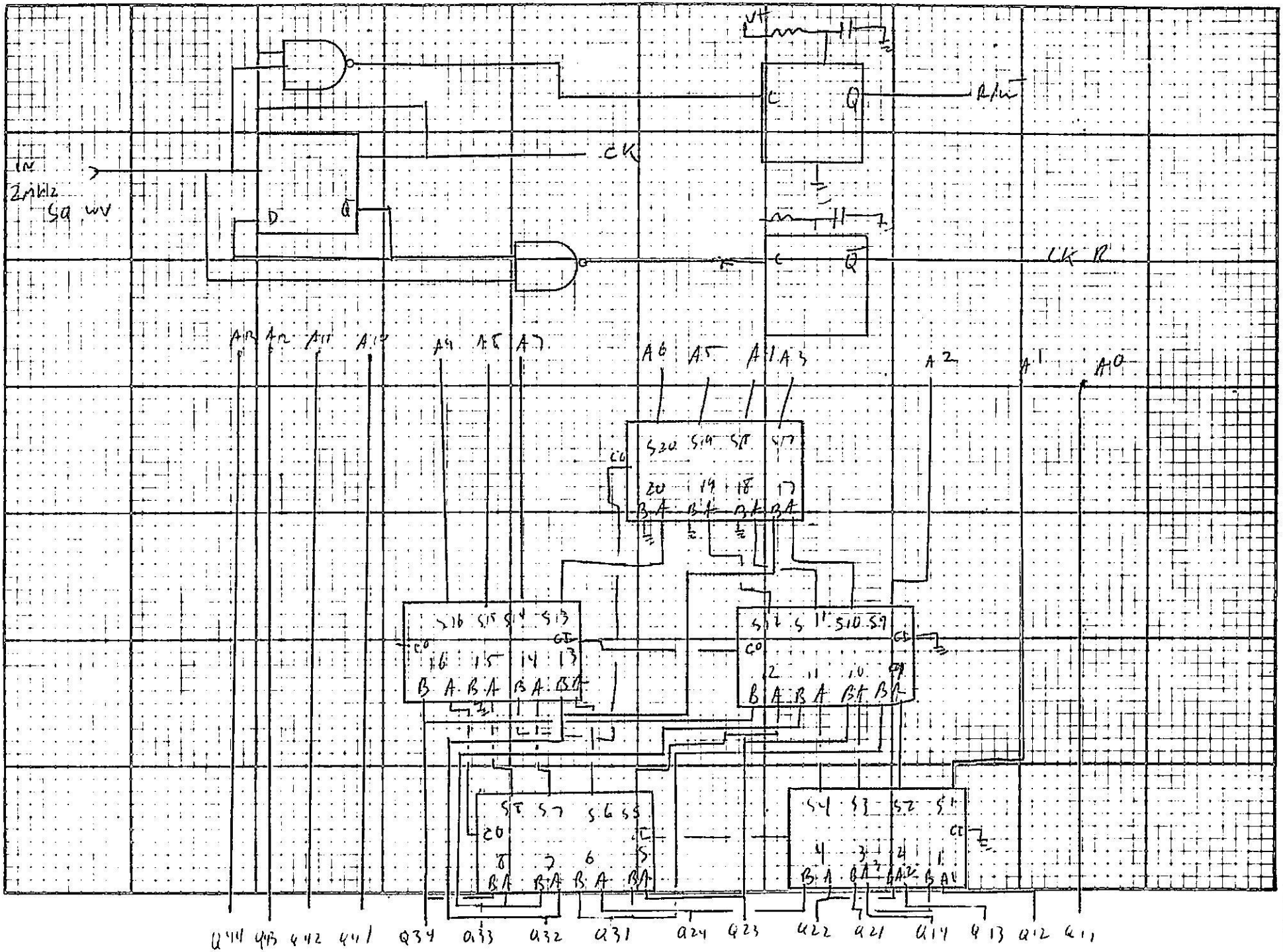

IN
2MHz
5Q WV
CK
D
Q
C
Q
CK R
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
S20 S19 S18 S17
20 19 18 17
B A B A B A B A
CO
S16 S15 S14 S13
16 15 14 13
S12 S11 S10 S9
12 11 10 9
S8 S7 S6 S5
8 7 6 5
S4 S3 S2 S1
4 3 2 1
CI
Q44 Q43 Q42 Q41 Q34 Q33 Q32 Q31 Q24 Q23 Q22 Q21 Q14 Q13 Q12 Q11

RAMs lengthen output delays

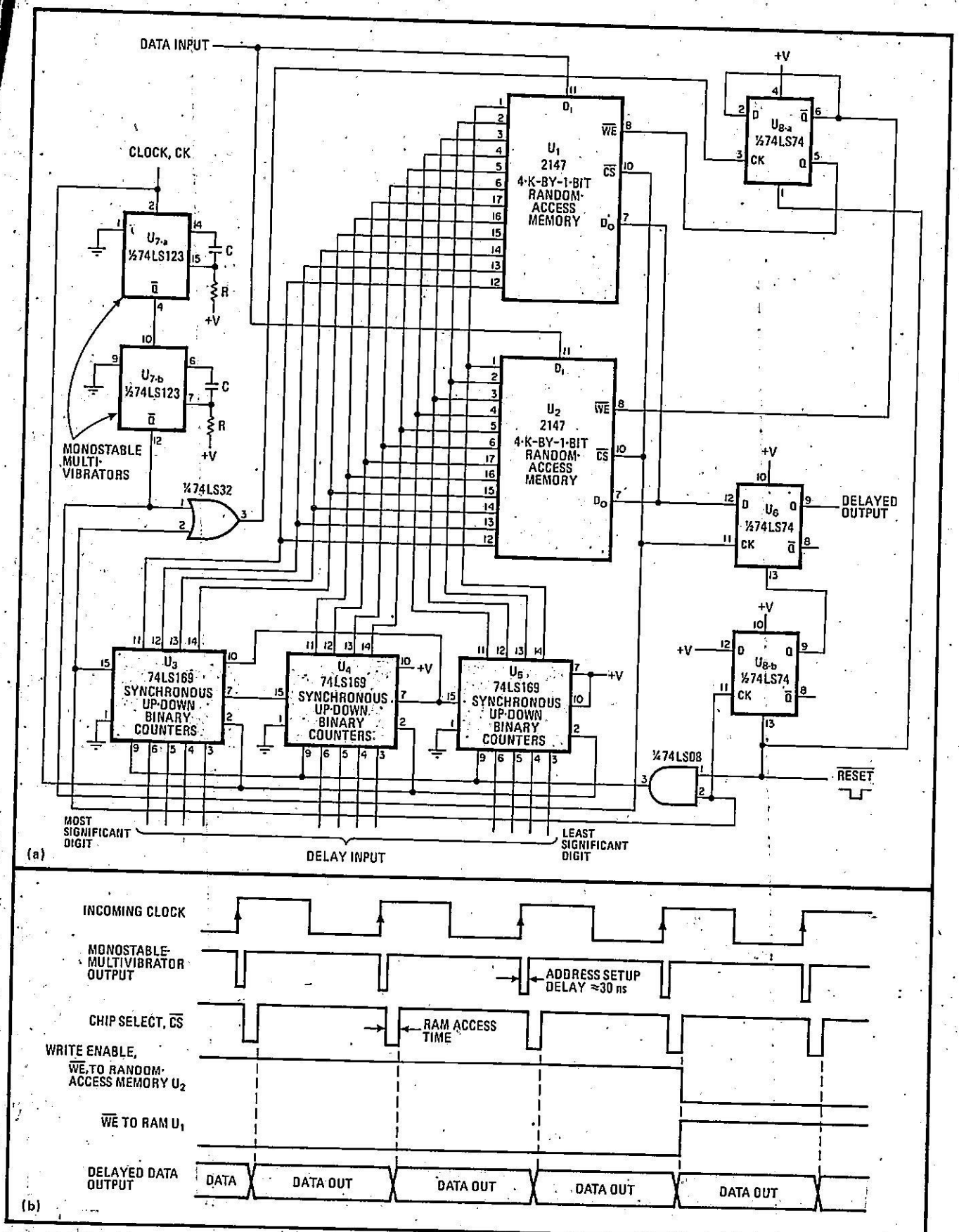
by Vittal Rao
ISRO Satellite Center, Peenya, Bangalore, India

Though output signals may be delayed slightly with a simple shift register, delays of longer duration require a disproportionately and often prohibitively larger number of such devices. However, this design uses a pair of random-access memories and a handful of integrated circuits to program a precise and accurate delay of up to 4,096 times the input clock pulse period into input data. The delay may be lengthened by using more counters and replacing the 4-K RAM with an 8-K RAM.

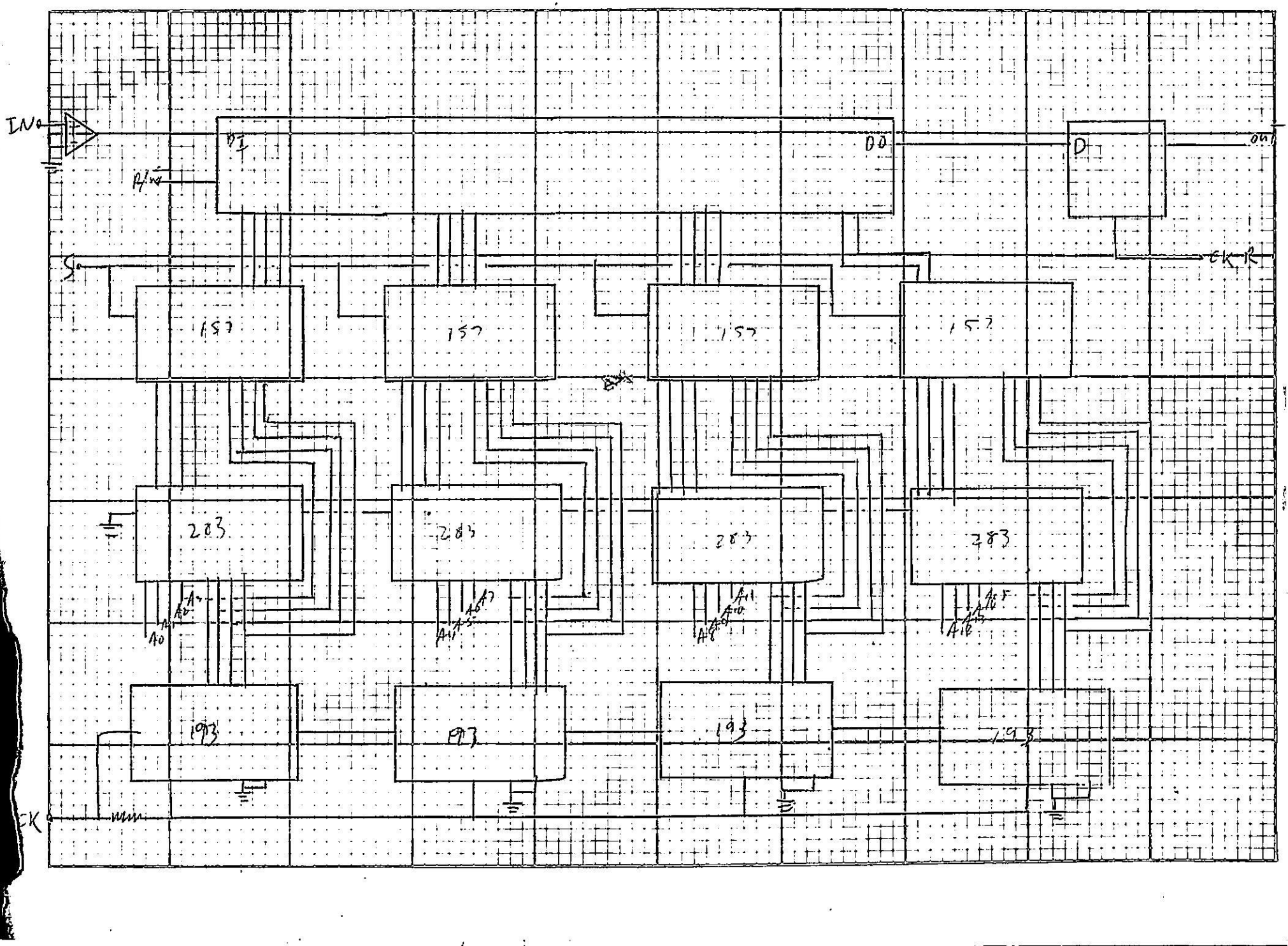
The desired time delay introduced by the circuit (a) is given by $T_d = N \times T$, where N is the multiplier number set by the RAM's delay input and T is the period of the input clock. The delay input is loaded into the address generator comprising synchronous down counters U_3 through U_5. For every incoming clock pulse (b), the counters decrement and generate an address for the data that is written.

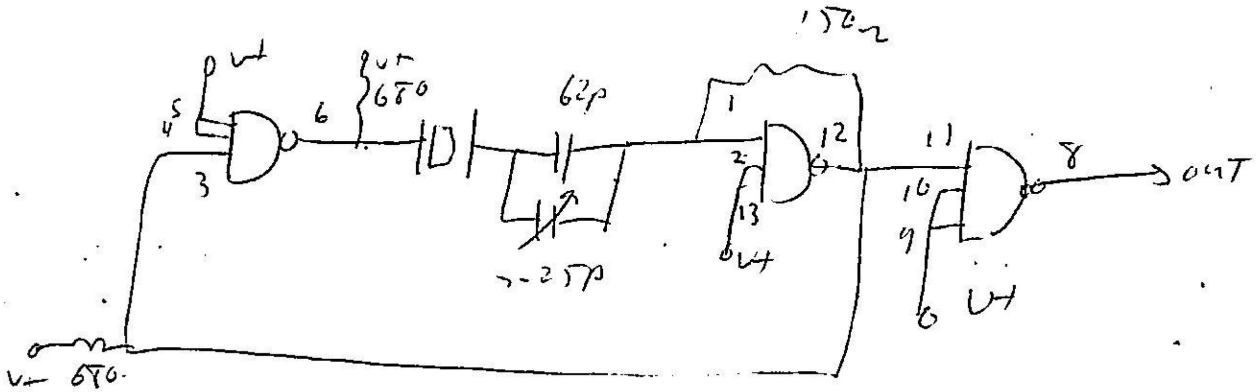
All incoming data that is written into RAM U_1 is simultaneously read from RAM U_2. This operation continues until the counters reach 000, thereby introducing a delay that is proportional to delay-input number N. When the counters reach 000, the delay input is once again loaded into the counters automatically, and the incoming data is now written into U_2 and simultaneously read from U_1.

For this configuration, the maximum size of delay input N is 4,096 and is determined by the bit capacity of the memory used. The input N can be increased by using a higher-capacity RAM and more counters. □

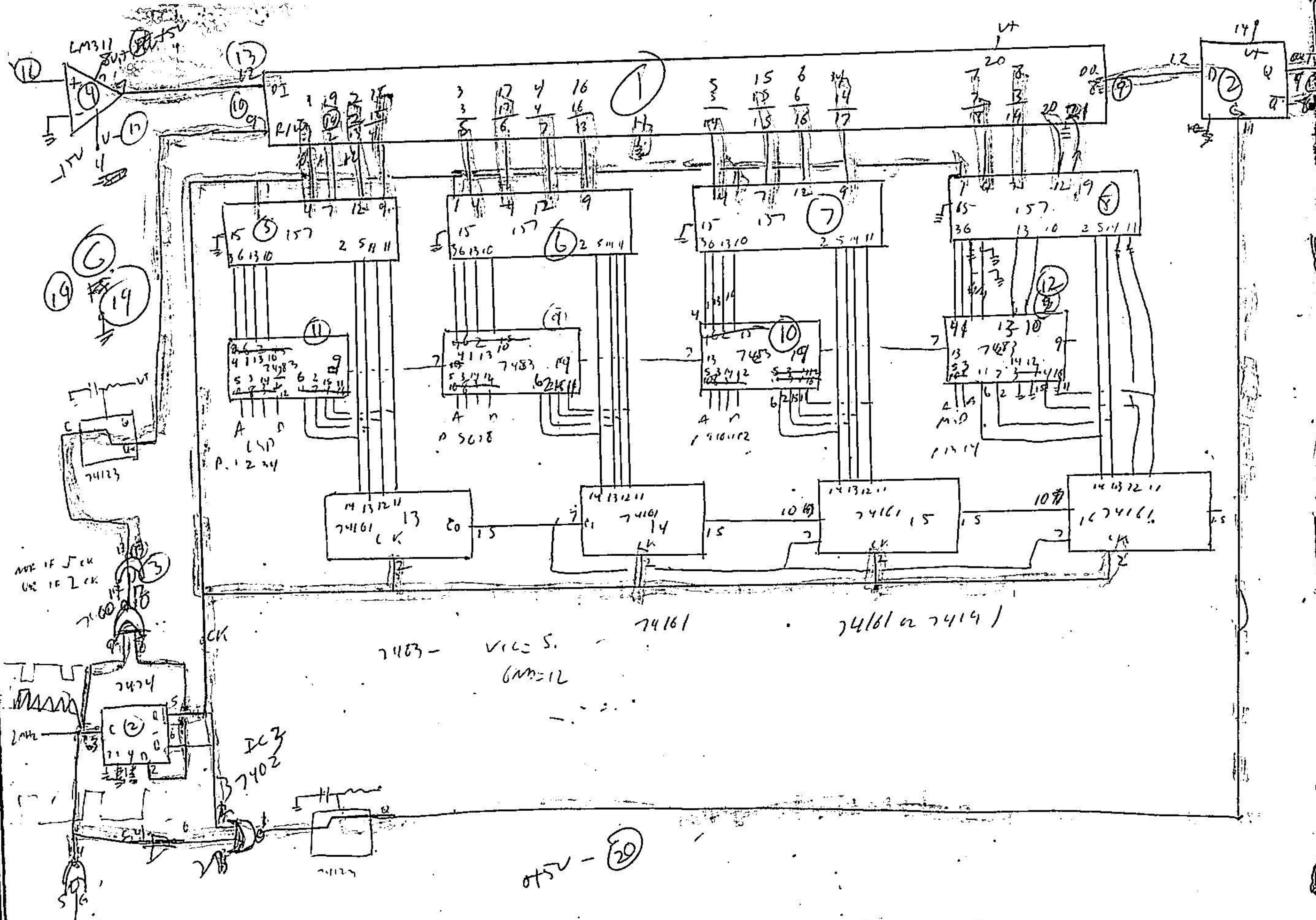


Delay. This digital circuit (a) delays incoming data by an amount proportional to delay input N, which is loaded into the address generator consisting of counters U_3 through U_5. The resultant delay introduced is given by $T_d = N \times T$, where T is the period of the clock input. Because a 4-K-by-1-bit RAM is used, the maximum value of N is 4,096. The timing diagram (b) shows waveforms for read, write, and latch operations.


IN
R/W
DO
D
out
CK R
157
157
157
157
283
283
283
283
193
193
193
193
CK



VS FM6RIV. ZIP



LM311
157
157
157
157
7483
7483
7483
74161
74161
74161
74123
7474
74123
IC3
7402
74161
7483 -
Vcc = 5.
GND = 12

b.c.d.-to-binary converter

The circuit described by Falko Kuhnke in October Circuit Ideas is unduly complicated. Conversion can be effected using just a pair of 4008 i.cs, rewriting

$$10X_{10}+X_1 \text{ as } 8X_{10}+2X_{10}+X_1.$$

Multiplication by eight and two in binary requires only shifting and this can be hard wired.

N. G. de Mattos-Shipley
London EC4

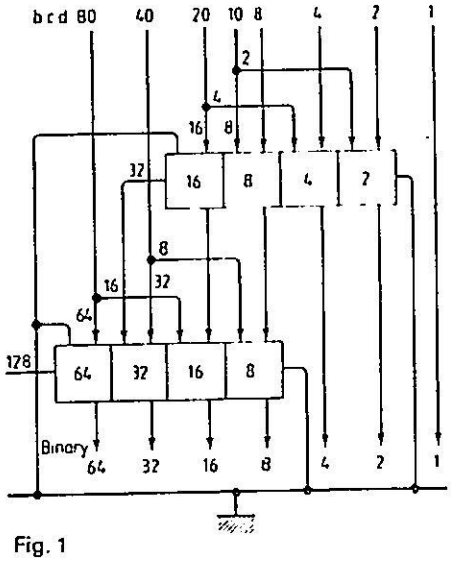


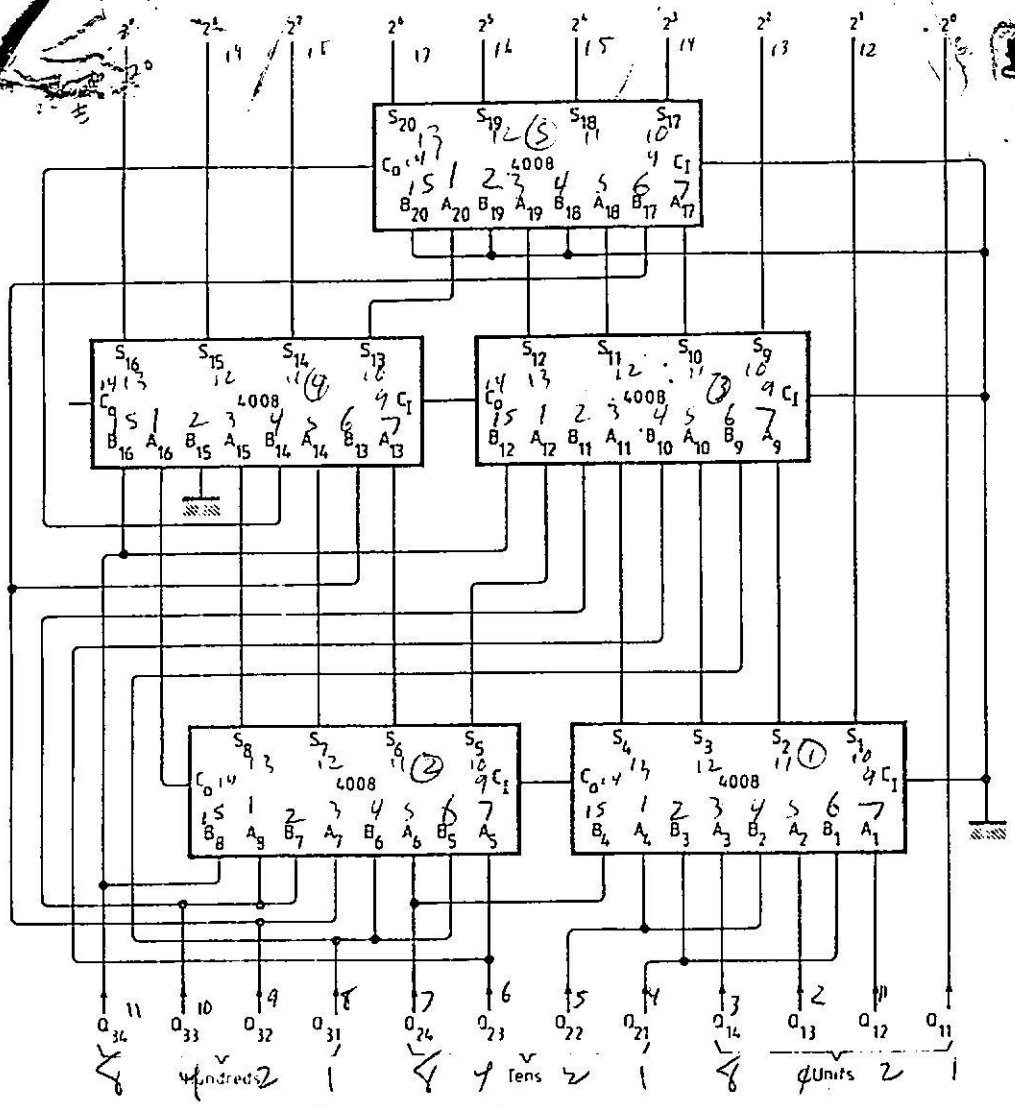
Fig. 1

The circuit described by F. Kuhnke can be simplified if we take into account that the b.c.d. numbers 10, 20, 40 and 80 may be split up into powers of 2, as 2+8, 4+16, 8+32, 16+64. If these values are added, together with the 1, 2, 4 and 8 inputs in a parallel adder, the output is a binary-weighted word with 64 as the highest value. The idea may be expanded to higher b.c.d. values, 100 to 800, 1000 to 8000, etc. as shown in my publication: The conversion of b.c.d. words into binary numbers", *Microelectronics Journal*, vol. 11, no. 2, pages 29 to 34.

For comparison, the conversion of the numbers 1 to 99 is shown in Fig. 1. Only two i.cs with four full adders (7483) each are needed.

C. van Holten
Technische Hogeschool, Delft

Binary output										b c d	
2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Value	Input
0	0	0	0	0	0	0	0	0	1	1	11
0	0	0	0	0	0	0	0	1	0	2	12
0	0	0	0	0	0	0	1	0	0	4	13
0	0	0	0	0	0	1	0	0	0	8	14
0	0	0	0	0	0	1	0	1	0	10	21
0	0	0	0	0	1	0	1	0	0	20	22
0	0	0	0	1	0	1	0	0	0	40	23
0	0	0	1	0	1	0	0	0	0	80	24
0	0	0	1	1	0	0	1	0	0	100	31
0	0	1	1	0	0	1	0	0	0	200	32
0	1	1	0	0	1	0	0	0	0	400	33
1	1	0	0	1	0	0	0	0	0	800	34



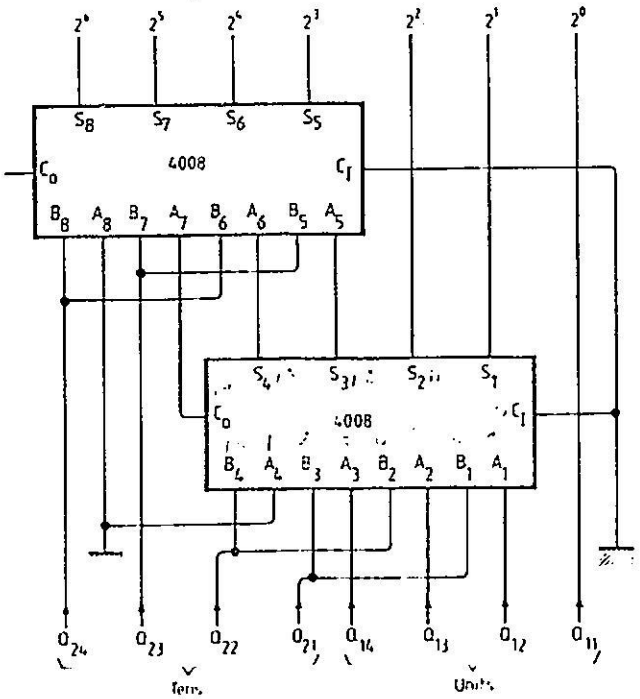


Fig. 2

The clue to the simplicity of Fig. 2. circuit is to be found in the table and the philosophy may be extended to derive a three decade converter.

The table shows the binary representation of the b.c.d. outputs from units, tens and hundreds counters. To obtain a binary representation of any decimal value in the range 000 to 999 it is only necessary to add the binary columns together of the appropriate rows, e.g. the binary representation of 647 may be obtained by adding the binary columns of rows Q_{11}, Q_{12}, Q_{13} (=7) to Q_{23} (=40) to Q_{32} and Q_{33} (=600). The maximum number of bits that need to be added together for a two-decade converter is three (see binary column 2^3). For a three-decade converter the maximum number is thus four (again, see binary column 2^3). Fig. 3 illustrates a three-decade converter using five four-bit full adder i.cs

A. J. Ewins
North Harrow

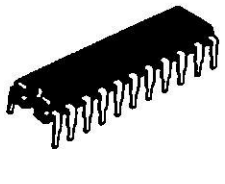
HM6287H Series

65536-Word × 1-Bit High Speed CMOS Static RAM

The Hitachi HM6287H is a high speed 64K static RAM organized as 64-kword × 1-bit. It realizes high speed access time (25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU. The HM6287H packaged in a 300-mil plastic DIP and SOJ, is available for high density mounting.

Low power version retains the data with battery back up.

HM6287HP Series



(DP-22NB)

HM6287HJP Series

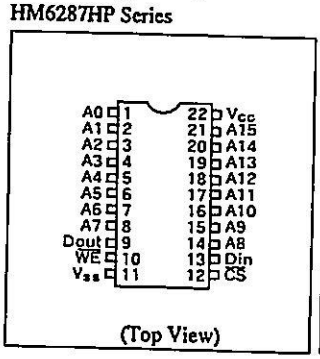
(CP-24D)

Features

- Single 5 V supply and high density 22-pin DIP and 24-pin SOJ
- High speed: Fast access time 25/35 ns (max)
- Low power
  - Operation: 300 mW (typ)
  - Standby: 100 µW (typ)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs

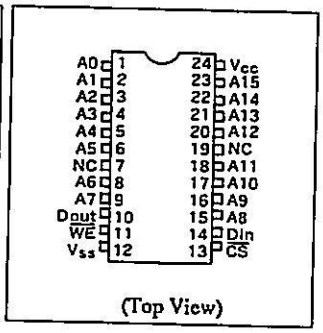
Pin Arrangement

HM6287HP Series



(Top View)

HM6287HJP Series



(Top View)

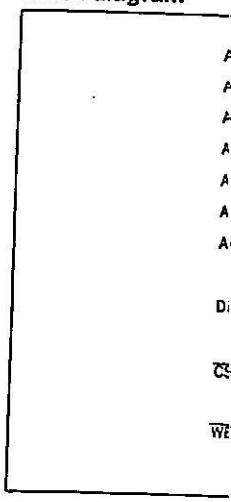
Pin Description

Pin Name	Function
A0 – A15	Address
Din	Input
Dout	Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Ordering Information

Type No.	Access Time	Package
HM6287HP-25	25 ns	300-mil 22-pin plastic DIP (DP-22NB)
HM6287HP-35	35 ns	
HM6287HLP-25	25 ns	
HM6287HLP-35	35 ns	
HM6287HJP-25	25 ns	300-mil 24-pin SOJ (CP-24D)
HM6287HJP-35	35 ns	
HM6287HLJP-25	25 ns	
HM6287HLJP-35	35 ns	

Block diagram



Function Table

$\overline{CS}$	$\overline{WE}$
H	×
L	H
L	L

Note: ×: H or L

Absolute Maximum R

Item
Voltage on any pin relati
Power dissipation
Operating temperature
Storage temperature
Storage temperature unde

Note: *1. VT min = –2.0 V f

Recommended DC Op

Item
Supply voltage
Input high (logic 1) voltag
Input low (logic 0) voltag

Note: *1. VIL min = –2.0 V f

HITACHI

Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

Static b.c.d.-to-binary converter

The circuit described by Falko Kuhnke in October Circuit Ideas is unduly complicated. Conversion can be effected using just a pair of 4008 i.cs, rewriting

$$10\bar{X}_{10}+X_1 \text{ as } 8X_{10}+2X_{10}+X_1.$$

Multiplication by eight and two in binary requires only shifting and this can be hard wired.

N. G. de Mattos-Shipley
London EC4

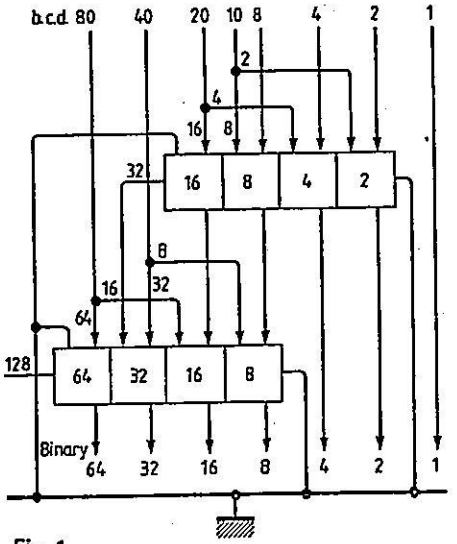


Fig. 1

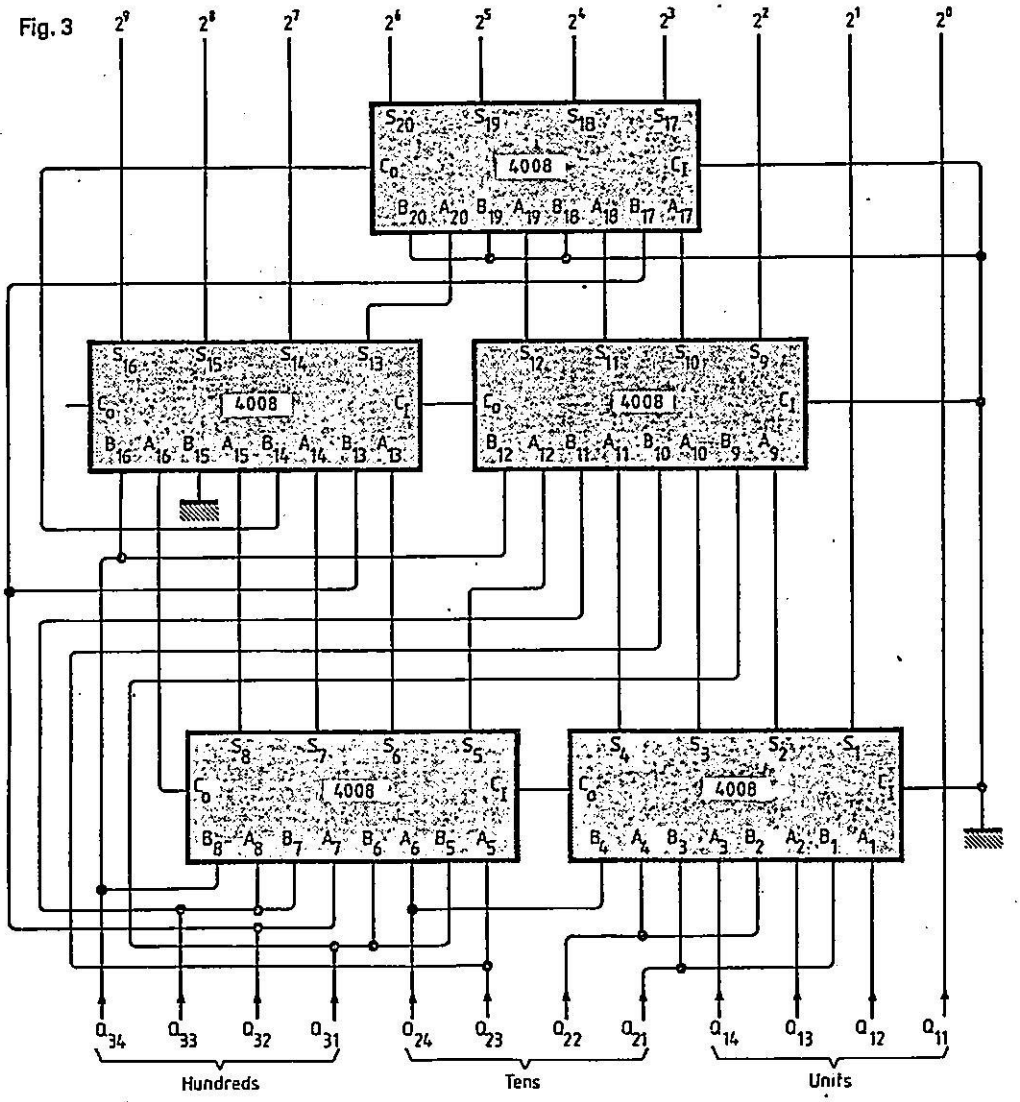
The circuit described by F. Kuhnke can be simplified if we take into account that the b.c.d. numbers 10, 20, 40 and 80 may be split up into powers of 2, as 2+8, 4+16, 8+32, 16+64. If these values are added, together with the 1, 2, 4 and 8 inputs in a parallel adder, the output is a binary-weighted word with 64 as the highest value. The idea may be expanded to higher b.c.d. values, 100 to 800, 1000 to 8000, etc. as shown in my publication: The coversion of b.c.d. words into binary numbers", *Microelectronics Journal*, vol. 11, no. 2, pages 29 to 34.

For comparison, the conversion of the numbers 1 to 99 is shown in Fig. 1. Only two i.cs with four full adders (7483) each are needed.

C. van Holten
Technische Hogeschool, Delft

Binary output										b.c.d.	
2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	Value	Input
0	0	0	0	0	0	0	0	0	1	1	11
0	0	0	0	0	0	0	0	1	0	2	12
0	0	0	0	0	0	0	1	0	0	4	13
0	0	0	0	0	0	1	0	0	0	8	14
0	0	0	0	0	0	1	0	1	0	10	21
0	0	0	0	0	1	0	1	0	0	20	22
0	0	0	0	1	0	1	0	0	0	40	23
0	0	0	1	0	1	0	0	0	0	80	24
0	0	0	1	1	0	0	1	0	0	100	31
0	0	1	1	0	0	1	0	0	0	200	32
0	1	1	0	0	1	0	0	0	0	400	33
1	1	0	0	1	0	0	0	0	0	800	34

Fig. 3



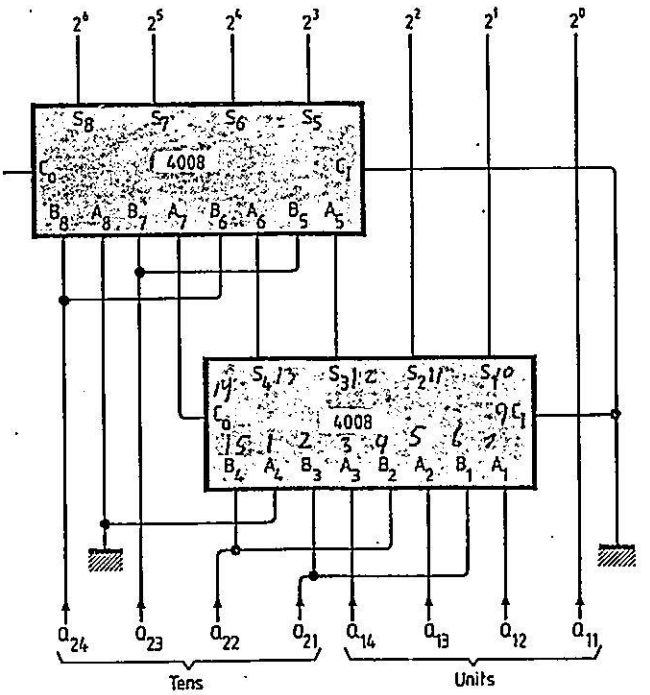


Fig. 2

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A. J. Ewins
North Harrow

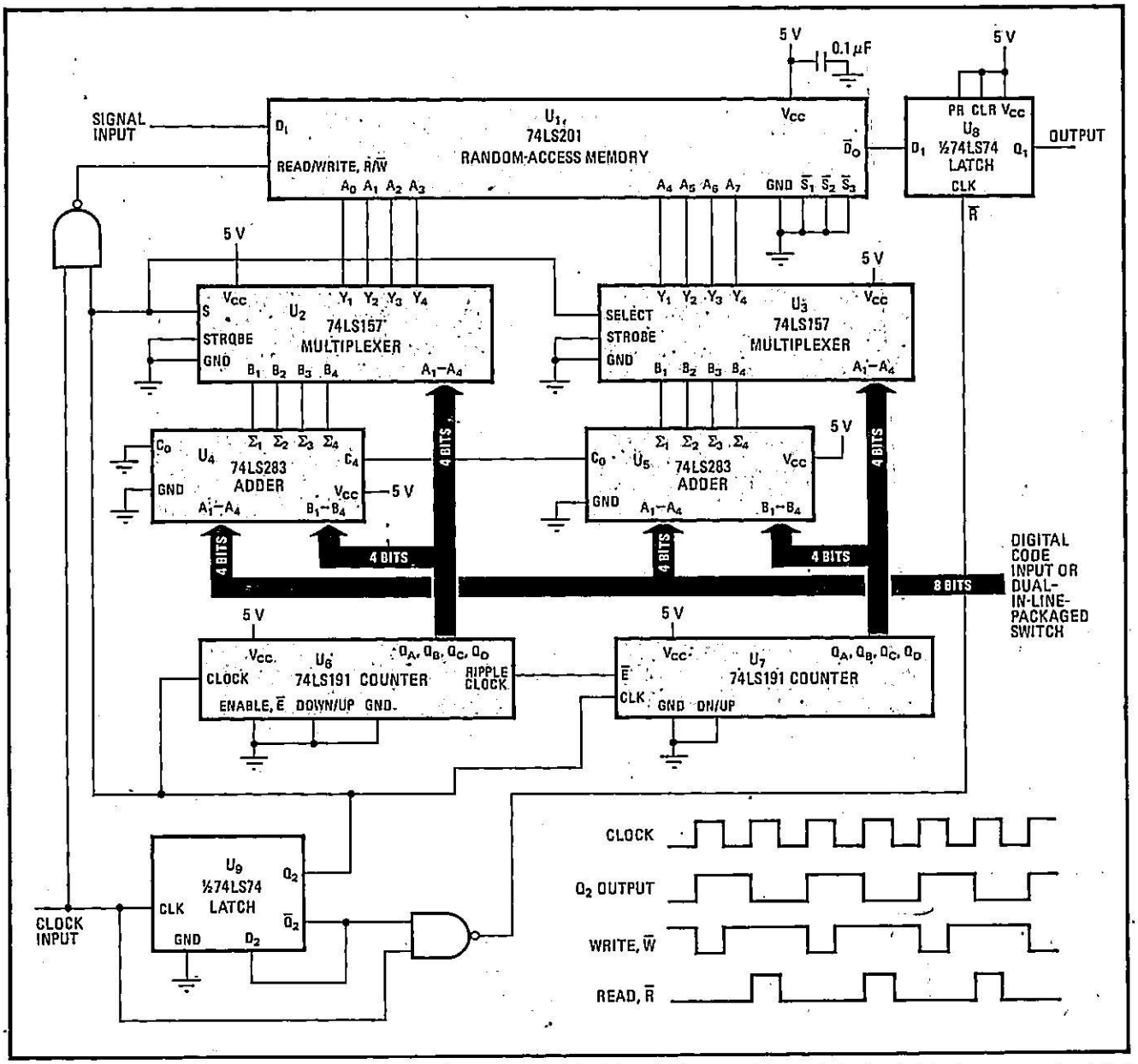
RAM makes programmable digital delay circuit

by Darius Vakili
Bayly Engineering, Ajax, Ont., Canada

For applications lacking in long shift registers and for which bipolar components are too expensive, this simple random-access-memory circuit will program the delay of digital signals precisely and accurately—and without needing varying clock frequencies. The RAM's ready availability and low cost add to the circuit's attractions, especially when high signal speeds are involved.

A digital input code programs the output delay of the signal. The input signal is written into the RAM U_1 at an address generated by synchronous up-down counters U_6 and U_7 and by a fixed input digital code set by the dual-in-line-packaged switch. The stored signal is available at the output when the write-enable input to the RAM is high. This data is read out of the RAM from a location that corresponds to the address generated by the counters only. Therefore, the signal read from the RAM is delayed by a time period equal to the DIP switch's displacement value multiplied by the period of the clock used for generating the address.

The input clock is divided by 2 by latch U_9. The Q_2 output of U_9 clocks address counters U_6 and U_7 and also the select inputs of multiplexers U_2 and U_3. The NAND gates generate the RAM's read and write inputs and also ensure the data is written into the RAM when the control input of U_2 and U_3 is high and read out when it is low. □



Programmed delay. Using random-access memory, this programmable-delay circuit accurately controls signal delay by means of a digital code generated by a DIP switch. Counters U_6 and U_7 generate the address for the RAM. U_9 provides the write and read inputs for the RAM.

Am2167

16,384 x 1 Static RAM

DISTINCTIVE CHARACTERISTICS

- High speed — access times as fast as 35ns maximum
- Automatic power down when deselected
- Low power dissipation
  - Am2167: 660mW active, 110mW power down
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL compatible interface levels
- No power-on current surge

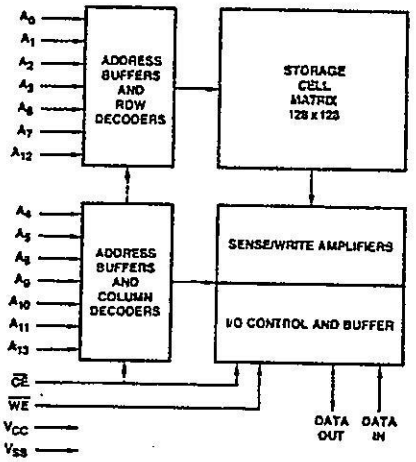
GENERAL DESCRIPTION

The Am2167 is a high performance, 16,384-bit, static, read/write, random access memory. It is organized as 16,384 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to six standard Schottky TTL loads or up to seven standard TTL loads.

Only a single +5 volt power supply is required. When deselected ($\overline{CE} \geq V_{IH}$), the Am2167 automatically enters a power-down mode which reduces power dissipation by 80%.

Data In and Data Out use separate pins and are the same polarity allowing them to be connected together for operation in a common data bus environment. Data Out is a three-state output allowing similar devices to be wire-OR'd together.

BLOCK DIAGRAM



BD000170

PRODUCT SELECTOR GUIDE

Part Number	Am2167-35	Am2167-45	Am2167-55	Am2167-70
Maximum Access Time (ns)	35	45	55	70
Maximum Active Current (mA)	120	120 (160 mil)	120 (160 mil)	120 (160 mil)
Maximum Standby Current (mA)	20	20 (30 mil)	20 (30 mil)	20 (30 mil)
Full Military Operating Range Version	No	Yes	Yes	Yes

03211D

Address De
External
A_0
A_1
A_2
A_3
A_4
A_5
A_6
A_7
A_8
A_9
A_{10}
A_{11}
A_{12}
A_{13}

Am2167-45 D M

Packa
D –
P –

Speed Selec
35 – 35ns
45 – 45ns

Device Type
16k x 1 SRAM

dard TTL loads or six Schottky TTL

erface levels
nt surge

power supply is required. When the Am2167 automatically enters a ich reduces power dissipation by

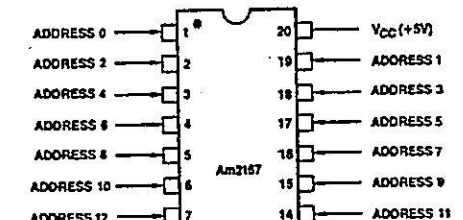
re separate pins and are the same be connected together for operation bus environment. Data Out is a ing similar devices to be wire-OR'd

67-55	Am2167-70
5	70
30 mil)	120 (160 mil)
) mil)	20 (30 mil)
es	Yes

03211D

CONNECTION DIAGRAM
Top View

D-20-1, P-20-1

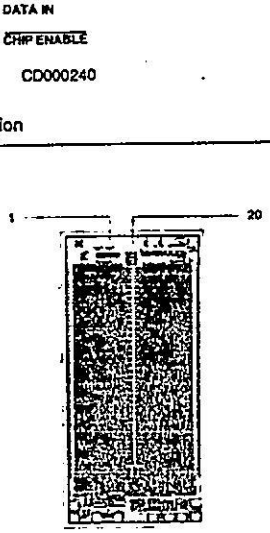


CD000240

Note: Pin 1 is marked for orientation

BIT MAP

Address Designators	
External	Internal
A_0	A_1
A_1	A_6
A_2	A_2
A_3	A_5
A_4	A_3
A_5	A_0
A_6	A_4
A_7	A_{13}
A_8	A_{10}
A_9	A_8
A_{10}	A_{11}
A_{11}	A_9
A_{12}	A_{12}
A_{13}	A_7



DIE SIZE: 0.121 x 0.249

Figure 3. Bit Mapping Information

ORDERING INFORMATION

Am2167-45 D M B

- B — Burn-in Option: B suffix denotes 160 hour burn-in.
- M — Temperature: C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D – 20-pin CERDIP; P – 20-pin plastic DIP
- 45 — Speed Select: 35 – 35ns; 45 – 45ns; 55 – 55ns; 70 – 70ns
- Am2167 — Device Type: 16k x 1 SRAM

Valid Combinations	
Am2167-35	PC, DC
Am2167-45	PC, DC DM, DMB
Am2167-55	PC, DC, DM, DMB
Am2167-70	PC, DC DM, DMB

03211D

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
Signal Voltages with
respect to ground ..... −3.0V to +7.0V
Power Description 1.0W
DC Output Current 10mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.5V to +5.5V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

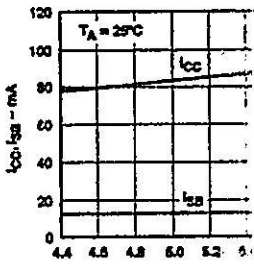
DC CHARACTERISTICS over operating range unless otherwise specified

Symbol	Parameter	Test Conditions		Am2167-35 Min	Am2167-35 Max	Am2167-45 Am2167-55 Am2167-70 Min	Am2167-45 Am2167-55 Am2167-70 Max	Units
I_{OH}	Output High Current	V_{OH} = 2.4V	V_{CC} = 4.5V	−4		−4		mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	COM'L	15		16		mA
			MIL	12		12		
V_{IH}	Input High Voltage			2.0	6.0	2.0	6.0	Volts
V_{IL}	Input Low Voltage			−3.0	0.8	−3.0	0.8	Volts
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$			10		10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC} Output Disabled		−50	50	−50	50	µA
C_I	Input Capacitance	Test Frequency = 1.0 MHz, T_A = 25°C, All pins at 0V, V_{CC} = 5V			5		5	pF
C_O	Output Capacitance				6		6	
I_{CC}	V_{CC} Operating Supply Current	Max V_{CC}, CE ≤ V_{IL} Output Open	COM'L		120		120	mA
			MIL		N/A		160	
I_{SB}	Automatic CE Power Down Current	MAX V_{CC}, (CE ≥ V_{IH}) (Note 3)	COM'L		20		20	mA
			MIL		N/A		30	

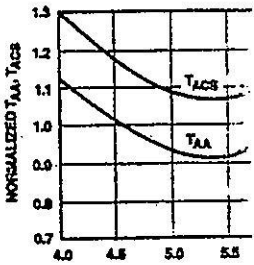
Notes:

1. Test conditions assume signal transition times of 5ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30pF load capacitance. Output timing reference is 1.5V.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power up. Otherwise I_{SB} will exceed values given.
4. The operating ambient temperature range is guaranteed with transverse air flow of 400 linear feet per minute.
5. The device must be selected during the previous cycle. Otherwise t_{AA} and t_{RC} are equivalent to t_{ACS}.
6. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for all devices. Transition is measured ±500mV from steady state voltage with load specified in Figure 2 for t_{HZ}, t_{LZ}, t_{OW} and t_{WZ}.
7. $\overline{WE}$ is high for read cycle.
8. Address valid prior to or coincident with $\overline{CE}$ transition low.

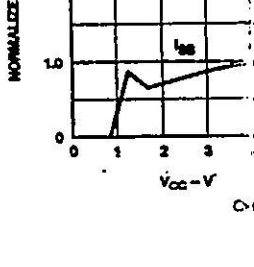
Supply Current
versus Supply Voltage



Normalized Access Ti
versus Supply Voltag



Typical Power-On Cur
versus Power Supp



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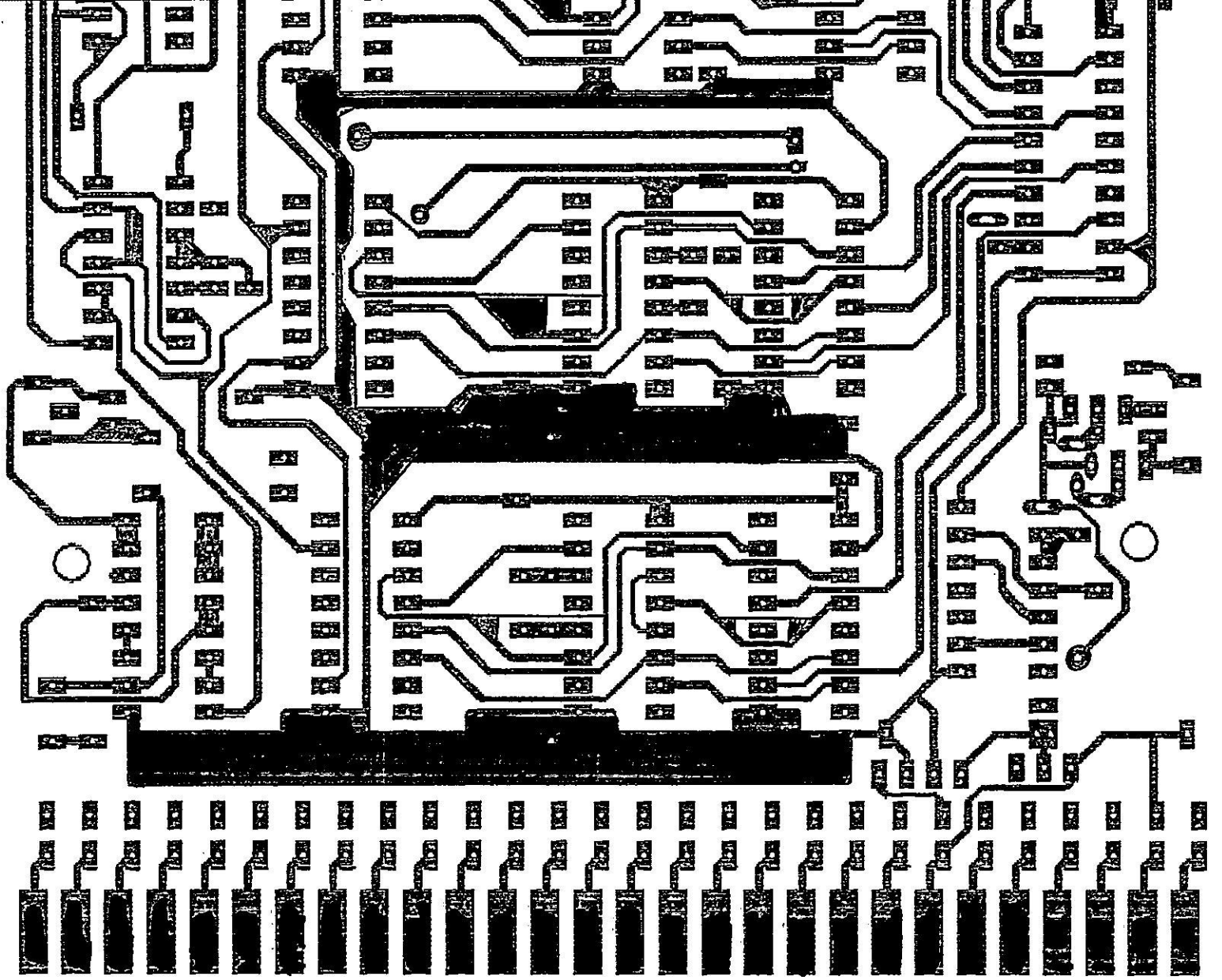


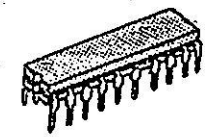
HM6167,HM6167-6,HM6167-8, HM6167P,HM6167P-6,HM6167P-8

16384-word×1-bit High Speed Static CMOS RAM

■FEATURES

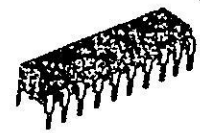
- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time — 70ns/85ns/100ns
- Low Power Stand-by and Low Power Operation
  Stand-by 25mW Typ. and Operating 150mW Typ.
- Completely Static Memory . . . . . No Clock nor Refresh Required
- Fully TTL Compatible — All Inputs and Output
- Separate Data Input and Output . . . . . Three State Output
- Pin-Out Compatible with Intel 2167 Series

HM6167, HM6167-6, HM6167-8



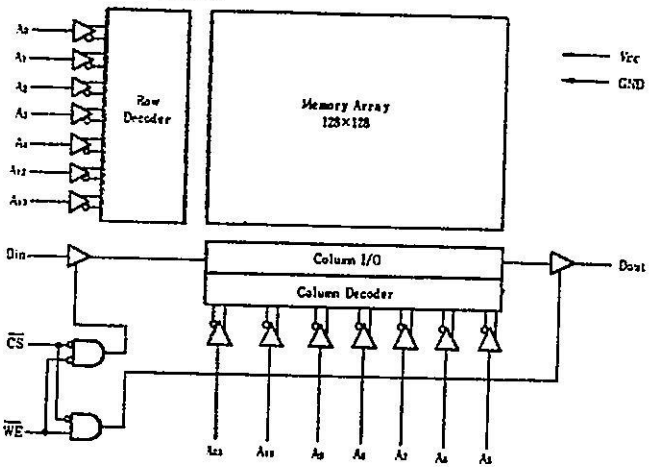
(DG-20)

HM6167P, HM6167P-6, HM6167P-8

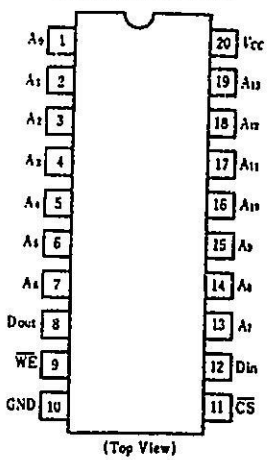


(DP-20)

■BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to GND	V_T	−0.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (Plastic)	T_{stg}	−55 to +125	°C
Storage Temperature (Ceramic)	T_{stg}	−65 to +150	°C
Storage Temperature**	$T_{stg(bias)}$	−10 to +85	°C

* Pulse width 20ns : −3.5V ** under bias

■RECOMMENDED DC OPERATING CONDITIONS

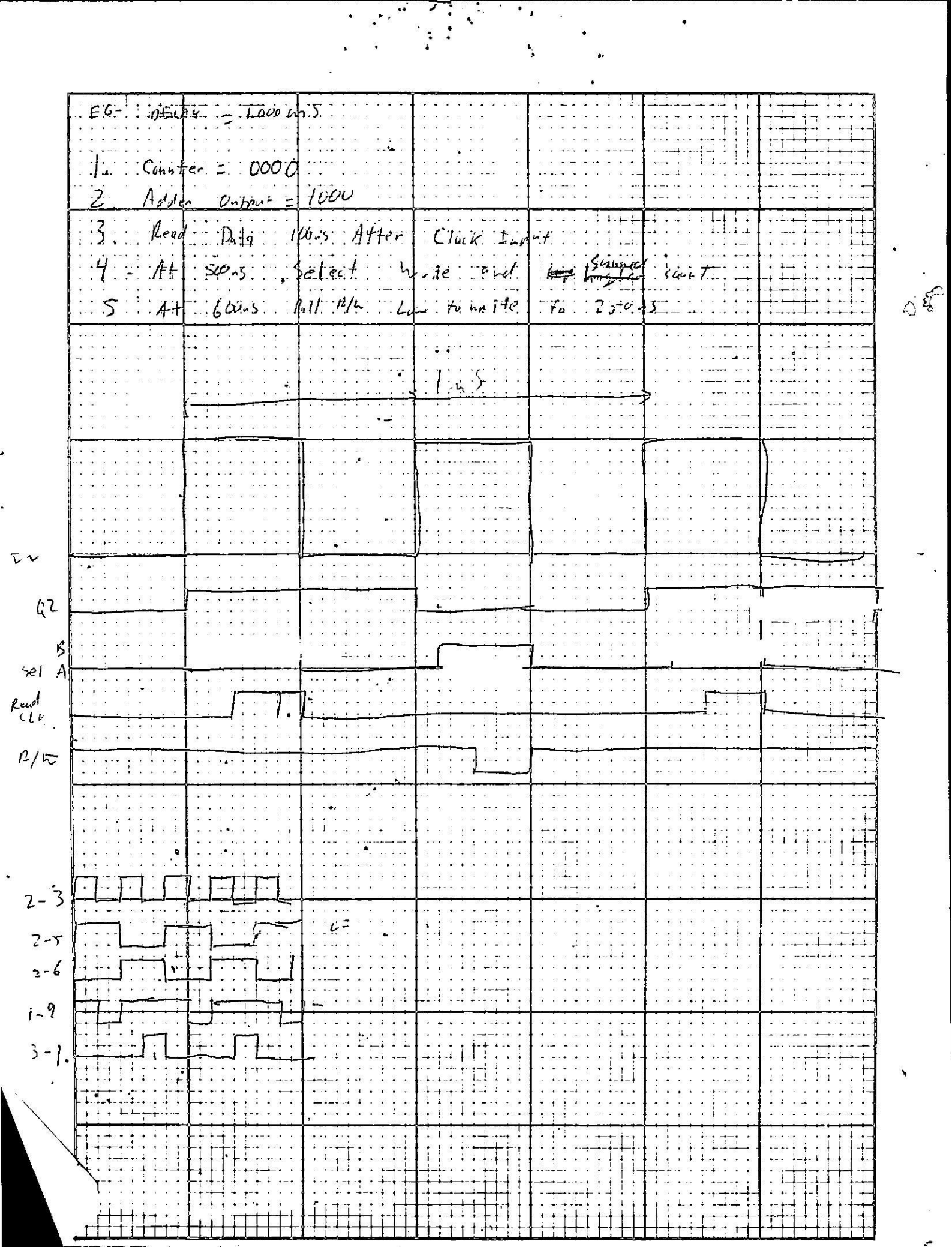
(0°C ≦ T_a ≦ 70°C)

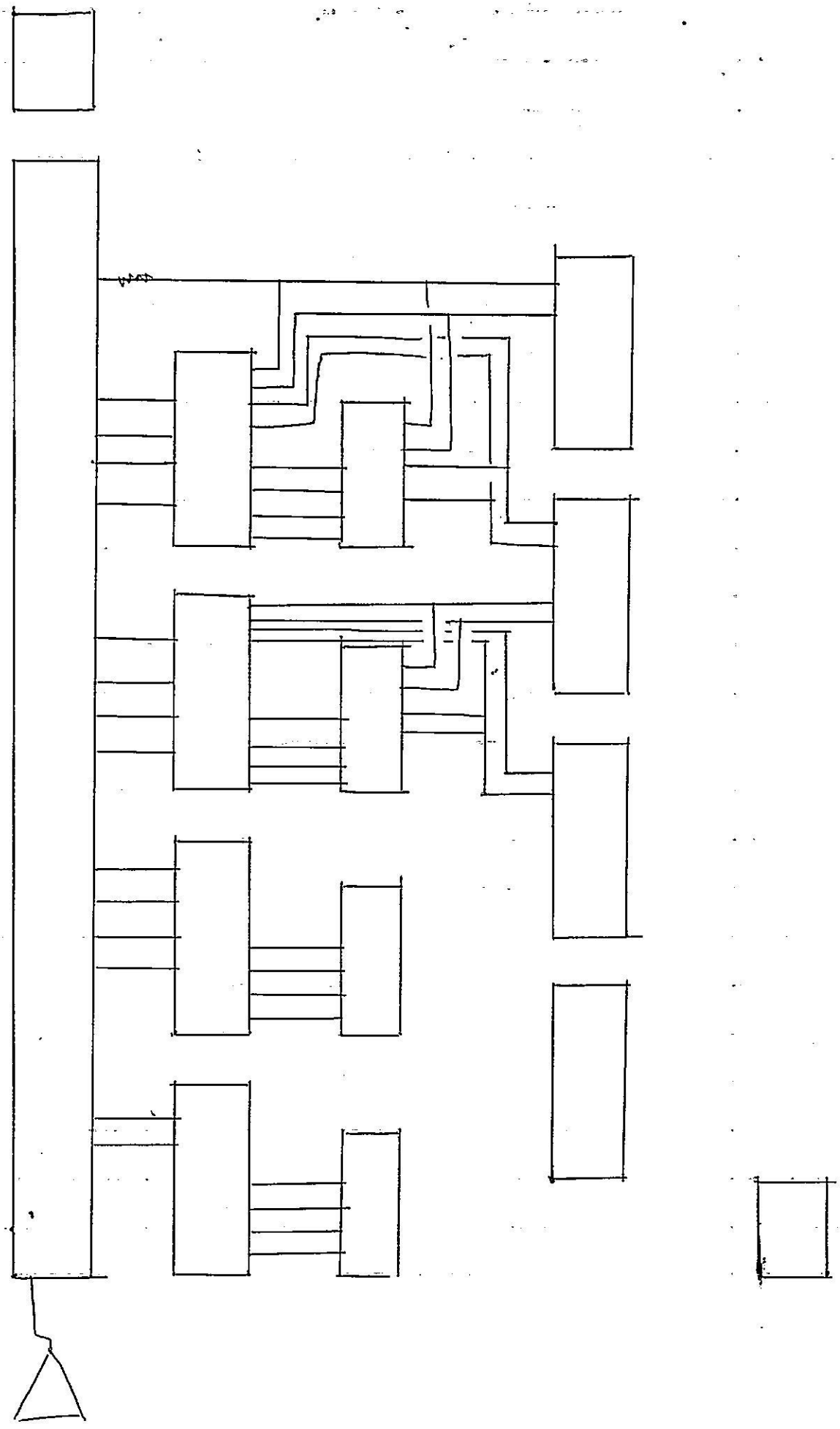
Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	−3.0*	—	0.8	V

* Pulse width 20ns, DC : V_{IL} min = −1.5V

E.G. Delay = 1000 m.S.

1. Counter = 0000
2. Adder Output = 1000
3. Read Data 100ns After Clock Input
4. At 50ns Select Write and Signed Count
5. At 60ns Roll R/W Low to write to 2-0-5





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