Low Power Data Conversion for Sensing Applications

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Abstract

Modern sensing applications often require high resolution conversion without compromising power consumption. In this Chapter, the maximum out-of-band quantization noise in delta-sigma converters is shown to play a key role in optimizing the performance of low power and high resolution delta-sigma analog-to-digital converters (ADCs). Two design examples will be highlighted that illustrate the use of these techniques to achieve high resolution conversion with low power consumption in deep submicron CMOS processes.

1. Introduction

Deep submicron CMOS processes often dictate different design styles and design approaches - particularly for analog circuit design [1,2]. As devices shrink in dimension, the tolerable signal swings reduce significantly. While for digital circuits this results in improved speed, transistor scaling can result in performance reductions for analog circuits. For example, to achieve the same ADC resolution when the signal swings are reduced, the noise floor must be reduced. This requires squaring the input capacitance when the voltage swing is halved for analog circuits limited by the kT/C noise. As a result, the power consumption is typically increased to achieve the same speed and resolution as the previous process generation.

Delta-sigma A/D converters are particularly interesting for a wide range of applications because they can be customized using digital signal processing. The also achieve high resolution with less stringent requirements on device matching, but typically at the expense of high oversampling ratios and therefore, lower bandwidths. This chapter will illustrate a critical parameter in the design of delta-sigma ADC converters that allows extending the performance of the converters to wideband applications while achieving high

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resolution. The basic background will first be given followed by two examples of recently fabricated converters.

2. A High Resolution Delta-sigma ADC with High OSR

The noise transfer function (NTF) of a delta-sigma modulator determines, in part, the overall resolution and the stability. A typical power spectral density of the quantization noise is shown in Fig. 1. The baseband boundary represents the input signal range for the converter and it is desirable to minimize the quantization noise in this band. The quantization noise amplitude increases for high frequencies and reaches a maximum at what is referred to as the maximum out-of-band quantization noise gain (Qmax). Prior work in delta-sigma ADCs supported limiting Qmax to ensure stable operation [5]. Further investigation has revealed that by optimizing this value, it is possible to increase the signal-to-noise-plus-distortion ratio of delta-sigma ADCs [6].

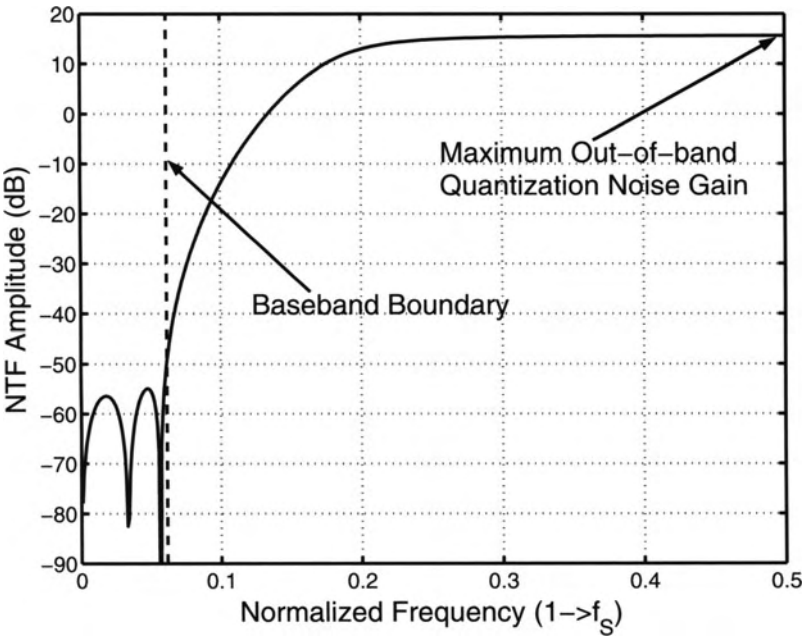

Fig. 1. Simulated power spectrum density of the quantization noise of a delta-sigma modulator.

For higher order A/D conversion, there are a number of high order delta-sigma architectures that are employed. One common implementation of a higher order delta-sigma modulator is the leapfrog architecture shown in Fig. 2. The interlocked feedback paths for the placement of zeros offer sufficient

insensitivity to the coefficient variations while providing higher-order loops for reduced signal-band tonal behavior. The complex transmission zeros in the quantization noise shaping characteristic are determined by the resonator feedback coefficients indicated by the *b's* in the figure. The quantization noise shaping characteristics and the stability properties are determined by both the *a* and *b* coefficients.

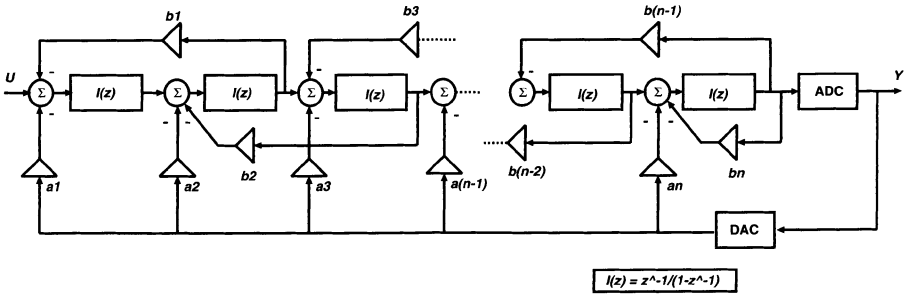

Fig. 2. Leapfrog architecture.

To determine the maximum SNR that can be achieved, a fourth-order delta-sigma modulator is simulated as a function of the maximum out of band quantization noise gain. As shown in Fig. 3, the maximum SNR is achieved for a Qmax value of approximately 1.7. Beyond this region, the modulator is unstable.

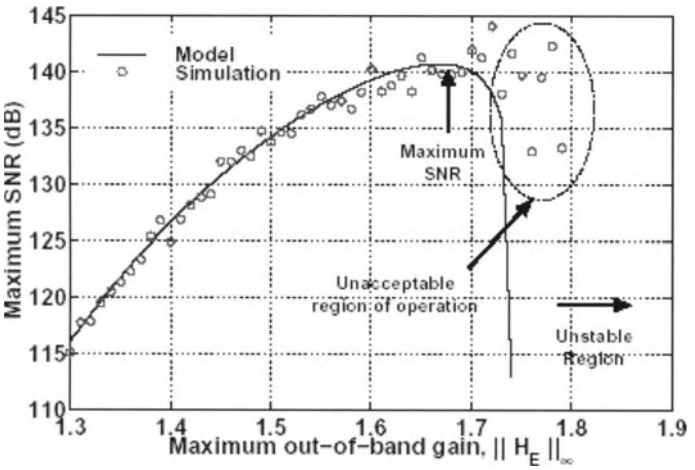

Fig. 3. Maximum SNR versus the maximum out of band quantization noise gain for a fourth-order modulator.

To optimize the design so that minimum power consumption is achieved, the integrators are designed to slew thus there are significantly less time constants required for settling. To illustrate the performance that can be achieved with this approach, two fourth-order delta-sigma ADCs are fabricated with the leapfrog architecture. A die microphotograph of two fourth-order delta-sigma ADCs is shown in Fig. 4 [8]. Both modulators are identical with the exception that one includes correlated double sampling at the input and the other does not. They are fabricated in a 0.6μm CMOS process operated from a single 3.0V power supply. The architecture as in Fig. 2 is used for this design and the Qmax is optimized to realize high resolution even with a low 3V CMOS process is employed. The reference signal is 1.0V and the maximum input signal voltage is 2.V single ended, peak-to-peak. The total power consumption is 22.8mW and the design consumes an area of 8.7mm x 2.8mm.

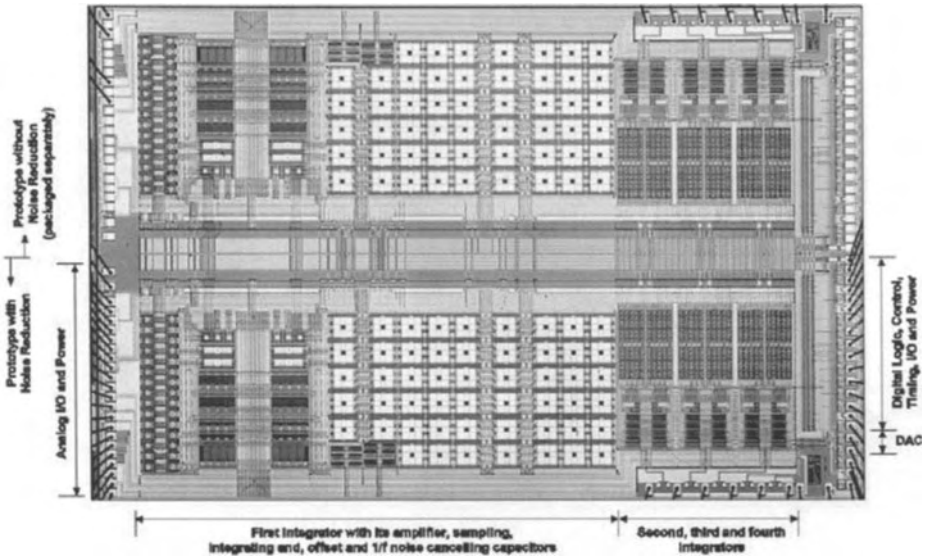

Fig. 4. Die microphotograph of two delta-sigma ADCs implemented in a 0.6μm 3V CMOS process.

The measured output spectrum from the two designs is shown in Fig. 5. The lower measurement is the design including correlated double sampling it shows a nearly 20dB lower noise floor. In this design, the noise floor is limited by KT/C noise while in the non-CDS design, the noise floor is limited by the 1/f noise. The maximum out-of-band quantization noise is shown to approximately the same for the two designs.

The measured SNR for the two designs is shown in Fig. 6. The modulators are clocked at 1.024MHz and a 50Hz input signal is applied. The results are plotted

for a bandwidth of 100Hz. The CDS modulator achieves an SNR of 22.4 bits in a 10Hz bandwidth and 19 bits in a 1kHz bandwidth.

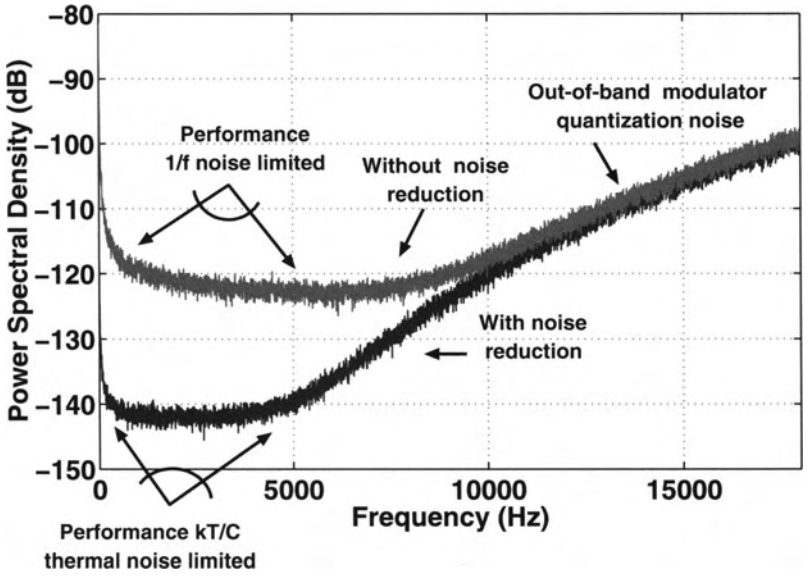

Fig. 5. Measured power spectral density of the delta-sigma modulators.

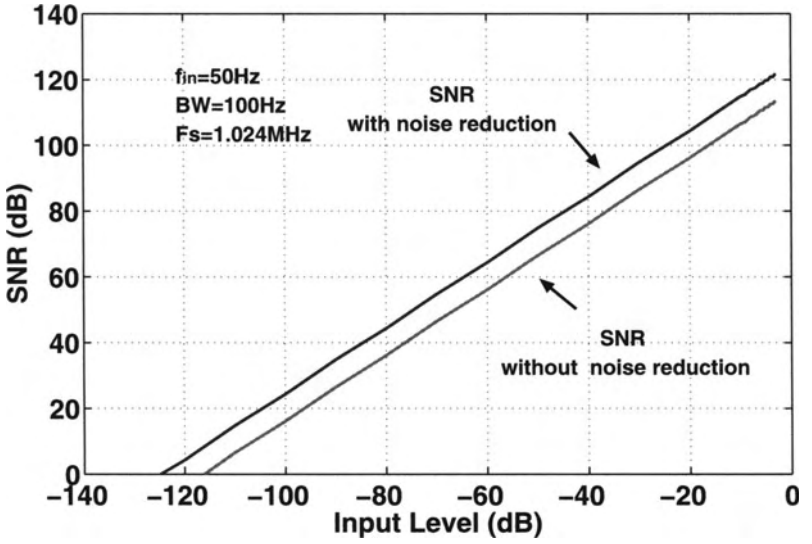

Fig. 6 Measured SNR versus input signal level for the two delta-sigma ADCs.

3. 14-bit Multi-path Delta-sigma Fabricated in a 0.18μm CMOS Process

The leapfrog architecture is suitable for delta-sigma modulator designs that use moderate to high oversampling ratios. However, for low oversampling ratios, it

limits the achievable SNDR as illustrated in Fig. 7. In this figure, the lower limit on the maximum out-of-band quantization noise gain is shown by the solid lines for various orders of delta-sigma modulators. Below this range, the modulators will produce tonal behavior. At the lower part of the graph, the value of the maximum out-of-band quantization noise gain is shown for a stable 5^{th}-order leapfrog modulator. Notice that for very low oversampling ratios, there is little or no room for developing a delta-sigma modulator that falls between these two ranges. However, at very high oversampling ratios (much greater than 20), this architecture is well suited to achieving high resolution with negligible distortion.

To determine the optimal maximum out of band quantization noise gain, the SNDR is simulated for 3^{rd}, 5^{th}, and 7^{th} order modulators. The maximum SNDR is shown when the maximum out of band quantization noise gain is increased from 1 to 7. Notice that for a 5^{th} order modulator, the SNDR can be increased by more than 25dB when Qmax is increased from 1 to 5. The primary challenge is to determine an architecture that can be implemented with higher Qmax values that does not have a high component spread.

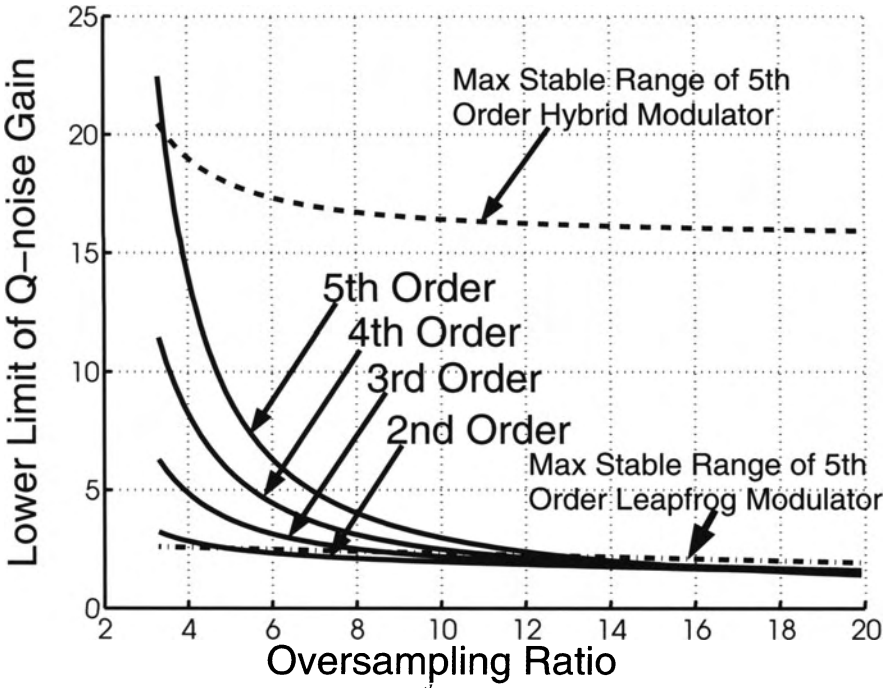

Fig. 7. Maximum stable range of a 5^{th}-order leapfrog and hybrid delta-sigma modulator

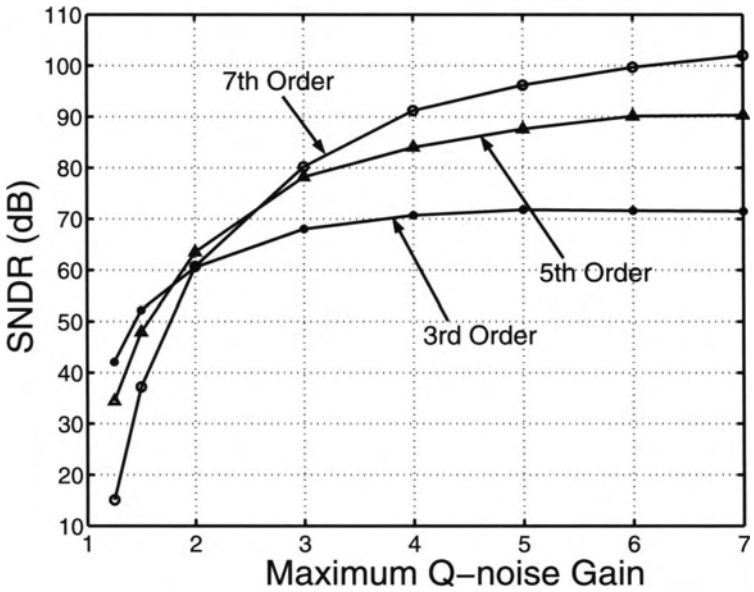

Fig. 8. Plot of SNDR versus the maximum out of band quantization noise gain.

The upper dashed lined in Fig. 7 indicates another architecture that is suitable for very low oversampling while achieving much higher SNDR. This architecture is referred to as a mult-path modulator and is shown in Fig. 9. This architecture consists of second-order IIR sections, shown in Fig. 10, embedded within the modulator. By embedding the second-order sections rather than cascading them, the requirements on the circuitry are relaxed. For example, in MASH architectures very high op amp gains are required, however, in this architecture, very low op amp gains are required to achieve high resolution. In the example below, it is shown that only 40dB of DC gain is required for a 14-bit ADC as compared to typically 80-90dB in MASH architectures. The architecture shown in Fig. 9 also includes a 4-bit ADC and DAC. Data weighted averaging is employed to attenuate the errors due to mismatches in the DAC.

An additional feature of this architecture is that there is a simple relationship between the noise transfer function pole/zero locations and the modulator coefficients. This is primarily due to the multipath nature of the architecture where each biquad is decoupled and not a complex high order set of equations. Another benefit of this structure is the coefficient spread is small. In the case of a 5^{th} order modulator with a 4-bit quantizer with 8X OSR, the coefficient spread is only 8 compared to more than 200 with a leapfrog architecture.

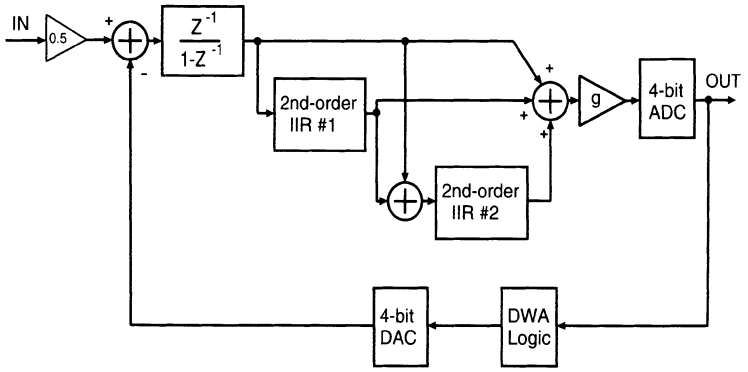

Fig. 9. Hybrid delta-sigma modulator architecture.

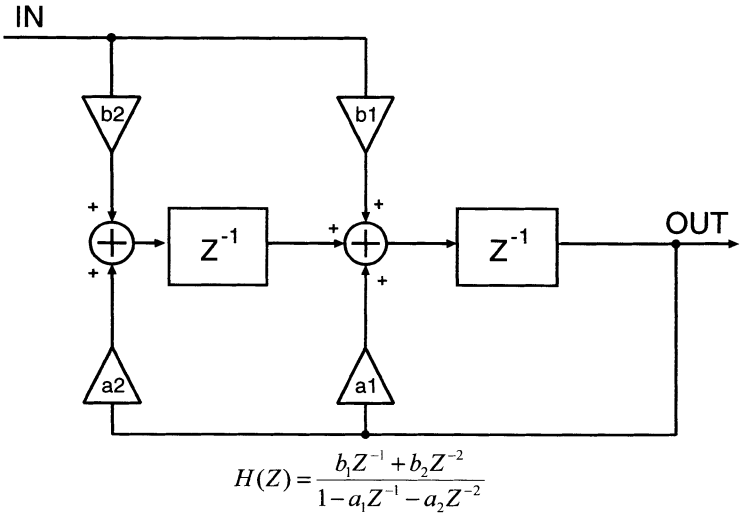

Fig. 10. IIR structure in Fig. 8.

To illustrate the applicability of this approach for low oversampling, a 14-bit converter with 8X oversampling is also shown. The die microphotograph is shown in Fig. 11 where the chip consumes 2.8mm^2. The modulator architecture is shown in Fig. 9 and it consists of a 17-level quantizer. The maximum out-of-band quantization noise gain of 6 is chosen to maximize the SNDR. The opamp DC gain is designed to be 43dB. This is particularly important since a 0.18μm CMOS process is used where it is difficult to achieve high opamp DC gains.

The converter achieves 83.9dB SNDR at 8X oversampling ratio and the measured results are shown in Fig. 12. The maximum input signal bandwidth is 2MHz for this implementation. Measurements also illustrate the performance

degradation when the data weighted averaging algorithm is not used for large input signals.

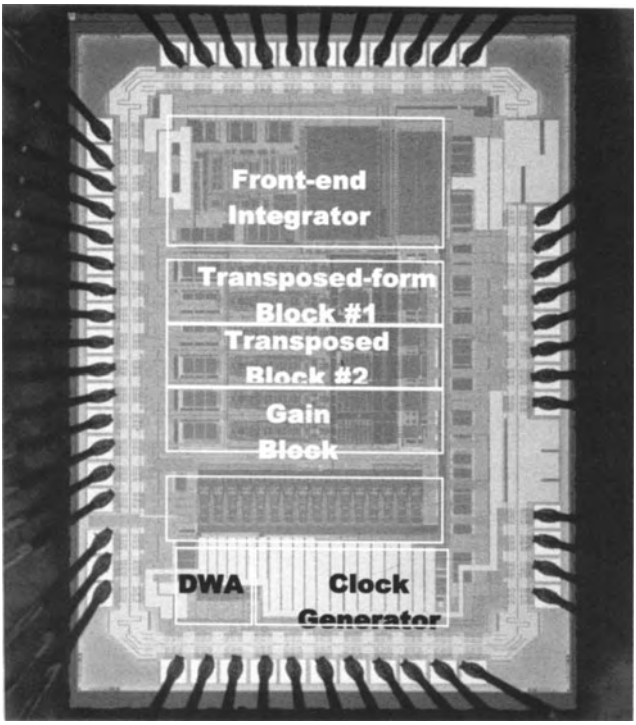

Fig. 11. Die microphotograph of the 14-bit delta-sigma ADC.

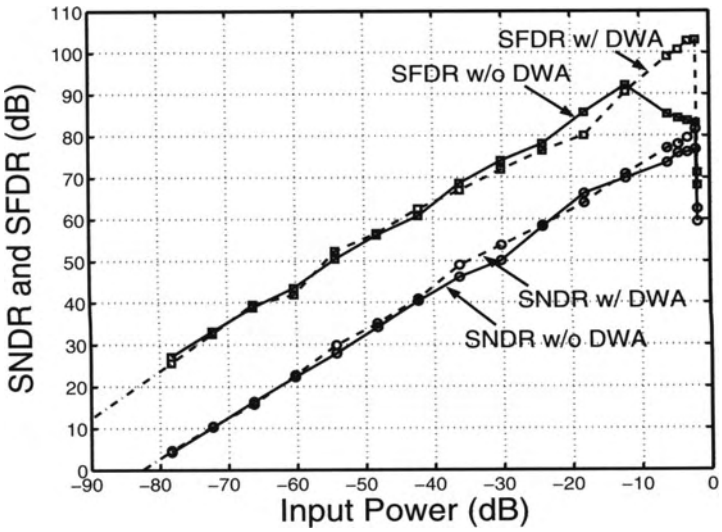

Fig. 12. SNDR and SFDR as a function of the input power for the 14-bit converter.

4. Conclusion

The importance of the maximum out-of-band quantization noise gain is stressed to achieve high resolution and/or high speed delta-sigma analog-to-digital conversion. Two design examples are given to illustrate the application of this approach. Both achieve very good performance with relaxed circuit requirements.

References

[1] J. Sauerbrey, T. Tille, D. Schmitt-Landsiedel, R. Thewes, "A 0.7-V MOSFET-only switched-opamp sigma-delta modulator in standard digital CMOS technology," IEEE J. Solid-State Circuits, vol. 37, no. 12, pp. 1662-1669, Dec 2002.

[2] S. Tadjpour, E. Cijvat, E. Hegazi, A.A. Abidi, "A 900-MHz dual-conversion low-IF GSM receiver in 0.35-μm CMOS," IEEE J. Solid-State Circuits, vol. 36, no. 12, pp. 1992-2002, Dec. 2001.

[3] P. Malcovati, C. Azeredo Leme, P. O'Leary, F. Maloberti, and H. Baltes, "Smart sensor interface with A/D conversion and programmable calibration," IEEE J. Solid-State Circuits, vol. 29, no. 8, pp. 963-966, Aug. 1994.

[4] C. Azeredo Leme and H. Baltes, "Multi-purpose interface for sensor systems fabricated by CMOS technology with post-processing," Sensors and Actuators A, vols 37-38, pp. 77-81, Oct. 1993.

[5] K.C. Chao, S. Nadeem, W.L. Lee, and C.G. Sodini, "A high order topology for interpolative modulators for oversampling A/D converters," IEEE Trans. Circuits and Systems II, vol. CAS-37, pp. 309-318, March 1990.

[6] R. Jiang and T.S. Fiez, "A 14-bit ΔΣ ADC with 8X OSR and 4-MHz conversion bandwidth in a 0.18μm CMOS Process," IEEE J. Solid-State Circuits, vol. 39, no. 1, pp. 63-74, Jan. 2004.

[7] R. Schreier, "The delta-sigma Toobox 5.1," ftp://next242.ece.orst.edu/pub/delsig.tar.Z ECE Department, Oregon State University, April 1998.