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DC-accurate, 32-bit DAC achieves 32-bit resolution

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Some applications, such as ADC testing and calibration, require a DAC with extremely good resolution, monotonicity, accuracy, and resolution. In these categories of performance, the circuit in **Figure 1** is hard to beat. Its typical specifications follow:

- Resolution=32 bits=3×10^{-10}=1.2 nV=192 dB.
- DNL (differential nonlinearity)=27 bits=400 nV=162 dB.
- INL (integral nonlinearity)=22 bits=1.6 µV=130 dB.
- Full-scale accuracy (untrimmed)=11 bits=±2.5 mV=66 dB.
- Zero accuracy=23 bits=±500 nV±10 nV/°C=140 dB.
- Ripple and noise=21 bits=2 µV p-p=128 dB.

The basis of the DAC's 32-bit resolution is the summing of two 16-bit PWM signals by analog switches S_1 and S_2 and precision resistor network R_2 through R_6. The DAC's monotonicity and DNL are theoretically infinite, and, in practice, the only limit is the 1-to-2^{16} ratio of R_2: ($R_6+R_5+R_{S2\text{-}ON}$) and R_3: ($R_6+R_4+R_{S2\text{-}ON}$). Typical accuracy of 0.1% resistors yields a DNL of approximately 0.1 ppm=27 bits.

The less-than-0.1Ω output impedance of the AD586 reference and the 130-dB CMR (common-mode rejection) of chopper-stabilized "zero-drift" amplifier A_1 mostly limit INL. R_7 suppresses a potential contribution from asymmetry in $R_{S1\text{-}ON}$, yielding the typical INL of approximately 0.3 ppm=22 bits.

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Zero-accuracy and output-noise specs are at the low-microvolt level because of the excellent specifications

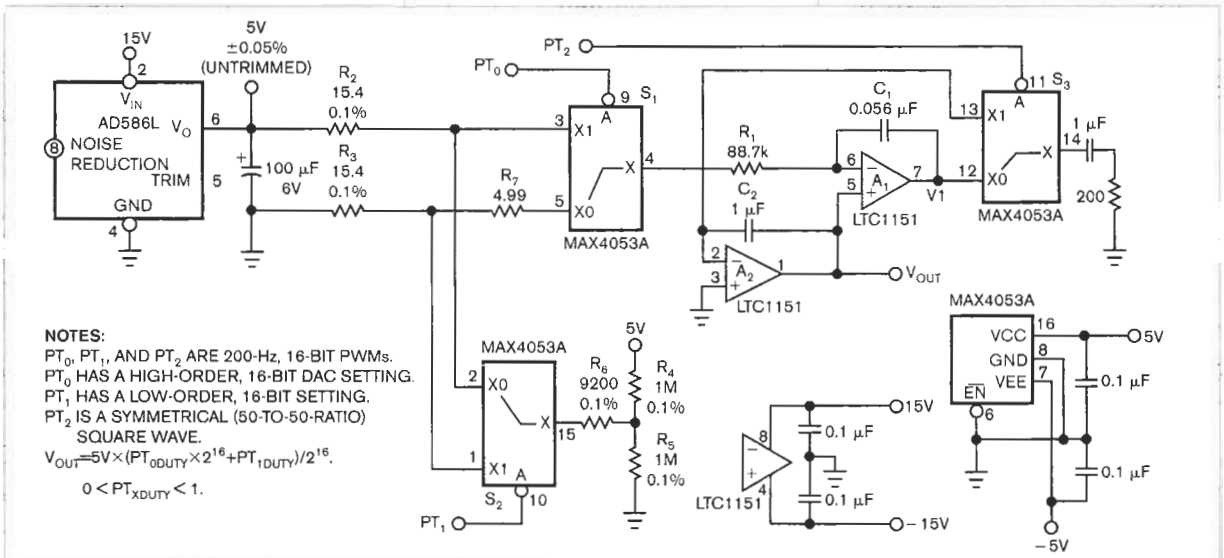

Figure 1 This DAC circuit sums two 16-bit PWM signals using precision analog switches to achieve 32-bit resolution.

of the LTC1151 A_1 and A_2 op amps and the charge-injection performance of the MAX4053A S_2: approximately 0.4 ppm, or 23 bits.

The precision of the AD586L 5V reference, which is ±500 ppm untrimmed, limits absolute accuracy. If your design requires greater accuracy, then you can use an Analog Devices (www.analog.com) simple trim circuit to further tweak it. There's nothing critical about the suggested 200-Hz PWM cycle. You need to change only R_1 and C_1 to accommodate any convenient frequency. How closely the R_1C_1 time constant matches the PWM-cycle time determines the settling time of the A_1-S_2-A_2 synchronous "zero-ripple" integrate-and-hold filter, and can be as fast as one cycle if the match is exact. EDN