ANALOG SIGNAL-HANDLING FOR HIGH SPEED AND ACCURACY
You're Paying for Accuracy in IC Converters;
Don't "Blow It" in the Analog Circuit Wiring

by A. Paul Brokaw

You've bought an IC a/d or d/a converter that's specified for 10-bit-and-better resolution and accuracy. Or, you've bought a current-ouput DAC with submicrosecond settling to 1/2 LSB. Much design effort, technological development, and process competence have been expended to solve the hardest part of your interface problem. But . . . you aren't out of the woods yet! Here are some of the issues that you will have to come to grips with to preserve speed, resolution, and accuracy:

1. If your DAC is a current-output type and you want voltage, the use of an op amp requires that you deal with the dynamic and steady-state signal-interfacing problems.

2. You will have to minimize interference introduced via common power-supply connections.

3. You will have to decide where "ground" should be and how to keep it there.

4. If "ground" is remote, you will have to couple to it without reduced accuracy or succumbing to interference.

5. If your analog signal is being converted by a successive-approximations converter, you may have to buffer the source from fast transients incidental to conversion.

To become aware of these potential problems is to have taken the first step towards solving them. Since all circuits and systems differ in important little ways, there are no "cook-book" solutions that can be blithely employed for satisfactory results in all cases. However, a little thought will go a long way towards solving them. The purpose of this Brief is to remind you of some of the things you should be thinking about.

DAC's AND OP AMPS — DYNAMIC PROBLEMS

A current-output DAC is usually connected to the summing point of an inverting op amp, and then the feedback loop is closed via the internal "span" resistor, R_F, as Figure 1 shows. The output impedance of the DAC can generally be treated as a parallel combination of resistance and capacitance. The shunt capacitance, C_O, combines with R_F to add a pole to the open-loop response, which may result in poor closed-loop response.
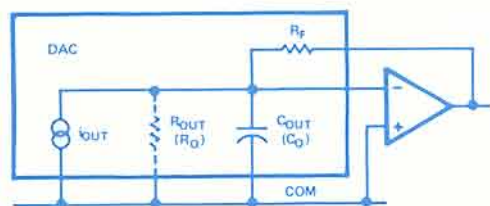

Figure 1. Equivalent circuit of current-output DAC.

Figure 2 shows how the open-loop amplitude and phase response might appear if the spurious pole due to C_O is below the undisturbed system-crossover frequency. Not only will the closed-loop bandwidth be reduced, but —more seriously— excess phase shift will be introduced. The extra phase shift reduces the system frequency stability margins and may cause ringing (and perhaps even oscillation).
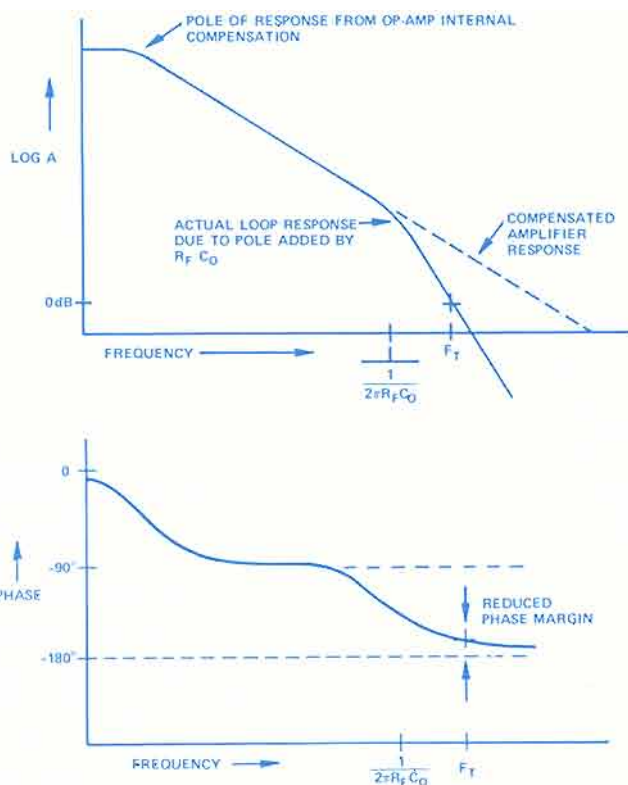

Figure 2. Amplitude and phase response of the circuit of Figure 1. The additional pole increases settling time by reducing bandwidth and increasing both overshoot and ringing.

As Figure 3a shows, the loop-stability margins can be restored by connecting a feedback capacitor, C_F, in parallel with the feedback resistor. This capacitance creates a zero in the open-loop transfer function, which can be adjusted to correct the phase margin. However, if R_{OUT} is very large (as is often the case with current-output DAC's), the large pole-zero mismatch remaining (Figure 3b) may result in slow settling.

Even with finite values of R_{OUT}, a small residual pole-zero mismatch (Figure 3c) may result in long-settling "tails"; the DAC output voltage may appear to settle quickly, but then it slowly changes —by a significant amount— to its final value, over the course of tens of microseconds, or even milliseconds.[1]

The residual mismatch will be eliminated when the DAC-output circuit and the feedback network form a frequency-compensated voltage divider, i.e., when $R_O C_O = R_F C_F$. This condition can usually be satisfied, but sometimes it requires large values of C_F. Unfortunately, C_F—which introduces an open-loop zero—also produces a closed-loop pole, which reduces the overall bandwidth and results in increased settling time.

R_F is generally fixed by the desired DAC gain; the minimum value of C_O is a property of the converter not under the system-

[1] This process is discussed in some detail, with waveforms, in the Appendix to an article, "Settling Time of Operational Amplifiers," by Bob Demrow, appearing in ANALOG DIALOGUE 4-1 (1970).
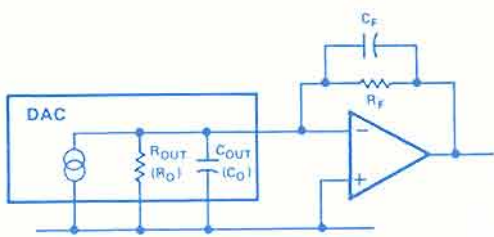
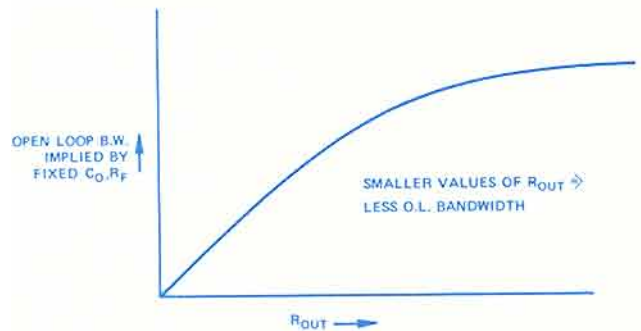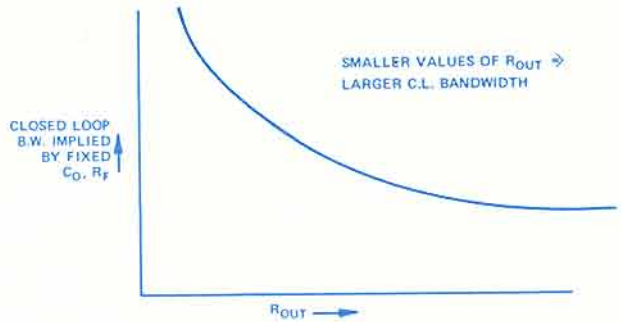Figure 3a. Improving loop stability by the use of feedback capacitance, C_F.
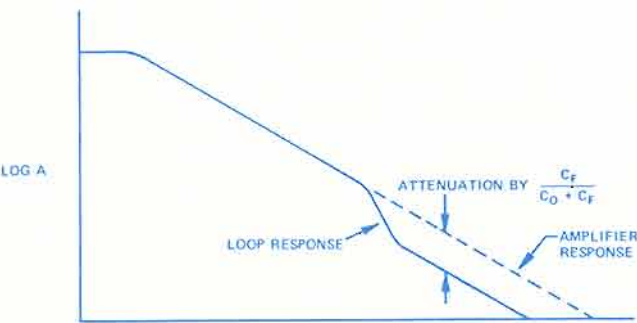

Figure 3b. Response of circuit 3a, neglecting R_{OUT}. Pole-Zero mismatch may yield poor transient response.
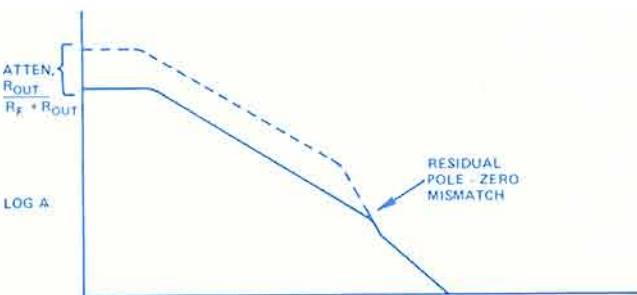
Figure 3c. Response of circuit 3a with finite R_{OUT}.

designer's control. Therefore, C_F and R_O are the only two parameters that can be manipulated (reduced). As R_O' (the effective value of R_O) is reduced by shunting the DAC output with a resistor, the required value of C_F is reduced, and the closed-loop bandwidth is increased (Figure 4). The unity-gain bandwidth of the op amp, b, limits the open-loop system bandwidth, which, in turn, limits the realization of closed-loop bandwidth. As R_O' is reduced, the *open-loop* bandwidth obtainable for a fixed op-amp bandwidth, b, is also reduced.

A compromise can be reached by adjusting R_O' to provide the same open- and closed-loop bandwidth. For a fixed C_O and R_F, the values of R_O' and C_F can be determined from:

$$R_O' C_O = R_F C_F = \frac{1 + \sqrt{1 + 8b\pi R_F C_O}}{4b\pi} \qquad (1)$$

The resistive component at the DAC output also influences the effect of the amplifier offset (V_{OS}) and noise on the overall output voltage. Both are magnified by $(1 + R_F/R_O)$.

Figure 4. Effect of varying R_{OUT} (R_O') on open-loop and closed-loop bandwidth.

DAC's AND OP AMPS - NULLING PROBLEMS

Perhaps the best way to control V_{OS} in an op amp used with a DAC is at the source—to choose an op amp with sufficiently low offset over the temperature range (such as the AD510). The next-best way is to null the op-amp's offset by the standard V_{OS} trim, taking pains to connect the pot wiper to the appropriate supply terminal *at the device*.[2] The amplifier's offset-trim adjustment should be used *only* for V_{OS} nulling; if it is used to compensate for offsets caused by the flow of bias current through the feedback resistor, as well as for offsets occurring in external circuitry, the amplifier input stage will have to be unbalanced, which will cause its V_{OS} tempco to be degraded.

If the amplifier lacks offset-adjust terminals, or if it is necessary to compensate for the additional sources of offset mentioned above in one convenient place, there are two commonly used ways of providing the trim; they are shown in Figure 5. The more-desirable approach is shown in 5a; the correction is applied to the amplifier's positive input terminal, as a voltage. Since it is effectively in series with V_{OS}, the V_{OS} correction is unaffected by changes of R_O'.

The less-effective way is to introduce a current at the summing point, as shown in 5b. If the resistances in the circuit (including R_O') are constant, there is no problem. However, if R_O' can vary, the output offset will change. If the change of R_O' is a function of the applied *digital code*, the result can be increased differential nonlinearity.
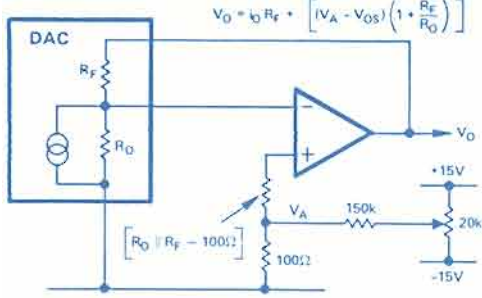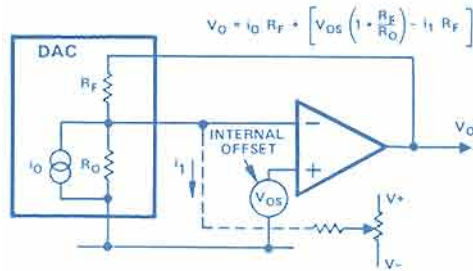
[2] The reasons for this are well-documented in the Application Note, "An IC-Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by the author, available from Analog Devices. A heavily edited version appeared in EDN Magazine, October 5, 1975.

$$V_O = i_O R_F + \left[(V_A - v_{OS})\left(1 + \frac{R_F}{R_O}\right)\right]$$

(a) Nulling offset with voltage applied to op-amp reference input.

$$\left[R_O \| R_F = 100\Omega\right]$$

$$V_O = i_O R_F + \left[V_{OS}\left(1 + \frac{R_F}{R_O}\right) - i_1 R_F\right]$$

(b) Nulling offset with current added at op-amp summing point.

Figure 5. External offset-null methods.

For example, if the DAC is an inverted R-2R-ladder type, as shown in Figure 6, the output resistance, R_O, approaches R for codes containing many 1's, 3R for codes containing a single 1, and ∞ for all-0's. If R = 10kΩ, the resistance looking back into the network is about 10kΩ for more than four 1's and 30kΩ for a single 1. Thus, for the one-bit transition from 0011111111 to 0100000000, the error voltage, $V_{OS} (1 + R_F/R_O)$, changes from 2 V_{OS} to $(4/3)V_{OS}$. If the offset had been nulled at all-0's $(1 + R_F/R_O = 1$, since $R_O \to \infty)$, the offset error will be $+V_{OS}$ at the first code and $(+1/3)V_{OS}$ at the second code; the incremental change of error will be $(-2/3)V_{OS}$. If V_{OS} is not much smaller than the voltage equivalent of the least-significant bit, a tangible error will result. It will be especially pernicious in the case of a multiplying-DAC application with small analog inputs. The solution is simple: use Figure 5a instead of 5b.
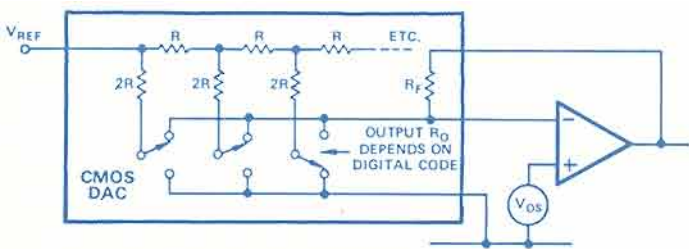

Figure 6. Variable output resistance of inverted R-2R ladder in CMOS and voltage-switching DAC's.

"Foreign" currents in common ground and power lines can introduce offset, noise, and other errors that will be amplified in the same way as V_{OS} errors. It is important to refer the amplifier circuit (and its external V_{OS} trim), the load across which the output voltage is developed, and the DAC's reference input — all of these — to the DAC terminals, in the manner shown in Figure 7.
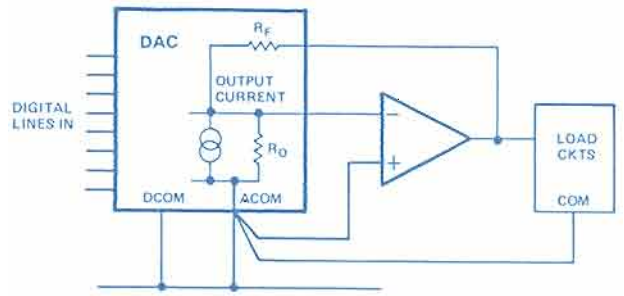

Figure 7. Referring buffer amplifier and load circuits to analog common.

BYPASSING AND DECOUPLING

In "virtual-ground" systems, such as an op amp, driven by a current-output DAC, the DAC output current doesn't actually return to ground, but to one of the power supplies, by way of the op amp's output stage (Figure 8). To reduce the impedance in the high-frequency current path, the bypass capacitor should be connected so as to return the currents from one (or both) power terminals to ground at the DAC. If the DAC output is active, it may require bypassing of its own supplies for the same reason.

WARNING: You and your drafting department may have conflicting objectives. Your objective is to design circuits that work and to communicate the important details to whoever assembles them. Your drafting department (or so it may seem) has the objective of drawing nice, neat, squared-off diagrams, in which the lines representing conductors are nicely equipotential. You may have noticed that, in Figures 7 and 8, these niceties have been avoided. The lines are configured to resemble closely the job that the wires perform, converging at the common analog connection. Again, the bypass-capacitor lead, in Figure 8, wends its way purposefully around the op amp's acute angle to its power-supply terminal, rather than shooting straight up to meet the power-supply line (a sure recipe for costly debugging). If you think your drafting depart-
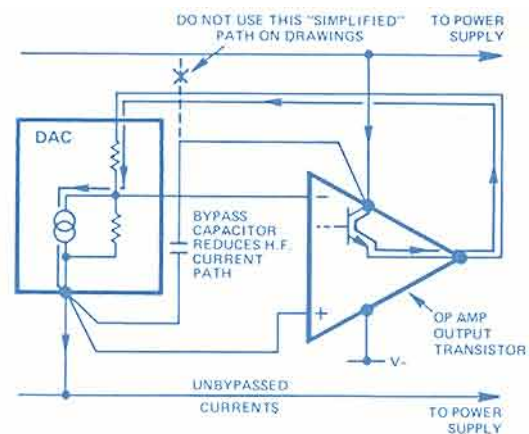

Figure 8. Bypassing power supplies for virtual-ground applications. Arrows show unbypassed current flow.

ment may have a mind of its own, you may want to include a special message for the person who builds the circuit to be sure that it gets built the way you want it built.

Figure 9a shows an example of ineffective decoupling. Here, the op amp drives a load, which connects to a long ground line (returning to the power-supply terminal), and the supply-decoupling for the amplifier returns to the power supply through another long line. The return path for the load current is as long as, or longer than, the supply lines powering the op amp. The "local" decoupling is not only ineffective; it may actually contribute to noise on the power-ground bus.
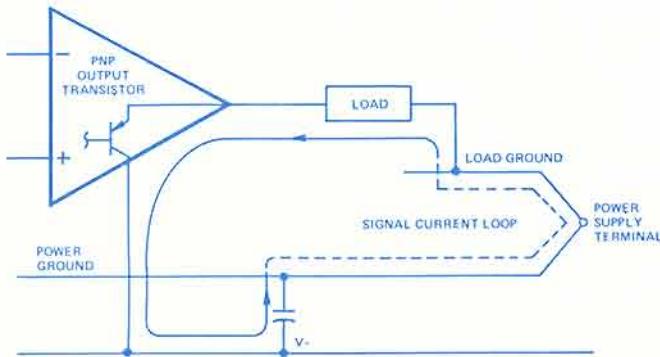
(a) Decoupling for negative supply ineffective.
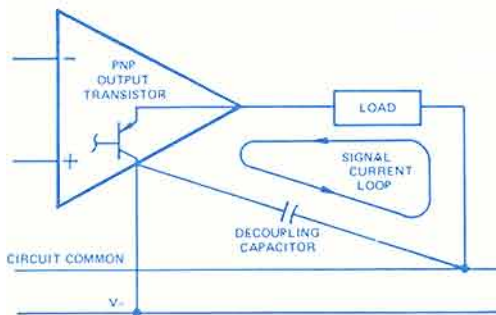
(b) Decoupling negative supply optimized for "grounded" load

Figure 9. Effective and ineffective decoupling.

The cardinal rule of decoupling is: *Make it easy for the current to get back by the shortest path.* Figure 9b shows a more-effective scheme, in which the decoupling capacitor connects by the shortest path between the load return and the load-voltage control element. Here, an op amp, swinging a resistive load-circuit negative, drives the load from an internal PNP transistor, connected to V−. Decoupling the V− pin of the op amp to the low side of the load provides the most direct return path for high-frequency currents, and bypasses them around ground and power buses.
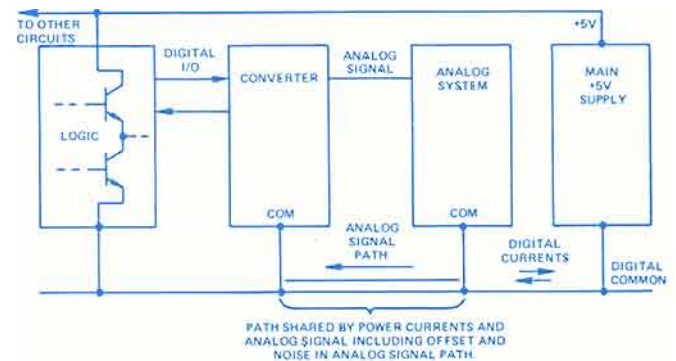
GROUNDING

Great amounts of effort, and many decoupling components, are spent in the attempt to correct problems created by poor ground-current management. In large systems, and in systems which deal with both high-level and low-level signals, "ground" (or common bus) management becomes an important aspect of design. The worst sin— allowing low-level analog signals to share conductors with logic returns or power connections— is an invitation to trouble.

Figure 10a shows an example of a path, shared by digital and analog signals, between the common connections of a converter and an analog system. If the least-significant bit is worth 2.5mV, and digital on-off current fluctuations of the order of 100mA are flowing an a lead with 0.1Ω resistance, the resulting 4-LSB uncertainty (not including spikes and glitches) suggests that it would be folly to waste money on a 12-bit converter, when 10-bit resolution is the very best that can be hoped for, because of wiring limitations.

As Figure 10b shows, in concept, an analog subsystem can be locally interconnected, with a single-wire connection to the digital common. This signal connection carries only the digital currents required for the *converter's* digital interface. Moreover, analog signals are not forced to share a conductor, even with those currents. The analog subsystem should be powered by a supply with a local common return, which may be connected to the digital common but does not share any current-carrying conductors. Ideally, there are no "foreign currents" flowing between the analog system and the digital system, except for those within the converter. If the two systems are joined only at the converter, the foreign currents share the shortest path, and their effect is minimized.

(a) Shared path produces interference and errors.
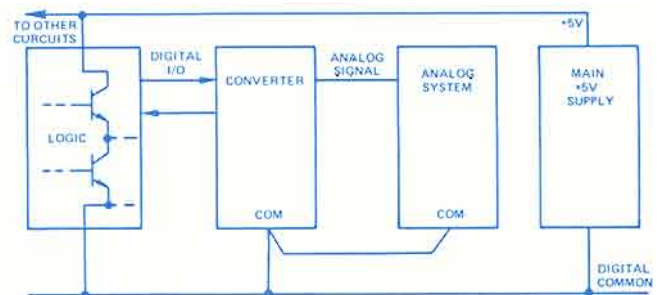
(b) This connection minimizes common impedance between analog and digital (including converter digital currents).

Figure 10. Proper and improper grounding.

In practical systems, it is often impossible to avoid multiple foreign-current paths. In systems which include several d/a and a/d converters, for example, each converter is a path for digital currents, yet it must have access to the analog

signal common. Frequently, the ground problem in such systems can be treated by using an analog common which handles *only* analog signal returns - and a separate system of returns for all digital or high-level signals (Figure 11). Occasionally, a third system of analog power commons may be used to advantage. Since the analog common must be connected to the digital common at no more than one point, safety diodes should be added to any modularized system. These diodes prevent large voltages from developing between ground systems if the key grounding unit, or "Mecca", should be removed from the system.
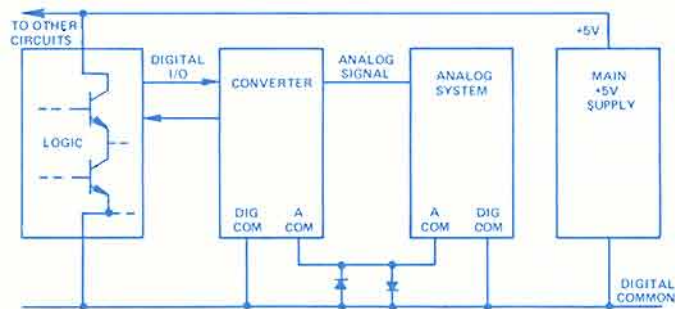

Figure 11. Improved ground current management (analog and digital common must be joined in either converter or analog system. Diodes are fault protection if this connection is broken.)

WHEN COMMON GROUND IS IMPRACTICAL

In large systems, it is often impractical to rely on a single common point for all analog signals. In these cases, some form of differential (or even *isolation*) amplifier is required to translate signals between ground systems. For the inveterate op-amp user, a simple subtractor, or "dynamic bridge" circuit may come to mind. These circuits translate a signal which is referred to one ground system into a similar or amplified signal, referred to a different ground system (Figure 12). The common-mode rejection of the amplifier and a resistance-ratio match are used to eliminate the effects of voltage differences between the two grounds, or common points.
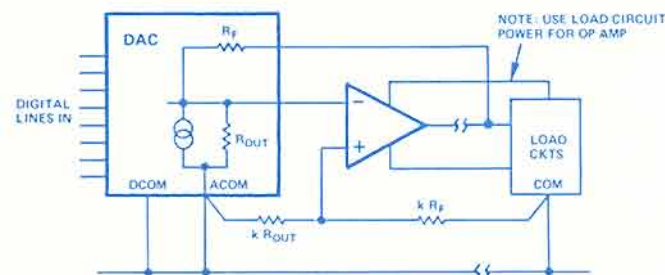

Figure 12. Use of differential amplifier to eliminate the effects of common-mode voltage.

It is generally wise to power the op amp from the power available at the *load* side of the circuit, and/or to decouple it with respect to the *load* common. The reason for this can be deduced from the circuit architecture of the most-common types of op amps (Figure 13).
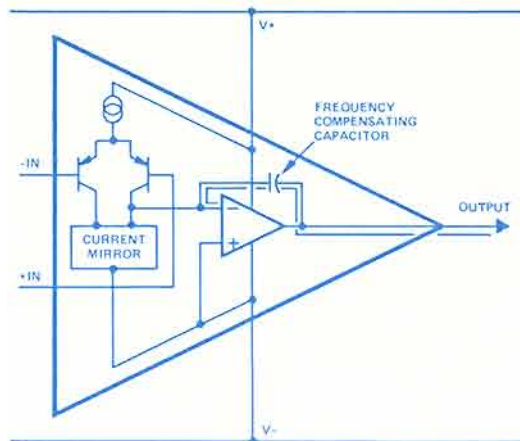

Figure 13. Typical op-amp circuit architecture. Reference for output integrator is V−.

An op amp converts a differential input signal to a single-ended output signal. In many popular op amps, the differential-to-single-ended conversion is done with respect to V− (some use V+), and the resulting signal drives an integrator.[3] The integrator characteristic is used to frequency-compensate the amplifier, and the integrator input is referred to the single-ended output, at V−. The integrator acts as a unity-gain follower for fast signals applied to its non-inverting (or reference) input. As a result, signals applied to the V− terminal have their high-frequency components conveyed directly to the output. Signals having frequency components above the amplifier *closed-loop* bandwidth will be transmitted from V− to the output with little or no attenuation.

As Figure 14a shows, if the op amp used as a subtractor amplifier is powered from or bypassed to the same common line as the input signal, any high-frequency signals associated with that common will appear as part of the output signal. If the ground-noise includes appreciable high-frequency noise (such as logic currents produce), the common-mode rejection will be defeated.

If, on the other hand (14b), the op-amp supply terminals are referred to the *output* signal common, no extraneous signals are coupled into the integrator. Any ground noise appears as a common-mode input signal and is reduced by the common-mode rejection of the amplifier (which is typically very much better than the negative-supply-voltage rejection at high frequencies).

Since noise-rejection performance of the subtractor depends on carefully matched source and feedback resistance ratios, it cannot be used in all situations. Whenever the source impedance cannot be controlled, or is exceptionally high, the subtractor (or dynamic bridge) becomes impractical. In this situation, ground noise and other remote-grounding difficulties can often be avoided by the use of an *instrumentation amplifier*.

IC instrumentation amplifiers, such as the AD521, accept differential input signals at high impedance, provide a fixed gain (which can be selected without introducing overall feedback that joins the input and output circuitry), and

[3] The reference mentioned in footnote 2 provides considerable detail regarding the integrator-reference and compensation schemes of some 32 device families.
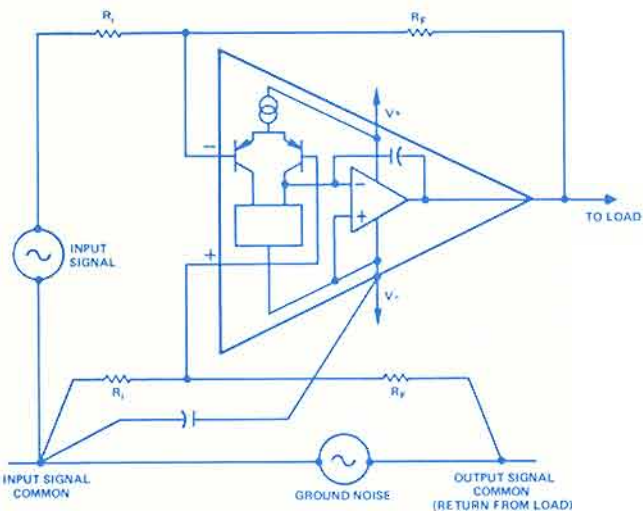
(a) Decoupling to *input* common includes ground noise in the path from the load to the integrator driving the output.
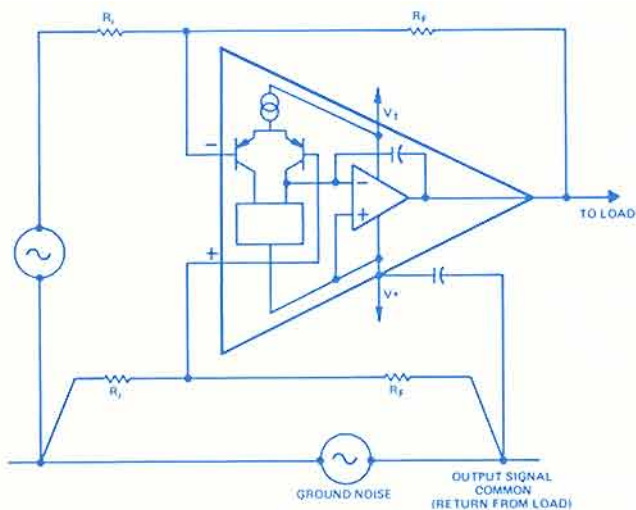
(b) Decoupling to *output* common eliminates ground noise from integrator reference path. Ground noise is minimized in output signal.

Figure 14. Proper and improper decoupling of subtractors using op-amp with integrator referred to V−.

develop the output voltage with respect to a reference terminal, which may be connected to the input common of a remote load-circuit (Figure 15).

Some instrumentation amplifiers are quite versatile and can provide additional functions, while isolating the common
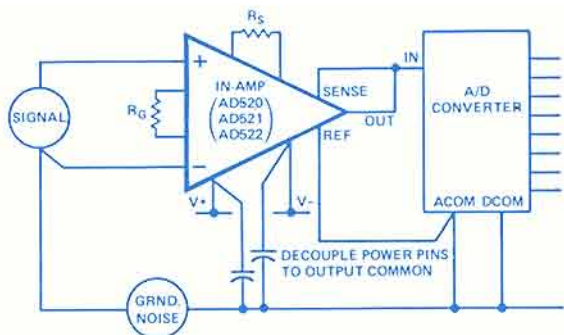

Figure 15. Use of instrumentation amplifier to interface separate ground systems.

returns. For example, the output-reference terminal can be used to add fixed or variable bias voltages to the output.

If the common-mode voltages are very large, or if galvanic isolation is essential for safety, isolation amplifiers, such as the 286 (described elsewhere in these pages), or amplifiers powered by dc-to-dc converters may be highly desirable.

A/D CONVERTERS

The input impedance of many analog-to-digital converters changes during the conversion process and can affect the performance of an amplifier furnishing the input signal.

For example, in successive-approximation converters, the input current is compared to a trial current (Figure 16). The comparison point is diode-clamped, but it may swing plus-and-minus several hundred millivolts. This gives rise to a modulation of the input current. The output impedance of a feedback amplifier is made artifically low by the loop gain. At high frequencies, where the gain is low, the amplifier output impedance rises to its open-loop value. In the case of most IC amplifiers, the open-loop output impedance is a minimum of 25 ohms, due to current-limiting resistors (but is more typically 100-200 ohms).
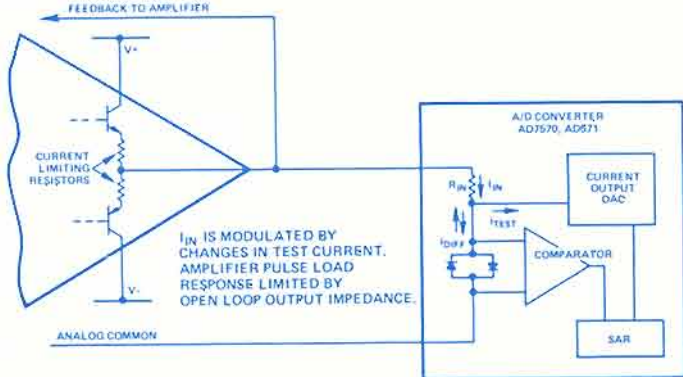

Figure 16. Relationship between successive-approximations A/D converter and op amp that is the source of the input signal.

Even a few-hundred microamperes, reflected from the change in converter loading, can introduce errors in instantaneous input voltage. If the conversion speed and the bandwidth of the amplifier are compatibly fast, the output may return to the nominal voltage before the converter makes its comparison, so that little or no error is introduced. However, many precision amplifiers have relatively narrow bandwidth. This means that they recover very slowly from output transients. Naturally, precision amplifiers are more likely to be used in high-resolution systems, where small errors are less tolerable. As a result, fast, high-resolution systems may suffer from amplifier output-transient errors.

There are a number of ways of solving the problem. Perhaps the easiest is to use an a/d converter that has its own on-board buffer, e.g., the AD572, or most modular types. In other cases, a sample-hold, with low output impedance, may serve as a buffer, as well as to provide the sampling function. Another solution is to use (carefully) a wideband op amp, such as the AD509, which does not include output current-limiting resistors. Finally, it is not difficult to construct an inside-the-loop buffer that can stiffen the output of a slow, accurate amplifier.

Figure 17 shows a simple unity-gain buffer, constructed from an NPN and a PNP transistor in a compound connection. The output impedance of this buffer remains low at high frequencies. A good rule-of-thumb for selecting transistor types to use in complementary-compound is that the input device — in this case, the NPN— should be a high-frequency transistor, and the output device— the PNP— should be a relatively slower transistor.
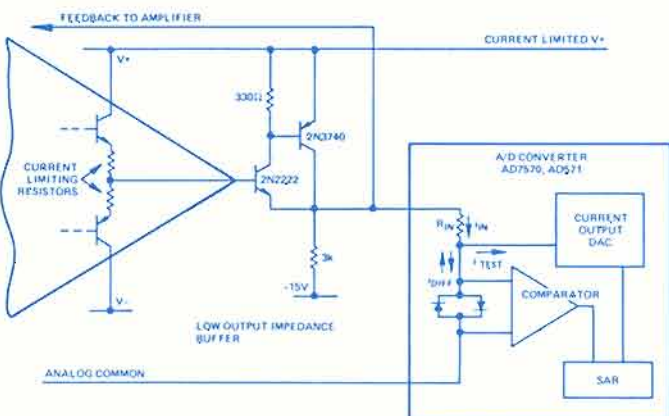

Figure 17. Inside-the-loop buffer provides stiff drive for unipolar ADC.

Since the buffer is not current-limited, a small power-device, capable of pulling down a 200-300mA current-limited supply without damage, has been suggested as the PNP. If the system is definitely safe from overloads, a smaller PNP can be used. This buffer is intended for positive unipolar signals; the 3kΩ resistor provides ample bias to keep the output impedance low over the active range.

A more-complex, protected buffer, for better performance with bipolar input signals is shown in Figure 18. An AD580 voltage reference can be used as a constant-current load to keep the buffer active over the bipolar range. This buffer also includes a bypassed resistor to limit the available output current without pulling down the power bus.
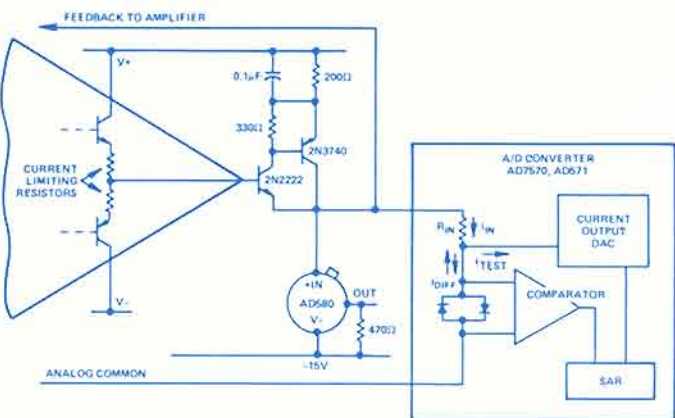

Figure 18. Protected buffer capable of driving bipolar signals into ADC.

TO CONCLUDE

As we told you, our objective was to make you aware of some of the analog problems of implementing interface circuitry, to start you thinking about how to solve them, and to give you some concrete ideas (but not "cookbook remedies"). We hope that they will help make you next system startup somewhat less painful. ▶▶▶