

Techniques for sampling high-speed graphics with lower-speed A/D converters

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One area where the need for high-speed A/D converters becomes apparent is in PC graphics digitizing. While conventional TV images have relatively low bandwidth and can be sampled at 13.5 MHz for component YUV signals or at a multiple (4x) of the subcarrier frequency for PAL or NTSC composite video, PC graphics digitizing requires much higher rates. Traditional CRT monitors accept an analog signal, but LCD monitors provide a pixellated display and need to be driven by a digital signal of the same resolution as the flat panel display in order to generate a full-size screen image. While the straightforward solution is to use an A/D converter specified at the same or a higher clock rate than the maximum pixel rate, two approaches using lower-speed converters are presented in this application note.

Sample rates

Table 1 lists some display formats and rates as specified by VESA. For example, while the XGA standard goes up to 94.5 MHz, most of the panels can handle a screen refresh rate of up to only 75 Hz and are therefore limited to a 78.5-MHz pixel rate at XGA resolution. In this case there is little sense in configuring the PC graphics adaptor to produce 85-Hz output, as the rate will have to be brought down by frame-rate conversion circuitry on the LCD monitor's analog input interface. The system designer shouldn't spend extra money on the analog front end to enable 85-Hz input, as it will not be a recommended operating mode.

Suppose an 80-MHz converter is to be used to process a 95-MHz input signal. The cost/performance tradeoff might actually be better than if a more expensive 95-MHz ADC is used. To help understand how a system can be designed to accept such a high-speed input, the architecture of a typical LCD monitor's analog front end should be examined.

Analog front-end architecture

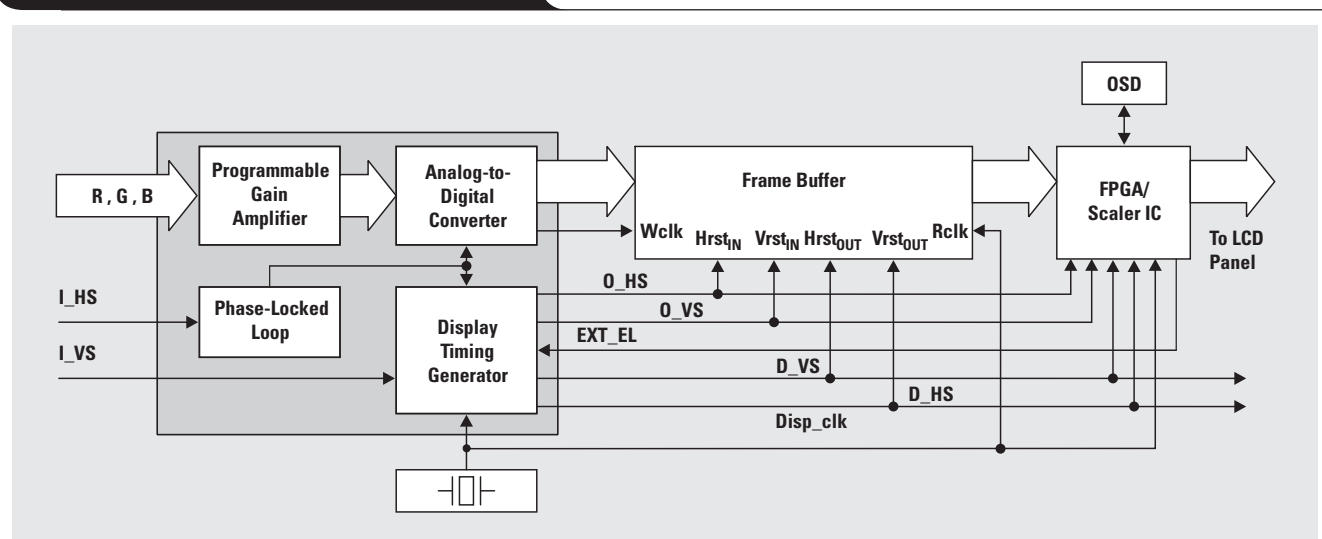
In concept, the analog front end includes a PGA (programmable gain amplifier), an A/D converter for each of the three color components (R,G, and B), a PLL to derive the pixel clock from the line rate, and a functional unit called a "display timing generator" to generate the LCD panel's timing control signals, as shown in Figure 1. This would be all that's required if there weren't a need for image

Table 1. Popular PC graphics formats

	REFRESH RATE (Hz)	PIXEL RATE (MHz)
SVGA (800 x 600)	72	50.000
	75	49.500
	85	56.250
XGA (1024 x 768)	70	75.000
	75	78.750
	85	94.500
SXGA (1280 x 1024)	60	108.000
	75	135.000
	85	157.500

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Figure 1. A typical LCD monitor's front end



A typical LCD monitor's front end includes PGA, ADC, PLL, and DTG. If ADCs with lower sampling rates can be used, the system cost is lower.

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scaling. To ensure full-screen display of lower-resolution images (e.g., VGA on an XGA panel), the image needs to be enlarged (zoomed). An image processor ASIC is normally used to perform the required real-time image scaling. The two-dimensional scaling needs at least a line memory and complete external frame buffer for storing its data. A complete frame buffer is also needed if there is frame-rate-conversion in the system (from an 85-Hz to a 75-Hz refresh rate, for example). It is this frame buffer that gives considerable flexibility for the data acquisition function. The memory decouples the pixel frequency of the analog front end (the data converter) from the display pixel frequency.

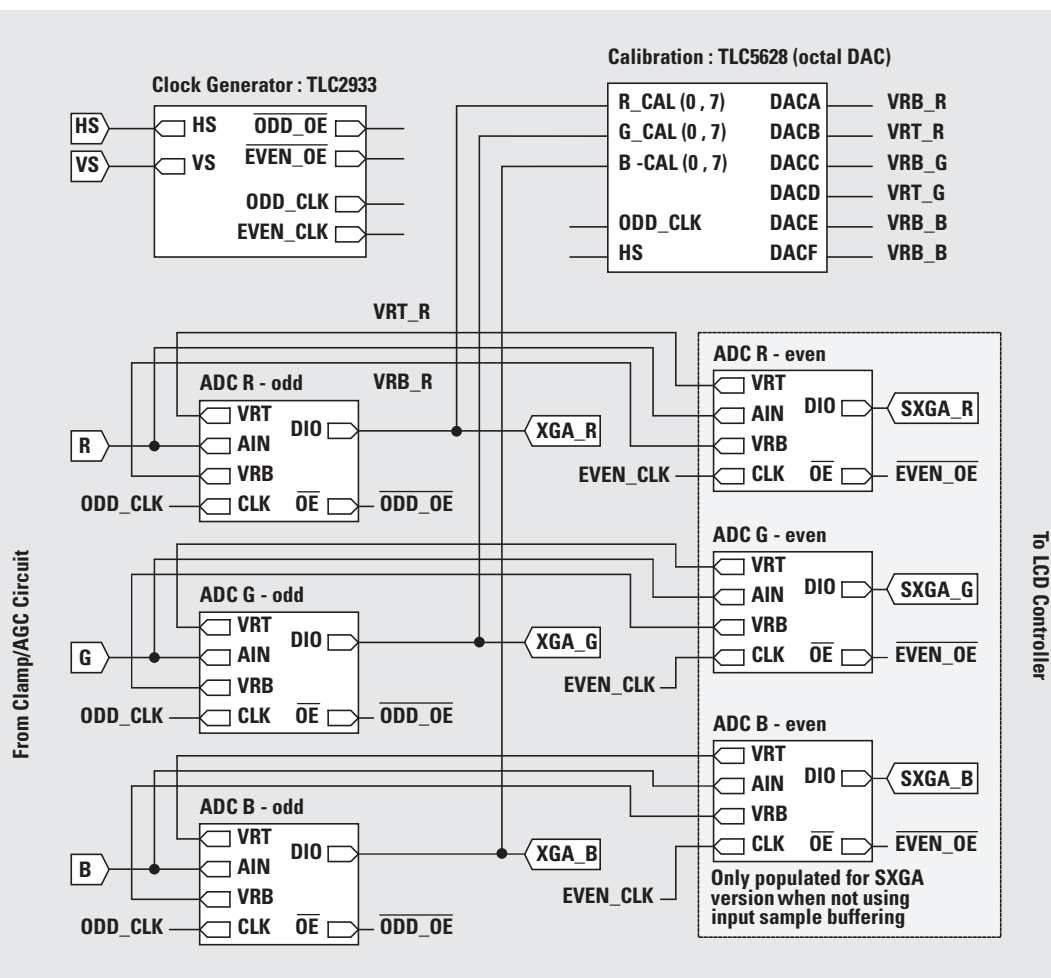
The system could be designed to capture data at a lower speed than the pixel frequency by digitizing selective pixels when the pixel frequency is higher than the maximum speed of the A/D converter. A simple algorithm for this would be the digitization (at half the input pixel rate) of only the odd pixels on every line in odd frames and even

pixels in even frames. In the example of a 94.5-MHz XGA, the converter need only operate at 48 MHz—in this case. A complete frame is captured for every two input frames. The frame buffer will hold the previous frame for further processing until the next one is completely acquired. Because of the lower sampling clock that needs to be generated in the system, there is an advantage on other functional blocks; e.g., the PLL's VCO operating range can be decreased since it needs to operate at up to only 80 MHz, not the original 94.5 MHz.

Advantages and disadvantages

Does all this come without disadvantages? Unfortunately not. Acquiring a full-screen image for only every two input frames essentially halves the horizontal frequency resolution over time. This will result in artifacts in objects that move horizontally in the image; however, given the fact that most LCD monitors will replace traditional analog PC monitors for the display of mostly static images, this performance penalty might be overcome by the price advantage. In the previous example, the 80-MHz converter

Figure 2. LCD monitor front end using reduced sample rates



This LCD monitor front end employs techniques to reduce the sampling rate for XGA performance at a 75-Hz refresh rate. The additional ADCs are needed only if full-speed SXGA performance is desired.

could be used to digitize input images at up to SXGA resolution at an 85-Hz (157.5-MHz) refresh rate, which makes sense only when the LCD panel can handle this resolution or when the resolution is reduced in some other way. This principle holds true only when a frame buffer is available for this function. Depending on the operation mode, a single memory could function for the storage of temporary results from the image scaler (at pixel rates lower or equal to the A/D converter's maximum speed) or act as an input buffer to extend the pixel input range of the LCD monitor, giving up its use of the scaling engine (which remains unused in this case). Higher pixel rates will normally occur for the panel's maximum resolution, so no zooming is needed anyway. If there is no frame memory present, it still might make sense to use lower-speed A/Ds.

Parallel ADCs

Two converters can be used in parallel to acquire the input image at full speed, with each converter operating at only half the input pixel rate. If the converter has an output enable function, like TI's TLV5580 8-bit 80-Msp ADC, the output bus could be used even for combining the A/D outputs, ruling out the need for an external multiplexer. Part and PCB uniformity across multiple LCD product lines might prove this concept to be commercially viable. For instance, a single LCD monitor interface board could handle both a version at up to XGA@75 Hz and a high-end version at higher refresh rates and/or resolutions. In both cases the same lower-priced ADC part can be used. Even using two in parallel for the high-end version might prove more cost-effective than using an expensive high-speed ADC.

To enable a correct matching of ADCs operated in parallel, their digitizing ranges (as set by their bottom/top reference voltages) should be identical. To ensure this, corresponding external reference pins on both parts can be tied together. Converters that provide the flexibility to enter both top and bottom reference voltages independently, like TLV5580, are preferred over parts that accept only a single (mid-range) level and derive both references internally. Small tolerance offsets between parts could (in the latter case) hamper their uniform operation, and the same analog input level could be digitized to different output codes in both converters. Note that for a $1-V_{pp}$ signal, 1 LSB on an 8-bit ADC corresponds to only 4 mV, so board noise in general is an issue. Careful PCB layout using separate analog and digital ground planes connected at a single point (underneath the A/D) is recommended. Converters that clearly separate analog and digital pins on their footprint simplify layout of the ground planes.

Autocalibration

To take accuracy even further, high-end monitors could include an autocalibration feature much like in high-end CRT monitors today where a calibration for color-temperature is provided. In the case of an LCD, a known stable input level is switched into the ADC during the non-active video portion of the image (the horizontal and/or vertical blanking interval). During that time the ADC output codes are monitored by the microcontroller and compared to their expected values. A control loop can adjust the analog input level or the ADC reference levels that may be generated from external DACs. Note that there is already control function on gain and offset of the analog input level for contrast and brightness level control of the display. Both are user controls accessible from the LCD monitor's front side.

Design example

The design example in Figure 2 shows some of the concepts described in this application. Three TLV5580s are used for the XGA@75-Hz board version, and three extra parts are included for the high-end SXGA that samples at full speed. Corresponding references of both odd/even sampling A/Ds are tied together to avoid in-channel offset. The autocalibration feature is implemented using an octal DAC with microprocessor interface. During horizontal sync (HS) the A/D values are read and compared to the expected blanking codes. These differences will adjust the DAC top/bottom DAC outputs. No use is made of the internal bandgap-derived references on the A/D, so they are powered down via their separate power-down pin (PWDN_REF high). Note also that in this design the maximum clock speed on the board is limited to half of the pixel clock. Even the panel interface is of "double pixel width," consisting of two buses for each color component. This reduces EMI considerably and eases PLL design. The same PLL circuit can be used both for XGA and SXGA versions. In the latter case the divider in the PLL feedback loop is programmed to half the number of pixels/line to produce half the pixel clock frequency. Even and odd clock signals run at the same frequency but in opposite phase.

Summary

Although analog LCD interface module design issues have been touched on only briefly, it is clear that there are considerable design trade-offs to be made and much room is left for product differentiation. It is the intent of this application note to present some options focusing on the data converter part and its impact on the complete system design.