SYSTEMATIC DESIGN OF SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTERS

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Abstract

This paper describes the systematic design of $\Sigma\Delta$ analog-to-digital converters (ADC), from the top level of abstraction represented by the filters defining signal and noise transfer functions, passing through the architecture-level, where topology-related performance is calculated and simulated, and finally down to circuit parameters. The systematic approach allows the evaluation of different loop filters and quantizer resolutions, mapped on single-loop or cascaded topologies with both discrete- and continuous-time loop filters.

1. Spectral Noise Shaping

Analog signals are continuous both in time and amplitude and their spectrum contains non-zero tones in a finite frequency band as an effect of their continuity in amplitude. In Fig. 1 the input signal spectrum is placed around DC (the void trapezoid) and extends to f_b in the positive spectrum. The analog-to-digital conversion requires the analog input signal to firstly be *sampled* by a sample-and-hold (the block S/H) which transforms it into an analog, discrete-time signal, only changing its amplitude at periodic intervals T_s (set by the sampling frequency f_s, $T_s = 1/f_s$). Because sampling introduces instantaneous amplitude

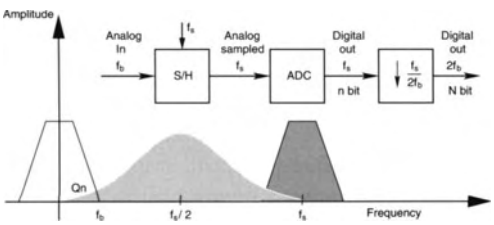

Figure 1: Noise shaping ADC

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changes in the analog signal, the spectrum of the sampled signal has infinite bandwidth, by replicating the input signal spectrum around the multiples of the sampling frequency (shaded spectrum around f_s). The sampled signal is quantized by the ADC, being *quantized* into a discrete-time, discrete-amplitude (digital) form. From a "spectral" point of view, the quantization introduces *quantization noise* in the signal bandwidth which limits the conversion resolution (as the ratio between a reference level and the minimal signal that can be converted). To reduce the in-band noise power, the ADC operates faster than $2f_b$, as an *oversampled ADC*. In this case, the *oversampling ratio* (OSR) is a design parameter showing how many times is f_s larger than the minimal value required by the Nyquist theorem

$$OSR = \frac{f_s}{2f_b} \tag{1}$$

With oversampling, only a part of the quantization noise power falls in the signal bandwidth. Furthermore, for large OSRs, the S/H block is not really required since the input signal changes little during one T_s period. Given enough OSR, the ADC resolution *n* can be eventually reduced to 1 bit, while attaining the final target resolution *N* (after the decimation filter).

To reduce the required OSR needed for a conversion resolution *N*, keeping a constant number of ADC bits *n*, noise shaping is applied. This is accomplished by high-pass filtering the quantization noise to displace most of its power from low frequencies where the input signal spectrum is placed to higher frequencies close to $f_s/2$, as shown in Fig. 1 by the bell-shaped shade centered on $f_s/2$. The amount of quantization noise power still left inside the signal bandwidth Q_n depends on the exact filtering applied in terms of filter order and cutoff frequency.

One method to attain a high-pass noise filtering is to implement a sigma-delta ($\Sigma\Delta$) loop around the quantizer, with a loop filter setting the noise shaping. $\Sigma\Delta$ ADCs are well-studied and versatile architectures which only miss one important feature: a highly-accurate analytical model.

2. Filter-Level Analysis

2.1. Linear Model. Transfer Functions

A generic discrete-time representation of a $\Sigma\Delta$ ADC, given in Fig. 2, is best used to explain the functioning of the $\Sigma\Delta$ ADC modeled as a linear system. The loop filter has two sections, a forward filter G(z) and a feedback filter H(z). The input signal X(z) is applied and compared with the signal fed back by H(z), filtered through G(z) and quantized to give the digital output. The quantization introduces an error E(Z) which is modeled as input-signal-independent and directly added to the output, in the quantizer (represented as a summation point).

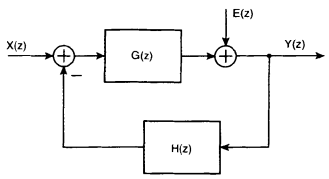

Figure 2: Noise shaper

The two $\Sigma\Delta$ transfer functions are defined on the system above: the *signal transfer function* to characterize the transfer from X(z) to Y(z) and the *noise transfer function* for the partial contribution of E(z) in Y(z)

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{2}$$

These functions can be independently defined because a linear model for the quantizer is assumed, thus making the whole system a linear one where superposition rules apply. The definitions of the two transfer functions are based on the two sections of the loop filter:

$$\begin{aligned} STF(z) &= \frac{Y(z)}{X(z)} = \frac{G(z)}{1+G(z)H(z)} \\ NTF(z) &= \frac{Y(z)}{E(z)} = \frac{1}{1+G(z)H(z)} \end{aligned} \tag{3}$$

The STF can be approximated with 1 (one) at frequencies where G(z) is large and H(z) is unity, while, at the same frequencies, NTF can be approximated with 0 (zero) [1]. Note that, if the filters are implemented using integrators, the frequency band where G(z) is large is around DC (see Fig. 3). If resonators are used instead of integrators, the central frequency for the region of interest is shifted around the resonance frequency of the resonators. The latter approach allows for *bandpass converters* to be designed. The feedback filter H(z) is usually not implemented separately, but as distributed feedbacks into the G(z) [3].

Typical shapes for NTF and STF are shown in Figure 3. The full line represents the STF while the dashed line is a typical NTF for low-pass $\Sigma\Delta$ converters. The important parameters of the two curves are shown, for STF the DC value and in-band ripple and for NTF the $f_s/2$ gain and out-of-band ripple. It is worth noting that the STF gain is dropping out of the band, rejecting high frequency signals. When STF is not well controlled it can also show an overshoot just above signal band limit, which is tightening the rejection specification for the digital filter following the converter [1].

The steepness of the NTF curve inside the signal band is given by the order of the loop, which is the order of the numerator of the product G(z)H(z) (see Fig. 2) multiplied by 20dB/dec. The poles of this product give the zeros of NTF

while the zeros of the G(z)H(z) product affect the poles of NTF. Using resonators inside the G(z), the NTF zeros can be moved away from DC and spread inside the signal bandwidth in a manner which minimizes total quantization noise power. This noise power, scaled by the quantization noise spectral density, is represented on the graph in Fig. 3 as the shaded triangle marked P_{qnoise} which gives the hard (theoretical) limit for the conversion resolution in the given band, for a given NTF and quantization noise total power.

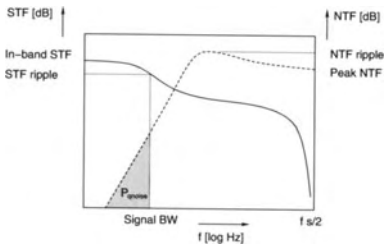

Figure 3: NTF and STF amplitude characteristics for a low-pass ΣΔ ADC

A large STF ripple is not convenient for most applications, which do not tolerate frequency-dependent in-band gain. For certain applications the STF phase is also important, as is the case with audio applications. The STF out-of-band attenuation can decrease the risk of input signal aliasing and relax the specifications for the digital decimating filter following the ADC, but is not a design goal when signal conditioning is available in front of the ADC. The out-of-band NTF magnitude influences the amount of quantization noise re-circulated on the loop [1]. A large magnitude around $f_s/2$ will put more noise at the input of the quantizer, thus reducing the maximum signal level which can still be processed. A high out-of-band NTF ripple makes the NTF shape more sensitive to process-induced pole shifts, possibly turning a stable design into a less-stable or even unstable implementation.

2.2. Design of Loop Transfer Functions

The NTF is the filter defining the resolution and other properties of a ΣΔ ADC, hence the design process always starts by defining this transfer function. Even if different filter families (Butterworth, Chebyshev or elliptic) can be used, an NTF filter has to be causal and scaled to yield an impulse-response starting with a unity output. The causality is required for a filter mapped to physical systems and implies that there cannot be more zeros than poles in the $NTF(z)$. The requirement of initial unity impulse-response stems from the architecture of a ΣΔ ADC, as shown in the previous section, Fig. 2. There is no direct (zero-delay) feedback from the quantizer output to the quantizer input. All the feedback is

supplied through the loop filter $G(z)H(z)$ which contains at least one delay in its forward path.

The required scaling of the NTF filter introduces a relationship between its cutoff (-3dB) frequency and its magnitude at half the sampling frequency $f_s/2$. An increased cutoff frequency induces a larger magnitude at $f_s/2$, as shown in Fig. 4 for the NTF of a fourth-order $\Sigma\Delta$ ADC with Chebyshev poles. The full line has the lowest cutoff frequency and the smallest magnitude in the same time. It is the *least aggressive* NTF in the set shown. The legend in the graph also shows simulated DR for the three curves designed into single-bit $\Sigma\Delta$ ADC architectures, and the least aggressive curve offers the lowest DR (66dB) from the three. This is caused by a larger in-band (DC to *Signal BW* limit) quantization noise power compared with the more aggressive members of the set.

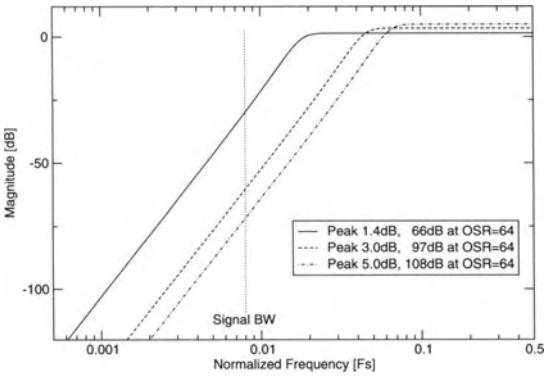

Figure 4: Choice of NTF aggressiveness for a fourth order $\Sigma\Delta$ ADC

2.3. Continuous-Time Loop Filters

Starting from DT loop filters, continuous-time equivalents can also be built. A noise shaper having the loop filter implemented with CT circuits still remains a sampled system [7], as shown in Fig. 5. Its output $Y(s)$ supplied by the quantizer only changes on the edge of a sampling clock signal with period T_s. Even with a passive DAC (a pair of resistors for example), the sampled nature of $Y(s)$ produces a DAC output $D(s)$ which is sampled with the same T_s. Assuming the input signal $X(s)$ is largely oversampled, the $\Sigma\Delta$ ADC in Fig. 5 can be designed to be equivalent with the DT-based version in Fig. 2. Noting $\mathcal{L}^{-1}\{\cdot\}$ the inverse Laplace transform for CT transfer functions and $\mathcal{Z}^{-1}\{\cdot\}$ the inverse $\mathcal{Z}$ transform for DT transfer functions, a mapping is performed between the complete transfer functions NTF and STF. By designing the entire $N\hat{T}F(s)$ and $S\hat{T}F(s)$ to show

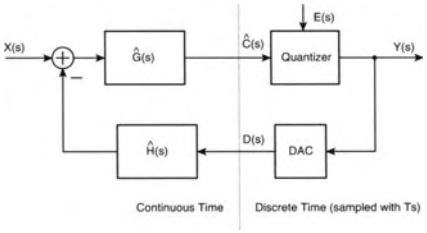

Figure 5: Noise shaper with continuous-time loop filter

identical impulse responses:

$$\begin{aligned} \mathcal{Z}^{-1}\{NTF(z)\} &= \mathcal{L}^{-1}\{N\hat{T}F(s)\}|_{t=nT_s} \\ \mathcal{Z}^{-1}\{STF(z)\} &= \mathcal{L}^{-1}\{S\hat{T}F(s)\}|_{t=nT_s} \end{aligned} \tag{4}$$

the partial contributions of the input signal and of the quantization noise to the quantizer input are identical in the two designs. This opens good comparison possibilities between the functioning of the DT and CT equivalent loops because the poles and zeros of the entire transfer functions are matched.

The direct mapping of NTF and STF assumes a constant DAC output during one clock cycle. However, return-to-zero (RTZ) DAC waveforms may be needed in high-DR CT designs. RTZ DACs switch from zero to nominal value during any clock period and, with such DAC waveforms, the design method has to be adapted to consider the Laplace transform of the DAC impulse response.

2.3.1. Fundamental Performance Limitation Compared to DT Loops

It has been mentioned before that a mapping of complete NTF and STF from realizable DT loop filters to CT equivalents opens the possibility to compare the performance of two equivalent implementations of virtually the same design. "Virtually" highlights the fact that an equivalence is only valid when the linear model holds in both cases, which is not true with large input signals. Therefore, it is important to analyze the performance of the two $\Sigma\Delta$ ADCs, with equivalent DT and CT loop filters respectively, as independent designs and compare the results from time-domain simulations which account for the non-linear loop transfer.

The range of usable NTF aggressiveness (as defined by the lower and upper limits of peak NTF magnitude yielding a stable NTF) has been found to vary with the order of the loop, the number of bits in the quantizer, as well as with the nature of the loop filter, DT or CT. This is proven in Fig. 6 for a set of fifth-order, single-loop modulators, with the number of quantizer bits ranging from 1 to 8. For any number of bits in the quantizer, the CT equivalents cannot

be designed as aggressive as the DT designs. Also, the range of usable NTFs increases very fast with the number of quantizer bits for DT designs but very slow for the CT equivalents. These results are valid for NRZ, CT DAC pulses. Independent simulations using RZ DAC pulses proved to yield results closer to DT designs, intuitively placing the cause of the effects explained for the NRZ designs in the DAC pulse shape.

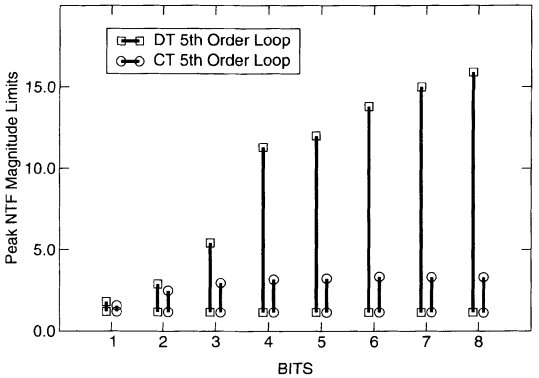

Figure 6: Peak NTF magnitude ranges for DT and CT loops of ORDER=5

2.3.2. Sensitivity to Initial Accuracy of Implemented Coefficients

One issue which is not present with DT loop design is the initial accuracy of all loop coefficients implemented in the final circuit. As opposed to DT loops, where all coefficients are implemented as ratios of either capacitors or currents [3] [9] [10], in CT loops the typical coefficient implementation is ultimately a resistor-capacitor (RC) product [11]. If no calibration is available for the RC product [12], the two on-chip passive components show independent spreads from their designed values. As a result, all RC products are within 30% in error from their nominal value.

The method to cope with this spread of loop coefficients is based on the assumption that spread is the same across a processed wafer. Since all the resistors and capacitors (of the same type) on the chip have identical initial accuracies, the feedback and the forward (and feedforward) paths keep the same gain ratios. The shapes of NTF and STF are not affected, but the NTF corner frequency is changed so enough margin should be considered for the quantization noise power when the high-pass filter is designed. The output of all integrators scales with the initial accuracy of the coefficients, so care should be taken that even when the loop coefficients are 30% larger than nominal no clipping occurs.

3. Architecture-Level Analysis

3.1. Non-Linear Loop Transfer

The linear model only yields accurate results if the two signals entering the system and used to define the transfer functions, X(z) and E(z) in Fig. 2, are mutually independent. This is true for small input signals, when the quantizer input is dominated by re-circulated quantization noise. At high input signals however, the signal at the input of the quantizer also contains some of the input signal spectrum.

From the point of view of attainable DR it is obviously more convenient to use aggressive NTF filters. There is however a price to pay for the NTF aggressiveness, and this is a reduced overloading level (OVL). A lower-than-0dBR OVL is produced by the modulation of the quantization noise with the input signal spectral components. A more aggressive NTF concentrates more quantization noise power around $f_s/2$ for small input signal levels. Hence, at large input signal levels, larger spectral components will be found in the quantization noise spectrum around the input signal frequencies, producing faster overloading due to increased non-linear $\Sigma\Delta$ loop transfer. Fig. 7 shows the variation of OVL as a function of the peak NTF magnitude (NTF magnitude at $f_s/2$ for flat out-of-band NTF) for a fourth-order single-bit $\Sigma\Delta$ ADC. The peak NTF magnitude is used to measure its aggressiveness rather than the cutoff frequency in order to highlight the effect explained above. The number of bits in the quantizer has to be taken into account since it changes the power of the quantization noise *and* the tonal behavior of the quantization noise at large input signals. This curve, connected with the DR values shown in Fig. 4, shows the trade-off between the attainable DR and peak SNDR (if limited only by OVL).

The graphs in Figs. 4 and 7 also contain the limits of the usable NTF ag-

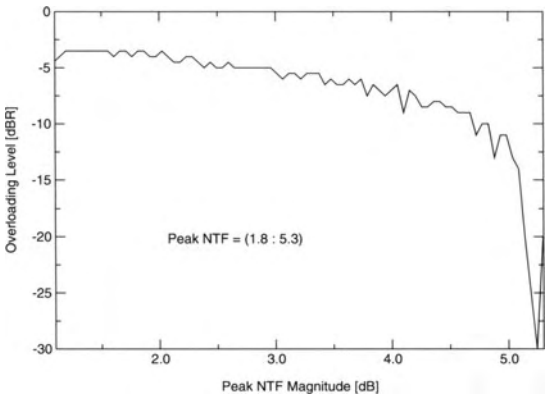

Figure 7: Overloading level variation with NTF aggressiveness

gressiveness for a fourth-order, single-bit ΣΔ ADC. It is impossible to design a stable ΣΔ ADC with this architecture if the peak NTF magnitude falls outside the shown limits [1].

3.2. Performance Metrics

During the design and characterization of a ΣΔ ADC, a number of performance metrics are collected from output spectra. Such a spectrum is shown in Fig. 8, generated by a fast Fourier transform (FFT) of the digital output of a fourth-order ΣΔ ADC with a 5-bit quantizer. The input signal is set close to the OVL, at -2dBR. The entire spectrum is scaled to bring the reference level to 0dBR. On such a graph it can be measured if the noise shaping has the correct order (here, 80dB/decade outside the signal bandwidth), showing the loop is not overloaded. The resolution and the distortion are also measured on this spectrum.

As with other ADCs, the resolution of a ΣΔ ADC is the measure for the smallest analog signal which can be converted. Only in the case of ΣΔ converters, due to the quantization noise particular shape, the definition of the resolution does not start from the noise floor level, but rather from the total in-band noise power which gives the dynamic range (DR)

$$DR = -10log_{10}\left(\frac{1}{2}\int_{f=0}^{f=f_b} Y(f)^2\right) \; [dBR] \tag{5}$$

with f_b being the input signal bandwidth (*Signal BW* in Fig. 3) and $Y(f)$ being the quantization noise spectral power density, measured as the spectrum of the digital stream output *with no input signal.*

Because of the overloading effect, DR cannot be used to define the effective number of bits (ENOB) since the full input scale is not at 0dBR. In the same time, DR does not explicitly include non-linearity information. To determine ENOB,

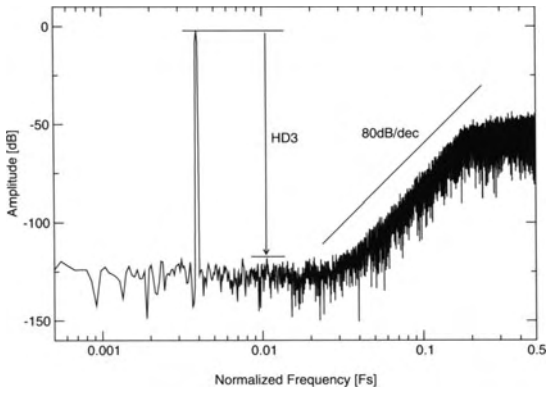

Figure 8: FFT spectrum for the output digital stream

the ratio between the input signal power and the power of all the other in-band spectral components is calculated as the signal-to-(noise+distortion) ratio SNDR

$$SNDR = 10log_{10}\left(\frac{1}{2}\int_{f=f_{in}-\delta f}^{f=f_{in}+\delta f} Y(f)^2\right) + DR\,[dB] \tag{6}$$

with f_{in} the frequency of the single-tone input signal, δf a small frequency shift and $Y(f)$ the spectral power density of the output signal. The SNDR is used to approximately calculate the ENOB as

$$ENOB = \frac{(Peak\ SNDR) - 1.76}{6.02} \approx \frac{Peak\ SNDR}{6} \tag{7}$$

To fully characterize the $\Sigma\Delta$ ADC, two other curves are used: the variation of DR and SNDR with the input signal amplitude. A large variation of DR with the input signal amplitude shows a highly-aggressive NTF or circuit-induced non-ideal effects, the differential non-linearity (DNL) can be measured on the SNDR curve as local changes of the slope and integral non-linearity (INL) as a variation of the average slope from the desired conversion gain.

3.3. Single Loop Topologies

Different topological variants can be used to design "stable" (or rather "realizable") $\Sigma\Delta$ ADCs. No topology design can stop the non-linear behavior of the $\Sigma\Delta$ loop to become apparent at high input signals, therefore the overloading level is less than 0dBR for all implementations. However, some topologies behave better than others at large input signals in terms of OVL value, increasing it by one or two dBR. OVL is much tighter connected with the NTF aggressiveness than with the $\Sigma\Delta$ topology used. Why "realizable" is a better term than "stable" when it comes to characterizing a topology becomes apparent by taking a look at Fig. 9 which is a typical fourth-order "realizable" topology, sometimes praised to be the most "stable" one due to its feedforward coefficients $b_1 \cdots b_3$ [5]. Without the feedforward coefficients, the only NTF that can be mapped on this topology would be

$$NTF(z) = \frac{(z-1)^4}{(z-1)^4 + f_1 a_1 a_2 a_3 a_4} \tag{8}$$

The NTF(z) above offers very little freedom in designing its poles and is practically impossible to map on a convenient filter shape like the ones in Fig. 4.

3.3.1. Mapping of Transfer Functions to Loop Coefficients

Starting from Fig. 9, the expressions of designable NTF and STF can be calculated from Eq. 3 after expressing G(z) and G(z)H(z) as sums of products of loop

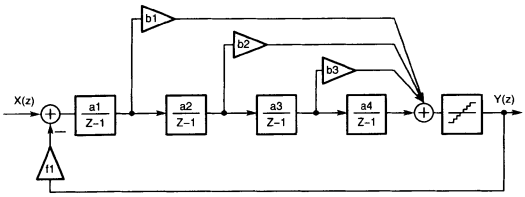

Figure 9: Distributed feedforward topology

coefficients $a_1 \cdots a_4$ and $b_1 \cdots b_3$. The filter G(z) is the partial contribution of the input signal X(z) to the quantizer input

$$G(z) = \frac{b_1 a_1}{z-1} + \frac{b_2 a_1 a_2}{(z-1)^2} + \frac{b_3 a_1 a_2 a_3}{(z-1)^3} + \frac{a_1 a_2 a_3 a_4}{(z-1)^4} \tag{9}$$

The other filter of interest, G(z)H(z), is

$$G(z)H(z) = -f_1 G(z) \tag{10}$$

By replacing the two expressions above in Eq. 3, the two transfer functions are easily written as $NTF''(z-1)$ and $STF''(z-1)$

$$\begin{aligned} NTF''(z-1) &= \frac{(z-1)^4}{\sum_{j=4}^{0} n_j (z-1)^j} \\ STF''(z-1) &= \frac{\sum_{i=3}^{0} m_i (z-1)^i}{\sum_{j=4}^{0} n_j (z-1)^j} \end{aligned} \tag{11}$$

with the polynomial coefficients calculated from the topology coefficients. The NTF and STF are only represented as functions of $(z-1)$ instead of z because they are easier to extract from the topology in this form. As such, they can still be mapped to an equivalent form of the filters generated from a set of target poles and zeros.

A complementary topology replaces the three feedforwards with three feedback coefficients, as shown in Fig. 10. The three feedback coefficients f_2, f_3

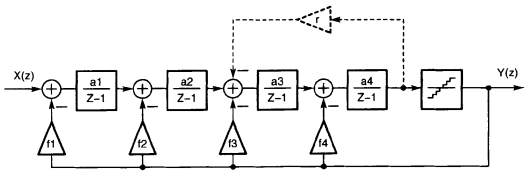

Figure 10: Distributed feedback topology

and f_4 are sufficient to offer control over the pole structure of the NTF and STF, hence this topology can also be used for $\Sigma\Delta$ ADC designs. Because only three feedback coefficients can be added, this architecture still lacks control over the STF zeros, independently of the NTF poles. To gain control over STF zeros as well, there is obviously need to use a more complex topology by connecting both distributed feedbacks and feedforwards.

Note that, although all four NTF zeros are shown in Eq. 11 as being placed at DC (z=1), it is possible, with minor architecture changes, to spread the zeros inside the signal bandwidth and further reduce the NTF's in-band mean value, thus reducing the total in-band quantization noise power. The use of a resonator (shown dashed in Fig. 10, loop coefficient r) introduces a zero in the NTF(z) at

$$z_{in-band} = \sqrt{1 + ra_3a_4} \tag{12}$$

Taking advantage of the usually small value of r caused by the small value of $z_{in-band}$ (especially at high OSR), the resonator can be completely ignored in the first mapping phase and only calculated and added after the integrator coefficients have been determined. Multiple resonators can be added to reduce the NTF in-band magnitude, the limit of their number being set by the loop order divided by two. From the circuit point of view, it is more efficient (both in area and power) to add resonators starting from the end of the loop filter.

The mapping flow is therefore a prioritized list starting with the strict mapping of NTF's poles, followed by the optional mapping of STF's zeros (depending of design requirements and architecture complexity), and ending with the addition of resonators in case more resolution is desired.

3.3.2. Noise and Distortion Contribution of Individual Integrators

Conversion performance limits for a low-pass $\Sigma\Delta$ converter are set by the noise and distortion, which are contributed by all integrators in the $\Sigma\Delta$ loop. Noise is generated in each integrator by resistors and active devices (MOS transistors). Distortion is caused by large-signal non-linear behavior of active devices. The weights associated with the noise and distortion contribution of each particular integrator in a $\Sigma\Delta$ loop depend on the loop gain from the input to the respective integrator.

For the following calculations only the white noise will be considered, generated in a bandwidth larger than half the sampling frequency, $f_s/2$. Noting the total noise power at the input of each integrator $P_{wn_i}, i = 1 \cdots 4$ (for a fourth order loop as shown in Figs. 9 or 10) and knowing the coefficient of integrator i is a_i, the power P_{wn_i} can be referred to the input of the converter as

$$P_i = P_{wn_i} \left(\prod_{j=1}^{i-1} \frac{1}{a_j^2} \right) \frac{\pi^{2(i-1)}}{(2i-1)OSR^{2i-1}} \tag{13}$$

under the assumption that the signal bandwidth f_b is much smaller than f_s.

The distortion power introduced by integrator i, noted D_{n_i} for similarity with the noise contributions, refers back to the input of the loop by the worst-case integrator gain, which is at the end of the input signal bandwidth. Assuming a large OSR, the input-referred distortion gets a simplified form

$$D_i = D_{n_i} \left(\prod_{j=1}^{i-1} \frac{1}{a_j^2} \right) \left(\frac{\pi}{OSR} \right)^{2(i-1)} \tag{14}$$

3.4. Cascaded Topologies

Cascaded $\Sigma\Delta$ ADC designs consist of a chain of $\Sigma\Delta$ ADC loops, only the first loop processing the input signal while the following ones process the quantization noise of the previous loop in the chain, respectively. In this way, the cascaded $\Sigma\Delta$ ADC designs maximize both the DR by using highly-aggressive (high cutoff frequency) noise shaping and the OVL by only applying the full input signal to a low-order loop placed as the first stage in the cascade. Cascaded designs are convenient in applications where a de-coupling between the increase in DR and decrease in peak SNDR is wanted at a fixed OSR, as is the case with broadband ADCs that reach into technology-limited OSR values.

3.4.1. Digital Cancellation of Quantization Noise

One possible topology for a fifth-order, three-loop cascade $\Sigma\Delta$ ADC is given in Fig. 11. It consists of a first loop, taking the input signal $X(z)$ and generating the digital stream $Y_1(z)$ which contains a delayed version of $X(z)$ and quantization noise $E_1(z)$ shaped by the second-order NTF_1. The subsequent loops convert the un-shaped quantization noise of the previous loop in cascade. Therefore the OVL is only limited by the second-order first loop, a likely larger value than what can be obtained with a fifth-order loop. The digital part of the topology, at the right of the dashed boundary, cancels all lower-order shaped quantization noise, allowing only the fifth-order shaped noise generated in the third loop to still be present in the output digital stream $Y(z)$. This is accomplished by combining the individual outputs $Y_{1...3}$ filtered through digital replicas of the analog NTF_1 and NTF_2 to generate the output stream (assuming g_1, g_2 and g_3 are 1)

$$Y(z) = X(z)z^{-5} + E_3(z)NTF_1(z)NTF_2(z)NTF_3(z) \tag{15}$$

According to this equation built on linear model of the loops in the cascade, only the quantization noise generated by the last loop in the cascade and shaped by the fifth-order product of all NTFs is present in the output stream, so the topology ideally attains the same DR as a fifth-order single-loop $\Sigma\Delta$ ADC with a quantizer having $N3$ bits.

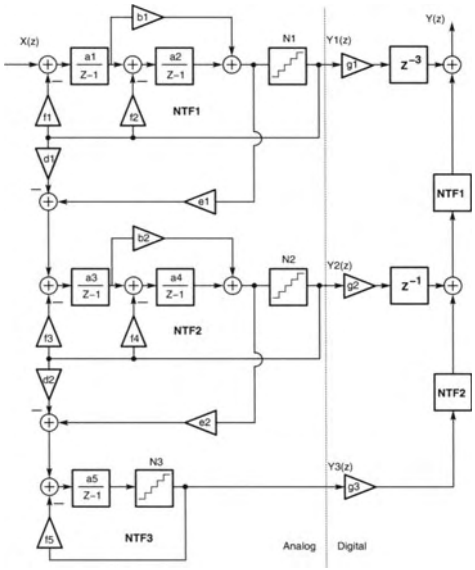

Figure 11: Fifth-order, 3-loop cascade ΣΔ ADC

Considering the non-0dBR OVL shown by all the loops in the cascade, the coefficients d_1, e_1 and d_2, e_2 are not unity in real designs. The coefficients g_2 and g_3 are sized depending of d_1, e_1, d_2 and e_2. In straightforward designs (no scaling of quantizer input in any loop) $d_1 = e_1$ and $d_2 = e_2$, so

$$g_2 = \frac{1}{d_1} \; g_3 = \frac{1}{d_1 d_2} \tag{16}$$

g_1 is only different from unity if there are differences in the reference level of the first and the subsequent loops.

4. Discrete-Time Circuits

4.1. Switched-Capacitor Summing Integrator

The most widely used DT integrator is the *switched-capacitor* integrator, shown in Fig. 12 in its differential, summing version. It consists of an opamp connected in closed-loop with the *integration capacitors Ci*, which are used to accumulate charge, thus performing the low-pass function. For half the clock period (*sampling phase*) the input signal is sampled on the *sampling capacitors Cs* by closing the switches *s* and keeping the switches *i* open. During the next half clock period, the switches *s* are open and the switches *i* are closed, thus connecting *Cs* to the charge-transfer nodes that are the opamp inputs. Because during this *integrating phase* the sampling capacitors *Cs* are connected between ground and the virtual

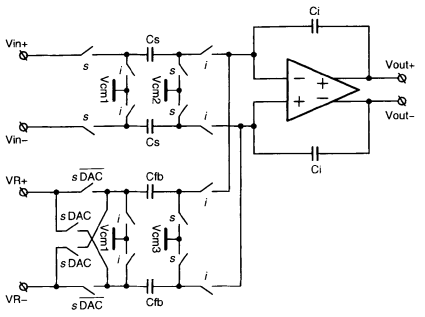

Figure 12: Summing SC integrator with two integration paths

ground nodes (held at virtual ground by the large opamp gain), all the charge stored in *Cs* is added to the charge of *Ci*, modifying the output voltage accordingly. The transfer function can be written in Z-domain, considering *VR+*=*VR-*, as

$$H_{SC}(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{C_s}{C_i} \frac{z^{-1}}{1 - z^{-1}} \tag{17}$$

A similar transfer function can be written from the *VR* input to the output. Hence the integrator coefficient, important for the mapping of the loop filter to the designed topology, is given by the ratio of the two capacitors. This is convenient from the point of view of yield optimization due to a relative mismatch of on-chip capacitors as low as 0.1% for a good layout.

The integrator in Fig. 12 completely separates the integration paths for the input signal and for the DAC reference voltage. Furthermore, the switching at the *VR* nodes is signal-independent, and so is the switching at the opamp's inputs, reducing harmonic distortion. The only signal-dependent switching is introduced by the use of physically different switches at the *VR* nodes, but this has minimal effects due to their connection to low-impedance nodes. The noise power (referred to the input of the integrator) introduced inside the signal bandwidth by this switching scheme is

$$P_{BWnoise} = \frac{4kT}{C_s OSR} \left(1 + \frac{C_{fb}}{C_s}\right). \tag{18}$$

The circuit described above implements a DT integrator transfer function only if circuit non-idealities are neglected. But even if these non-idealities alter the function implemented in the final circuits, their effects on the overall conversion performance can be reduced by correct design of circuit components and signals.

4.1.1. Finite, Nonlinear Amplifier Gain

Amplifiers designed in CMOS processes suffer especially from a low value of the DC gain caused by reduced output impedance of MOS transistors. This affects the transfer function of the SC integrator by an incomplete discharge of the sampling and DAC capacitors, *Cs* and *Cfb* in Fig. 12, during the integration phase. The input capacitance of the opamp also becomes important in high-speed CMOS processes. With the input capacitance of the opamp *Cp*, a more accurate expression of the integrator's output at the end of the integration phase can be calculated:

$$V_{out} = \frac{z^{-1}\left(V_{in}C_s + V_R C_{fb}\right)}{C_i\left(\left(1+\frac{1}{A_{DC}}\frac{C_i+C_s+C_{fb}+C_p}{C_i}\right) - z^{-1}\left(1+\frac{1}{A_{DC}}\frac{C_i+C_p}{C_i}\right)\right)}. \tag{19}$$

This expression can be placed in time-domain simulations of ΣΔ ADCs to show the impact of the finite amplifier DC gain on the conversion performance. Since Eq. 19 shows that a real integrator introduces both a gain and a pole error compared to the ideal integrator in Eq. 17, the finite amplifier DC gain affects the NTF characteristic and therefore decreases the DR.

Traditionally, is said that gain linearity is not important in SC integrators. This is true as long as the DC gain of the amplifier is large enough to keep a low voltage at its inputs after the integration phase or as long as the gain, even if small, does not vary with the output voltage. Both these assumptions tend to be difficult to attain in high-speed CMOS processes.

4.1.2. Finite Amplifier Bandwidth and Slew-Rate

Switched-capacitor circuits count on fast charge transfer from the sampling and DAC capacitors to the integrating capacitor, and so far, this transfer has been considered to be much faster than the sampling speed. This is only true if the unity-gain frequency of the amplifier (loaded with all the switching capacitors) is extremely large compared to the sampling frequency, which is almost never the case. In SC circuits, the limited amplifier bandwidth and slew-rate introduce errors at each integration and sampling phase, in the form of harmonic distortion. In practical circuits the amplifier bandwidth is minimized to reduce power consumption, and the lower limit is set by the total harmonic distortion which can be introduced by the integrator. The distortion introduced by each integrator has to be analyzed separately and considering the associated loop gain.

Settling errors are introduced both during sampling and integrating phases. In designs with static biasing and clocked with 50% duty cycle, the capacitive load of the amplifier during the integration phase is always larger than the load during the sampling phase so the former phase (which constitutes the worst case) must be analyzed to determine the settling properties of the integrator.

4.2. Power Consumption Analysis

The transconductance of the opamp inside a SC integrator is a good model of the power consumption of the integrator, especially if the amplifier is a one-stage design. Starting from the noise budget available for the integrator, one can calculate the capacitors building the $\Sigma\Delta$ coefficients. With the capacitor values and the distortion requirements (translated in settling constraints), the g_m of the opamp's input stage can be calculated.

4.2.1. Noise

The noise budget allocated to each integrator (based on designer expertise or by CAD) is consumed by two components: the switch noise (kT/C noise) and the opamp noise. For a one-stage amplifier with a large input transconductance g_m, the noise power depends only on the capacitive load

$$P_{n_{amp}} = \frac{2kT\gamma}{C_{cl}} \tag{20}$$

with γ the noise enhancement factor for short-channel transistors [3] (applicable for opamp input devices). The total noise power (wide-band) at the input of the SC integrator is

$$P_n = 4KT\left(\frac{1}{C_s}\left(1+\frac{C_{fb}}{C_s}\right)+\frac{\gamma}{2C_{cl}}\right) \tag{21}$$

with

$$C_{cl} = C_s + C_p + C_{fb} + C_l + \frac{C_l(C_s + C_p + C_{fb})}{C_i} \tag{22}$$

where C_l is a fraction of the integration capacitor (parasitic capacitance of C_i) connected at the opamp's output

$$C_l = \alpha C_i \tag{23}$$

with α a technology-dependent percentage. C_p is also proportional to C_i (for a given $V_{gs} - V_T$ and UGB):

$$C_p = \eta C_i. \tag{24}$$

The C_s and C_{fb} capacitors are related to the integration capacitor through the $\Sigma\Delta$ loop coefficients supplied by the architecture design (see Fig. 9)

$$C_s = aC_i,\ C_{fb} = afC_i \tag{25}$$

and using these proportionalities the load capacitance can be written as a function of the integration capacitor, technology parameters and $\Sigma\Delta$ loop coefficients

$$C_{cl} = C_i\left((a + af + \eta)(1 + \alpha) + \alpha\right). \tag{26}$$

Combining the expression of the noise power with the compact expression of the load capacitance, an expression of the integration capacitor as a function of the noise budget of the integrator can be written

$$C_i = \frac{4KT}{P_n}\left(\frac{1}{a}(1+f) + \frac{\gamma}{2\left((a+af+\eta)(1+\alpha)+\alpha\right)}\right). \tag{27}$$

As part of the total noise budget (allocated for the entire converter), the noise power inside the signal bandwidth is referred at the input of the $\Sigma\Delta$ converter using Eq. 13.

4.2.2. Distortion

Starting from a specification of harmonic distortion $|HD_3|$ (only the third one since differential circuits are used), the linearity of the integrator can be expressed in bits as [14]

$$B \approx \frac{|HD_3| \ [dBc]}{6}. \tag{28}$$

The number of bits B is then used to calculate the number of time constants required by a single-pole system to settle to B bits [14]

$$N_\tau = Bln(2) \tag{29}$$

which, for a settling time T_{settle} requires an UGB

$$UGB = \frac{N_\tau}{T_{settle}}. \tag{30}$$

The concept of the single-pole system is true for single-stage amplifiers and is also a good approximation of the behavior of two-stage amplifiers with enough phase margin.

4.2.3. Required OpAmp Transconductance

The g_m is then calculated from the required UGB, as

$$g_m = 2\pi C_{cl} UGB = 2\pi C_{cl}\frac{N_\tau}{T_{settle}} \tag{31}$$

For a slewing followed by settling model [3] the time available for settling is

$$T_{settle} = \frac{T_{CLK}}{2} - T_{slew} \tag{32}$$

with T_{slew} being the time needed for the opamp to recover from non-linear behavior. Hence, the expression of g_m results in

$$g_m = \frac{2\pi C_{cl}\left(N_\tau - 1\right)}{\frac{T_{CLK}}{2} - V_f^+\frac{C_{cl}}{I_0}} \tag{33}$$

where I_0 is the biasing current (tail current) of the opamp MOS input pair and V_f^+ is the voltage at the input of the opamp at the beginning of the integration phase, and after passive charge re-distribution [3].

If MOS transistors operated in weak inversion are used in the input stage of the opamp, $g_m = 10I_0$, and a compact expression for g_m is obtained

$$g_m = \frac{4\pi C_{cl}}{T_{CLK}} \left((N_\tau - 1) + 10V_f^+ \right). \tag{34}$$

5. Continuous-Time Circuits

5.1. Integrator Topology

A fully-differential active-RC integrator for use in ΣΔ ADC design is shown in Fig. 13. Apart from the input signal path, *Vin* with V/I conversion performed by *Ri*, there is a second path which implements the ΣΔ DAC, in this case only one-bit, with the pair of resistors *Rdac*. The current from both paths is integrated on *Ci*. The opamp keeps a null voltage difference between its inputs, hence the integrated current is

$$I_{Ci} = \frac{V_{in}^+ - V_{in}^-}{2R_i} \pm \frac{V_{ref}^+ - V_{ref}^-}{2R_{dac}} \tag{35}$$

The sign of the summation is decided based on the decision of the ΣΔ quantizer, represented in the schematic by the logic bit *B0*. If the decision *B0* is logic-High, it means the output of the integrator is too large and *Vref* is switched to reduce the output voltage.

The noise power at the input of the integrator is given by the input and DAC resistors and the g_m of the opamp's first stage

$$P_{CTnoise} = 8kTBW(R_i + \frac{R_i^2}{R_{dac}} + \frac{\gamma}{4g_m}) \tag{36}$$

As opposed to SC integrators, there is no noise aliasing since no noise sampling is taking place.

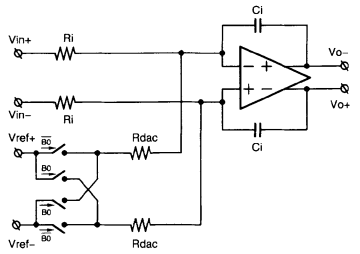

Figure 13: Active RC integrator with DAC resistors

The integrator using DAC resistors can be extended for multi-bit DACs by adding DAC paths, independently connected to the same *Vref*.

5.2. Effects of Circuit Non-Idealities

In comparison with a switched-capacitor (SC) integrator, the only active element in a CT integrator with resistive DAC is the operational amplifier. In such integrator topologies the opamp is the circuit element limiting integrator's performance, assuming highly linear on-chip passive components are available.

5.2.1. Finite, Nonlinear Opamp Gain

The finite gain of the opamp used inside the CT integrator affects the transfer function of the integrator, in a similar manner as in the case of SC integrators. Yet its effect is different in the CT integrator. The transfer function of the integrator with an opamp exhibiting finite DC gain is

$$H(s)^{A_{DC}} = \frac{1}{\frac{1}{A_{DC}} + sR_iC_i} \tag{37}$$

for a finite opamp DC gain of A_{DC}. This equation shows that both the DC gain of the integrator and its pole are affected by the finite DC gain of the amplifier. These changes in integrator transfer functions are expected to cause loss of $\Sigma\Delta$ conversion performance mainly in terms of resolution, by introducing changes in the designed NTF likely to increase quantization noise inside the signal bandwidth.

5.2.2. Finite, Nonlinear OpAmp Transconductance

With a voltage input, the active-RC CT integrator still integrates a *current*. The major non-linearity, analyzed here, is introduced by opamp's finite and strongly nonlinear transconductance g_m. A simplified model of a single-stage amplifier can be used for this analysis, yielding results that can also be applied to more complex opamp designs by replacing the g_m in this model with the equivalent g_m of a multi-stage, correctly-compensated (approximately single-pole behavior) amplifier.

5.2.3. Finite Opamp Bandwidth and Slew-Rate

Compared to SC integrators, the finite bandwidth of the amplifier in a CT integrator does not affect the linearity of the integration but the in-band quantization noise power by changing the NTF shape. For a single-pole opamp with a unity-gain bandwidth of ω_0 and DC voltage gain A_{DC}, the frequency-dependent voltage

gain $A(s)$ can be used in Eq. 37 to find the transfer function of a CT integrator containing the bandwidth-limited opamp

$$H(s)^{GBW} = \frac{1}{\frac{1}{A(s)} + sR_iC_i} = \frac{1}{\frac{1}{A_{DC}} + s\left(\frac{1}{\omega_0} + R_iC_i\right)} \tag{38}$$

The equation above shows that, in order to have a good approximation of the ideal integrator function,

$$H(s)^{ideal} = \frac{1}{sR_iC_i} \tag{39}$$

not only the DC gain A_{DC} should be much larger than $1/\left|sR_iCi\right|$, but also the unity-gain bandwidth of the opamp should be much higher than the unity-gain bandwidth of the integrator

$$\omega_0 \gg \frac{1}{R_iC_i} \tag{40}$$

To compare the result in the equation above with the sampling frequency f_{CLK} of the $\Sigma\Delta$ ADC, the value of the loop coefficient associated with the integrator should be used

$$a_i = \frac{1}{R_iC_if_{CLK}} \tag{41}$$

For typical a_i values of 0.1 to 0.3 results that

$$\omega_0 \geq f_{CLK} \cdots 3f_{CLK} \tag{42}$$

The exact value depends on the overall tolerance to in-band noise leakage and it scales with the fill factor for a return-to-zero (RTZ) DAC shape, that changes the $1/R_{dac}C_i$ to $\delta/R_{dac}C_i$, with δ the RTZ fill factor.

The second issue associated with a limited opamp bias current is the slewing of the amplifier's output stage. Since the signal processed is the integrated current, a limitation of this signal would introduce distortion in the overall A/D conversion. Therefore, a hard limit can be found for the biasing current of the output stage of the opamp as the peak of the integrated current during nominal operation of the $\Sigma\Delta$ ADC. This is usually not a very restrictive limit.

5.3. Power Consumption Analysis

A good estimate of the CT integrator's power consumption can be obtained from the required opamp transconductance. For each integrator in a $\Sigma\Delta$ ADC, the input and DAC resistors, as well as the integration capacitor, are calculated from the noise budged of the integrator and its associated loop coefficients. The values of the passive components are in turn used to calculate the opamp's g_m required to keep the distortion lower than the limit allocated to the integrator. The integrator is assumed to be a active-RC, fully differential design with both input and DAC resistive paths, as shown in Fig. 13.

5.3.1. Noise Performance

For the differential CT integrator in Fig. 13 the noise budget is distributed among the two pairs of resistors R_i and R_{dac}, and the operational amplifier's transconductance g_m, resulting (Eq. 36), for a signal bandwidth *BW*,

$$P_{CTnoise} = 8kTBW(R_i + \frac{R_i^2}{R_{dac}} + \frac{\gamma}{4g_m}) \tag{43}$$

The equation above can be written in a more compact form if the expressions connecting the $\Sigma\Delta$ loop coefficients with the passive circuit components are used (see Fig. 9)

$$a = \frac{1}{R_i C_i f_{CK}},\ f = \frac{R_i}{R_{dac}} \tag{44}$$

to write $P_{CTnoise}$ only as function of C_i and R_i

$$P_{CTnoise} = \frac{8kTBW}{aC_i f_{CK}} \left(1 + f + \frac{\gamma}{4g_m R_i}\right) \tag{45}$$

To quickly estimate C_i, the last term of the equation above can be ignored or be allocated a (small) fraction of the noise budget. Knowing C_i, the resistors can be calculated and used to calculate g_m from the distortion specification. Alternatively, an optimized set of circuit parameters can be calculated if first the distortion specification is used to extract an expression for the $g_m R_i$ product, free from other circuit parameters.

5.3.2. Distortion Performance

Assuming the opamp has a large g_m [2], third-order harmonic distortion is given by the amplitude of the input signal V_A, the nonlinear component of the opamp transconductance g_3, and the equivalent resistor connected at the input of the opamp, R,

$$\frac{1}{R} = \frac{1}{R_i} + \frac{1}{R_{dac}},\ HD_3 = \frac{V_A^2}{24 g_3 R^3} \tag{46}$$

the distortion results to only depend on the non-linear component of the opamp's transconductance, g_3. The expression of g_3 is calculated as the third derivative of the residual input voltage which, for a MOS input pair with transistors sized W/L in strong inversion, is

$$V_r^{SI} = \sqrt{\frac{I_b}{2K_P W/L}} \left(\sqrt{1 + \frac{I_i}{I_b}} - \sqrt{1 - \frac{I_i}{I_b}}\right) \tag{47}$$

while, for weak inversion transistors, it is

$$V_r^{WI} = nV_T ln\left(\frac{I_b + I_i}{I_b - I_i}\right) \tag{48}$$

Derivatives of these expressions yield the transconductance components g_m and g_3. Considering the expression of R, the third harmonic distortion becomes, for strong inversion transistors,

$$HD_3^{SI} = \frac{V_A^2 V_{gt}}{32 R_i^3 I_b^3} \left(1 + \frac{R_i}{R_{dac}}\right) \tag{49}$$

and, respectively, for weak inversion,

$$HD_3^{WI} = \frac{V_A^2 n V_T}{6 R_i^3 I_b^3} \left(1 + \frac{R_i}{R_{dac}}\right) \tag{50}$$

5.3.3. Required OpAmp Transconductance

From the equations above and using Eqs. 44, a compact expression of the required g_m for transistors in strong inversion

$$g_m^{SI} = \frac{1}{R_i} \sqrt[3]{\frac{V_A^2 (1+f)}{32 V_{gt}^2 HD_3}} \tag{51}$$

and, respectively, for weak inversion

$$g_m^{WI} = \frac{1}{R_i} \sqrt[3]{\frac{V_A^2 (1+f)}{48 n^2 V_T^2 HD_3}} \tag{52}$$

Both expressions yield a value for the product $g_m R_I$ which is free of other design parameters

$$g_m = \frac{K_{gm}}{R_i} \tag{53}$$

The factor K_{gm} can be calculated before the optimization of each integrator takes place, from $\Sigma\Delta$ loop coefficients, performance requirements, MOS transistor parameters, and a design decision for V_{gt} when strong inversion is used.

With K_{gm}, the integration capacitor C_i can be calculated from the noise budget

$$C_i = \frac{8kTBW}{a P_{CTnoise} f_{CK}} \left(1 + f + \frac{\gamma}{4K_{gm}}\right) \tag{54}$$

and, using Eq. 44, the resistors R_i and R_{dac} are calculated. With R_i, g_m is calculated from Eq. 53 or directly from Eqs. 51 and 52.

6. Computer-Aided Design of Sigma-Delta ADCs

Since no accurate analytical model is available for $\Sigma\Delta$ ADCs in general, there is need to simulate different possible solutions before deciding which one has the

potential to be the optimal one. This Section presents a systematic procedure to exhaustively explore the design space of ΣΔ ADCs, by automatically designing and evaluating a large number of candidate solutions based on behavioral simulations. Two design examples are also shown, to illustrate the advantages and limitations of this procedure.

6.1. Filter-Level Design

A fast design space exploration is performed at filter-level, using a linearized model of the ΣΔ ADC. The goal of this search is to quickly evaluate all solutions in the design space and select only candidates that can attain the target dynamic range (DR). The search algorithm is shown in Fig. 14. The entire ΣΔ ADC design space is split in two sub-spaces, the *topology* sub-space and the *parameter* sub-space. The *topology* design sub-space is defined by the *ORDER*, number of cascaded *LOOPS* and number of *BITS*, while the *parameter* design sub-space is defined by the oversampling ratio *OSR* and peak *NTF* (noise transfer function) magnitude. Multiple *parameter* sub-space elements can be associated with every *topology* sub-space element, changing the performance of the final solution while keeping a fixed physical implementation. All dimensions of the search space are browsed using constant stepping, linearly in *topology* space and exponentially in *parameter* space.

At each step a set of two filter transfer functions are generated, the NTF and the signal transfer function (STF). Filter generation can also optimize in-band

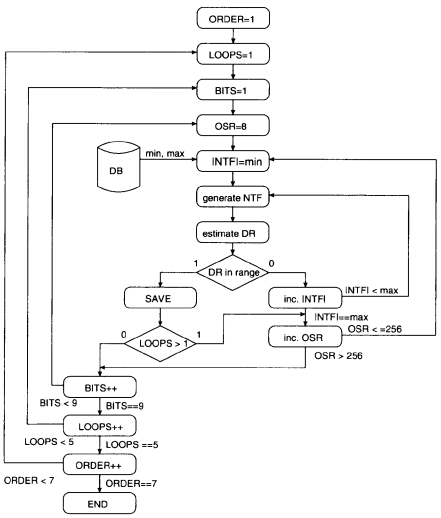

Figure 14: Filter-level exploration algorithm

zeros for the NTF (to reduce total in-band noise power [4]) and off-band zeros for the STF (to reduce in-band gain ripple and increase off-band rejection). After the two filter transfer functions are generated the in-band noise power is estimated to find the DR. A test is applied with two thresholds derived from the target DR (in dB)

$$DR_{target} + DR_{lower} \leq DR \leq DR_{target} + DR_{upper} \tag{55}$$

The lower limit tests if, after the circuit (white) noise is added, the converter still reaches the final target DR. The upper limit is set to reject power-hungry solutions which offer more quantization-noise DR than actually needed. If the test is passed, the solution is saved in a database.

For single-loop solutions the algorithm stops when a combination of minimal *OSR* and *NTF* is found. For cascaded designs however, because significant architectural details are not available at the filter level, the algorithm continues searching for solutions even after finding the first valid one. This insures that no valid solution is prematurely rejected.

The limits within which *NTF* is browsed are decided based on a database stored on disk containing, for each set of (*ORDER*, *BITS*), the value of the overloading level. This database is built by applying the entire design procedure explained in this section (both filter-level and architecture-level design) to the entire *topology* design sub-space with the *LOOPS* constrained to 1 (OVL of cascaded solution is ultimately decided by the a single loop). In the *parameter* sub-space, *NTF* is sampled in a wide range while *OSR* is set to 64, because *OSR* does not affect the overloading level. The use of the NTF database results drastically reduces run-time because the solutions considered as possible candidates are actually guaranteed to yield stable $\Sigma\Delta$ loops.

6.1.1. NTF Database

The one performance parameter of $\Sigma\Delta$ ADCs that cannot be predicted accurately by linear modeling is the overloading level (OVL) [1]. In the algorithm presented here, the overloading levels for each single-loop $\Sigma\Delta$ ADC are computed once from time-domain simulations and stored in a database. The peak magnitude of NTF is varied in a wide range. Each single-loop $\Sigma\Delta$ ADC is designed and optimized in a range of input signal values for each NTF peak magnitude. The overloading level is detected as the input signal which causes integrator clipping.

Fig. 15 shows the entry in the peak NTF database for the single-bit, fourth-order $\Sigma\Delta$ ADC. It shows the variation of overloading level *OVL*, peak output of the last integrator *Out4* and the peak *SNDR* in the NTF range where the loop can be stabilized. The decision that the loop can be stabilized is taken by comparing the values of integrator coefficients against a bottom value. If all integrator coefficients are larger than the bottom value and integrator outputs are smaller than

the V_{clip} value, the loop can be designed stable and there exists a dB-negative overloading level.

Because of this tight relationship between the *OVL* value and the ratio of the clipping voltage over reference voltage, the database has to be generated for each different ratio of V_{clip}/V_{Ref}. The same database can be used for any target DR (SNDR) design as long as the V_{clip}/V_{Ref} ratio does not change.

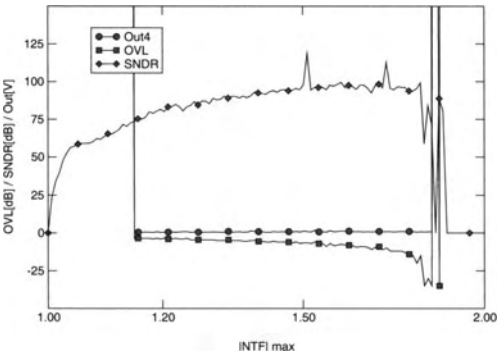

Figure 15: Peak NTF magnitude database entry example

6.1.2. Dynamic Range Estimation

A fast yet accurate method to estimate the DR is used. It overcomes the drawbacks of both time-domain simulations, which are slow, and classical DR estimation using a formula which is inaccurate especially for high-order $\Sigma\Delta$ loops [1]:

$$DR = \frac{3}{2}\frac{2L+1}{\pi^{2L}} OSR^{2L+1}(2^B - 1)^2 \tag{56}$$

First the magnitude of NTF is calculated in *n* points equally spaced from DC to $f_s/2$ from its polynomial form, in Z domain. Considering the total power of quantization noise [1] if the quantizer step is Δ, the (white) quantization noise amplitude in each bin *i* from DC to $f_s/2$ (from 0 to *n*), referred to $V_{ref} = \Delta(2^{B-1})/2$, is

$$S_{qn,Bbit} = 20log_{10}\left(\sqrt{\frac{2}{3n}}\right) - 20(B-1)log_{10}(2)\ [dBR] \tag{57}$$

if the quantizer has *B* bits.

The value of the NTF magnitude, expressed in dB, is added to the value of $S_{qn,Bbit}$ and a curve showing the quantization noise amplitude in each bin is drawn. Its integral in the band of interest yields the estimated DR value. Fig. 16 shows the estimated (*left*) and time-domain simulated (*right*) spectrum of the

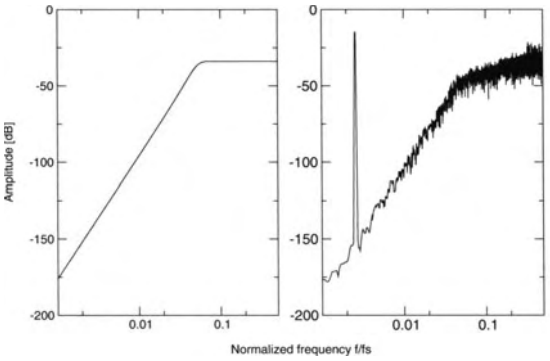

*Figure 16: Estimated (*left*) vs. time-domain simulated (*right*) noise shaping*

output of a fourth-order, one-bit, single-loop $\Sigma\Delta$ ADC. The two graphs show the good accuracy of this estimation method for high-order loops. An extended comparison between the classical formula and the polynomial estimation method applied to single-loop $\Sigma\Delta$ ADCs shows that the estimation error is always less than 4dB, as opposed to the error yielded by calculating the DR using the classical formula which can be comparable to the target DR itself. The polynomial estimation method also works better than the calculation for cascaded loops.

6.2. Architecture-Level Design

The architecture-level exploration algorithm evaluates the performance of the filter-level solutions mapped on a specific architecture, as shown in Fig. 17. If a single-loop solution is processed, an architecture is generated with the feedforward and feedback connectivity specified by the user. An initial set of coefficients are then calculated and simulations are performed with a wide range of input signal amplitudes to determine the OVL. Because the initial set of coefficients are not optimized they can cause premature overloading if integrator clipping to the supply rails is simulated. Therefore, for these simulations the clipping voltage is considered to be many times larger than the actual value. Since the reference voltage remains the same, this simulation setup is equivalent to using no-clipping integrator outputs. Single-tone input signals produce frequency-dependent OVL values, so the input signal applied at this design stage is a pulse, a good approximation of a busy signal [1] which produces a frequency-independent OVL.

The next step is the coefficient optimization, performed at the OVL previously detected by observing the peak output of each integrator and by correcting the associated loop coefficient accordingly. The SNDR and DR variations as a function of the input signal are then simulated using a sine input signal. The two curves are tested for performance and passing solutions are saved for further processing.

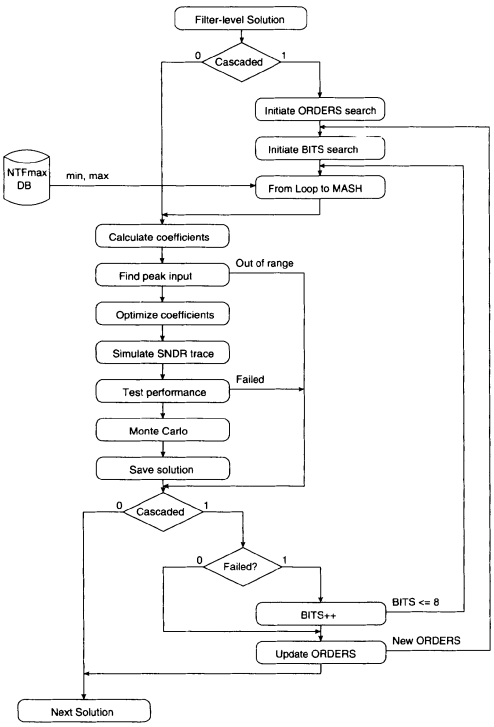

Figure 17: Architecture-level design space exploration

For the cascaded $\Sigma\Delta$ ADCs the only architectural details predefined at filter level are the number of loops and the number of bits in the last loop. Therefore, the filter orders of individual cascaded loops are generated as one additional design space dimension named *ORDERS* in Fig. 17. Another new design space dimension is the number of *BITS* in the first loop of the cascade. For simplicity, the last $n-1$ loops in a cascade of n loops have the same number of bits as the last one. Each derivative of the input solution in the extended design space is analyzed as a possible solution. The architectural derivative is built starting from the parameters supplied in the filter-level solution, namely the peak NTF and the number of quantizer bits for the last loop in the cascade. The peak NTF in the filter-level solution is the product of peak NTF values in each loop.

The generation of a cascaded design architecture consists of finding the $|NTF|$ value that yields stable NTFs for all the loops in the cascade, considering their individual order and quantizer bits. The individual orders and quantizer bits are set at this stage by the filter-level solution and the *ORDERS* and first quantizer *BITS* design parameters, so the range of common stable NTFs is found by performing a *logical-AND* between the stable ranges of each loop in the cascade, as extracted

from the peak NTF database. There are cases when the *logical-AND* yields a null range and the architectural derivative is then dropped. Each individual loop in the cascade is then designed following the procedure described for single-loop solutions. The coefficients connecting the loops are derived from corresponding loop coefficients [6].

6.2.1. Performance Test

Performance testing is based on statistics of SNDR and DR curves as functions of input signal level. Linear regressions are performed on each curve, from SNDR zero-crossing to the overloading level. The slope of SNDR is tested to be close enough of the desired conversion gain (typically unity). A slope outside this range shows a strong dependency of quantization noise power of the input signal level, which is not desired. The intercept of the DR curve is then tested against the target DR value to insure the target DR is attained in the worst condition. Finally, the peak regression residual of the DR curve is tested to be lower than 6dB (1 bit) to insure the required integral non-linearity (INL).

$SNDR(V_{in})$ and $DR(V_{in})$ curves for an architecture rejected by performance test algorithm are shown in Fig. 18. The dotted lines are the linear regression fitted values for both simulated curves. The drop in DR at high input levels (larger than -20dB) shows that the NTF aggressiveness needed to reach the target DR is too high [4]. The peak SNDR which still keeps a good overall INL is about 85dB instead of almost 95dB, as shown by its absolute peak value. Based on the fact that the decrease in peak SNDR already disqualifies this solution, the simple yet effective criterion of peak regression residual limiting is used as rejection criterion. The slope of DR fitted line shows that the test for DR intercept works toward rejecting the solution as well, even if peak regression residual would be passing its test. The test for SNDR slope also works toward rejecting

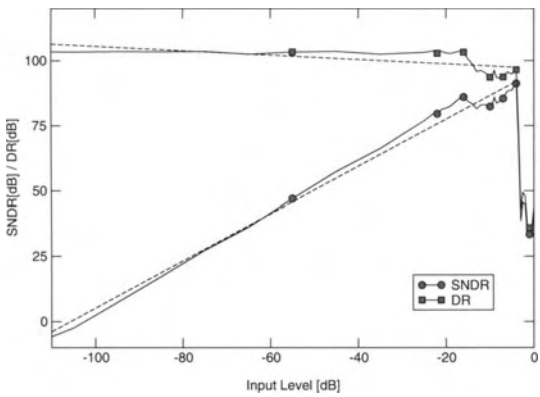

Figure 18: SNDR and DR curves for a rejected architecture

the solution.

6.2.2. Estimation of Power Consumption

Each integrator in the loop has its power consumption characterized by the g_m of the operational amplifier insuring the required integration linearity. To calculate the total g_m for a designed architecture-level solution, the passive components (resistors and capacitors) in each integrator have to be calculated from the noise budget and placed in the power models developed in previous Sections for SC and CT circuits respectively.

The noise budget of each integrator is allocated based on evaluation of total power consumption as a function of noise budget distribution across the converter. A part R of the noise power of the previous integrator is allocated to the next in the loop

$$(P_n)_i = R\,(P_n)_{i-1} \tag{58}$$

and the value of R is chosen to minimize total power consumption. Up to 25% reduction in current consumption by optimization of R has been observed on practical designs.

6.2.3. Yield Analysis and Optimization

From the accepted solutions, a top-ten set is chosen based on the ratio of peak SNDR and the power consumption in opamps measured by the total g_m. For each top-ten solution, a Monte-Carlo analysis varies the $\Sigma\Delta$ ADC coefficients using a normal distribution with the standard error supplied by the user. The user can also specify a spread 3σ value along with the coefficient-to-coefficient mismatch 3σ value. The spread is used in the case of CT designs to simulate the effect of RC product spread over design performance. A few hundreds Monte-Carlo simulation steps are run for the top-ten solutions and the performance tests are applied. The single-loop solutions can be designed from the early stages to give 100% yield with relaxed matching requirements by controlling the difference between the quantization noise power and in-band white noise power. For cascaded solutions however, the yield can be corrected by increasing the number of bits in the first loop. This decreases the quantization noise power in the first loop and therefore the power of the mismatch-induced, low-order shaped noise leaking to the output. When the yield is lower than 90% the number of bits in the first loop in the cascade is increased and another Monte-Carlo yield analysis is started.

6.3. Design Examples

Two examples are presented to show the effectiveness of global optimization through exhaustive design-space exploration. The first one is an audio $\Sigma\Delta$ ADC

powered at 1.5V with rail-to-rail input and 1.5V reference voltage. A designed circuit has been reported [17] which consumes 0.95mW for a DR of 98dB and peak SNDR of 89dB at a signal bandwidth of 20kHz. The second one is an ADC for xDSL applications, powered at 2.5V, also with rail-to-rail input and reference voltage equal to the supply voltage. The signal bandwidth is 2MHz. A design has been reported which consumes 90mW in the analog circuits to attain 95dB DR and 90dB peak SNDR.

The designs mentioned above are state-of-the art examples. The results presented here show that other architectures can offer better peak SNDR versus supply power consumption ratios (here used as figure of merit FOM) but these designs are still among the best options.

6.3.1. Audio Sigma-Delta ADC

The search for an optimal audio $\Sigma\Delta$ has been first performed in the entire design space, to find the global optimum. The global optimization results are shown in Table 1. It is worth noting the massive presence of cascaded solutions. The column *LOOPS* shows each cascaded loop's order in parentheses, while the column *BITS* contains the number of bits in the first loop in parentheses. The solutions have virtually the same figure-of-merit *FOM*. All solutions have OSR=32 and a large number of bits in the first loop, which increases the FOM value by increasing the overloading level with no additional power costs (in the power model used here).

Table 1: Global solutions for Audio $\Sigma\Delta$ ADC

ORDER	LOOPS	BITS	OSR	SNDR	FOM
4	2 (2-2)	2 (6)	32	97.5	119.8
4	3 (2-1-1)	2 (5)	32	97.3	119.5
5	3 (2-1-2)	1 (7)	32	98.5	120.2
5	2 (2-3)	4 (7)	32	98.5	119.8
5	2 (2-3)	5 (7)	32	98.1	119.5

Table 2 contains the optimization results for a set of solutions restricted by the number of loops (LOOPS=1). The best solution is the third order, 4-bit loop, again working at OSR=32. This solution is also remarkable by its low number of bits compared to the other top performers.

Further design space restriction to 1-bit single-loop architectures yields only the state-of-the-art fourth-order, single-loop solution with OSR=64 reported in [17]. The solution is chosen from a set of four possible, three of which do not pass the yield test.

Table 2: Audio ADCs with LOOPS=1

ORDER	BITS	OSR	SNDR	FOM
3	6	16	95.3	117.6
3	8	16	96.3	117.8
3	4	32	95.5	118.4
4	8	8	95.6	116.4
4	5	16	96.0	117.8
5	4	16	95.4	116.5
5	6	16	96.2	115.9

6.3.2. Delta-Sigma ADC for xDSL Applications

The results of global optimization for a 4MS/s $\Sigma\Delta$ ADC are shown in Table 3. Again a third-order solution with OSR=32 and 4-bits quantizer has good performance, but most of the solutions operate at 16 times oversampling. They also have large number of bits in the (first loop) quantizer to attain high overloading levels.

Table 3: Global solutions for xDSL $\Sigma\Delta$ ADC

ORDER	LOOPS	BITS	OSR	SNDR	FOM
3	1	4	32	96.5	102.7
4	2 (2-2)	4 (8)	16	97.4	103.1
4	3 (2-1-1)	4 (7)	16	98.1	102.7
5	2 (2-3)	3 (8)	16	96.6	102.1
5	2 (2-3)	4 (6)	32	97.1	101.7
6	3 (2-2-2)	2 (8)	16	97.4	102.6

To avoid solutions like the ones requiring 32 times OSR, the search space is limited, by (ORDER=5, OSR=16). Furthermore, the maximal number of bits can be limited, for example to 6, to keep a low DAC complexity. The solutions for this search are shown in Table 4. They are all cascaded $\Sigma\Delta$ ADCs except two which, even with their low-FOM, can be good choices for low-voltage, mismatch-tolerant designs. The best are the three-loops with a 2-2-1 configuration. The state-of-the-art solution reported so in [15] is among them. During initial optimization stages, only 3 bits were needed in the first loop, but yield optimization reached the 5-bit solution reported in [15], the increase being needed to accommodate capacitor/capacitor mismatch effects.

Table 4: xDSL ADCs with ORDER=5, OSR=16

LOOPS	BITS	SNDR	FOM
2 (4-1)	2 (5)	93.1	98.0
3 (2-2-1)	2 (6)	97.1	102.6
3 (2-2-1)	3 (5)	95.7	101.0
3 (2-2-1)	4 (6)	97.8	102.5
1	5	96.6	100.4
3 (2-2-1)	5 (5)	98.1	102.6
1	6	96.5	99.6
3 (2-2-1)	6 (6)	98.2	101.7

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