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Circuit for driving a switched-capacitor SAR ADC with a buffered instrumentation amplifier

Art Kay

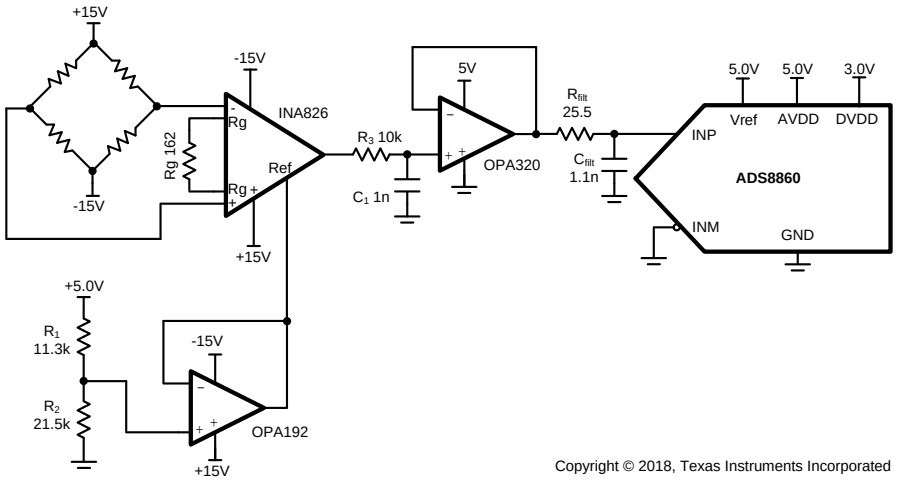
Input	ADC Input	Digital Output ADS8860
–10mV	Out = 0.2V	$0A3D_H$ or 2621_{10}
5mV	Out = 4.8V	$F5C3_H$ or 62915_{10}

Power Supplies					
AVDD	**DVDD**	**V_{ref_INA}**	**V_{ref}**	**V_{cc}**	**V_{ee}**
5.0V	3V	3.277V	5.0V	15V	–15V

Design Description

Instrumentation amplifiers are a common way of translating low-level sensor outputs to high-level signals to drive an ADC. Typically, instrumentation amplifiers are optimized for low noise, low offset, and low drift. Unfortunately, the bandwidth of many instrumentation amplifiers may not be sufficient to achieve good settling to ADC charge kickback at maximum sampling rates. This document shows how a wide-bandwidth buffer can be used with an instrumentation amplifier to achieve good settling at high sampling rates. Furthermore, many instrumentation amplifiers are optimized for high voltage supplies and it may be required to interface the high voltage output (that is, ±15V) to a lower voltage amplifier (for example, 5V). This design shows how a current-limiting resistor can protect the amplifier from electrical overstress in cases where the instrumentation amplifier is outside the input range of the op amp. A related cookbook circuit shows a simplified approach that does not include the wide-bandwidth buffer (*Driving a Switched-Capacitor SAR With an Instrumentation Amplifier*). The simplified approach has limited sampling rate as compared to the buffered design. Note that the following circuit shows a bridge sensor, but this method could be used for a wide range of different sensors.

This circuit implementation is applicable in applications such as *Analog Input Modules*, *Electrocardiogram (ECG)*, *Pulse Oximeters*, *Lab Instrumentation*, and *Control Units for Rail Transport*.



Specifications

Specification	Calculated	Simulated
Sampling rate	1Msps	1Msps, settling to –44µV
Offset (ADC Input)	40µV · 306.7 = 12.27mV	16mV
Offset Drift	(0.4µV/ºC) · 306.7 = 123µV/ºC	N/A
Noise	978µV	586μV_{RMS}

Design Notes

1. The bandwidth of instrumentation amplifiers is typically too low to drive SAR data converters at high data rates (the INA826 bandwidth is 10.4kHz for a gain of 305V/V in this example). Wide bandwidth is needed because the SAR has a switched capacitor input that needs to be charged during each conversion cycle. The OPA320 buffer was added to allow the ADC to run at full data rate (ADS8860 1Msps).
2. Select the gain to achieve an input swing that matches the input range of the ADC. Use the instrumentation amplifier reference pin to shift the signal offset to match the input range. This is covered in the *component selection* section.
3. The INA826 gain is scaled so that the op amp input voltage levels are inside the normal operating range of the amplifier. However, during power up or when a sensor is disconnected the output may drive to either power supply rail (±15V). The resistor R_3 is used to limit the current . This is covered in the *Overvoltage Protection Filter Between Instrumentation Amplifier and Op Amp* section of this document.
4. The buffer amplifier following the voltage divider is required for driving the reference input of most instrumentation amplifiers. Choose precision resistors and a precision low offset amplifier as the buffer. Refer to *Selecting the right op amp* for more details on this subject.
5. Check the common mode range of the amplifier using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* software tool.
6. Select COG capacitors for C_1, and C_{filt} to minimize distortion.
7. Use 0.1% 20ppm/°C film resistors or better for the gain set resistor R_g. The error and drift of this resistor will directly translate into gain error and gain drift.
8. The *TI Precision Labs – ADCs* training video series methods for selecting the charge bucket circuit R_{filt} and C_{filt}. Refer to *Introduction to SAR ADC Front-End Component Selection* for details on this subject.

Component Selection

1. Find the gain set resistor for the instrumentation amplifier to set the output swing to 0.2V to 4.8V.

$$Gain = \frac{V_{out\_MAX} - V_{out\_MIN}}{V_{in\_MAX} - V_{in\_MIN}} = \frac{4.9V - 0.2V}{5mV - (-10mV)} = 306.7$$

$$Gain = 1 + \frac{49.4k\Omega}{R_g}$$

$$R_g = \frac{49.4k\Omega}{Gain - 1.0} = \frac{49.4k\Omega}{(306.7) - 1.0} = 151.6\Omega \text{ OR } 162\Omega \text{ FOR STANDARD 0.1\% RESISTOR}$$

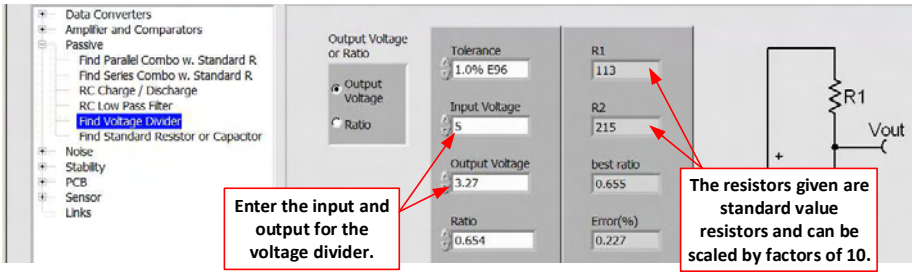
2. Find the INA826 reference voltage (Vref) to shift the output swing to the proper voltage level

$$V_{out} = Gain \cdot V_{in} + V_{ref\_INA}$$

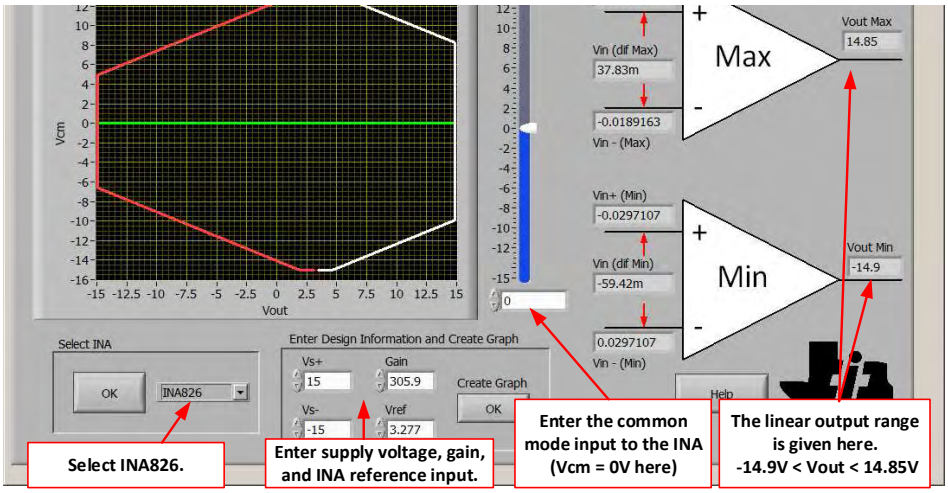
$$V_{ref\_INA} = V_{out} - Gain \cdot V_{in} = 4.8V - \left(1 + \frac{49.4k\Omega}{162\Omega}\right) \cdot (5mV) = 3.27V$$

3. Select standard value resistors to set the INA826 reference voltage (V_{ref_INA} = 3.27V). Use the *Analog Engineer's Calculator* ("Passive\Find Voltage Divider" section) to find standard values for the voltage divider.

$$V_{ref\_INA} = \frac{R_2}{R_1 + R_2} \cdot V_{in\_div} = \frac{21.5k\Omega}{11.3k\Omega + 21.5k\Omega} \cdot (5V) = 3.277V$$

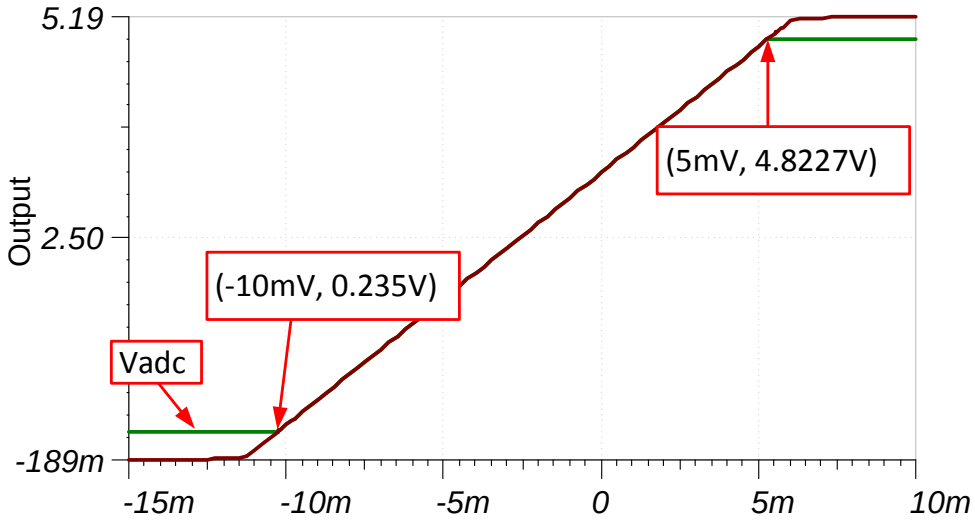


4. Use the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* to determine if the INA826 is violating the common mode range.



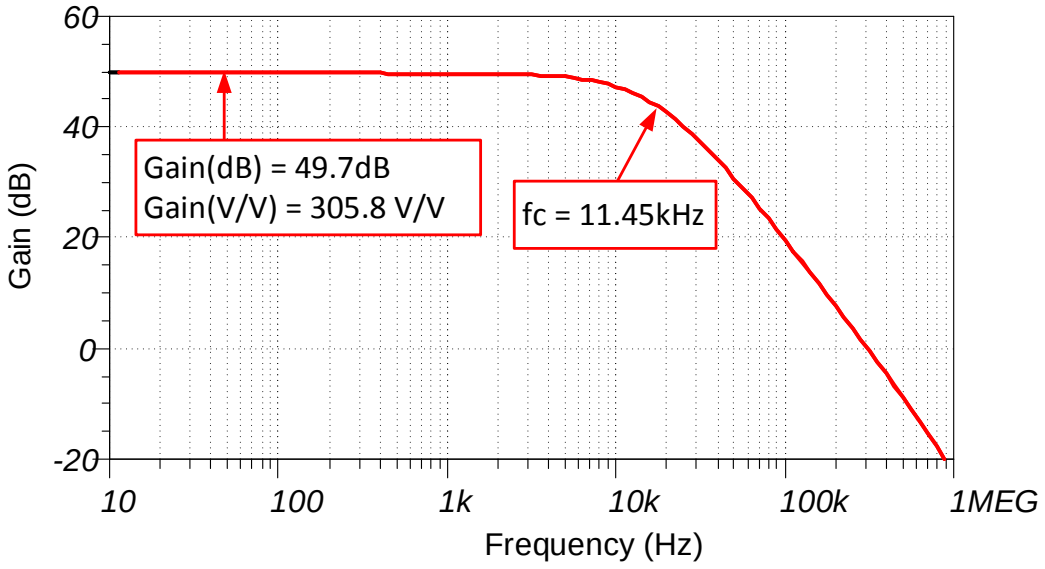
DC Transfer Characteristics

The following graph shows a linear output response for inputs from –5mV to +15mV. Refer to *Determining a SAR ADC's Linear Range when using Instrumentation Amplifiers* for detailed theory on this subject. In cases where the INA826 output exceeds the op amp input range, the ESD diodes turn on and limit the input. The resistor R3 protects the amplifier from damage by limiting the input current (see the *Overvoltage Protection Filter Between Instrumentation Amplifier and Op Amp* section). The op amp output is inside the absolute maximum rating of the ADS8860 (–0.3V < V_{IN} < REF +0.3V).



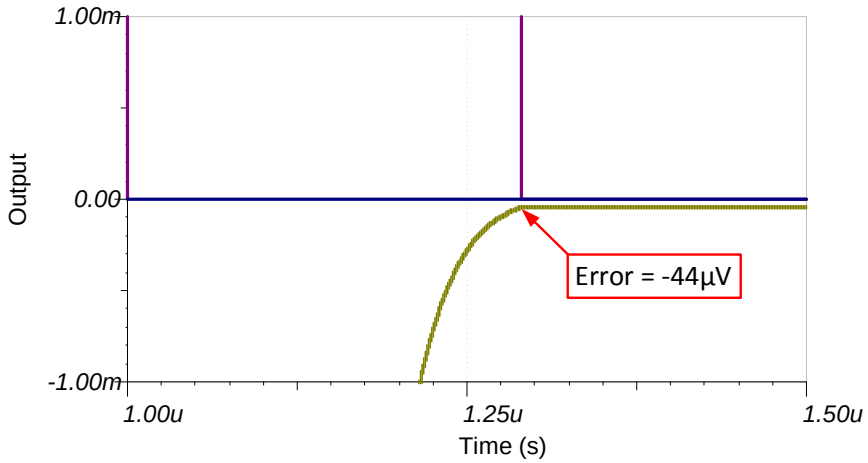
AC Transfer Characteristics

The bandwidth is simulated to be 11.45 kHz in this configuration. In this bandwidth it is not possible to drive the SAR converter at full speed. See the *TI Precision Labs* video series *Op Amps: Bandwidth 1* for more details on this subject.



Transient ADC Input Settling Simulation

The OPA320 buffer (20MHz) is used because it is capable of responding to the rapid transients from the ADC8860 charge kickback. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



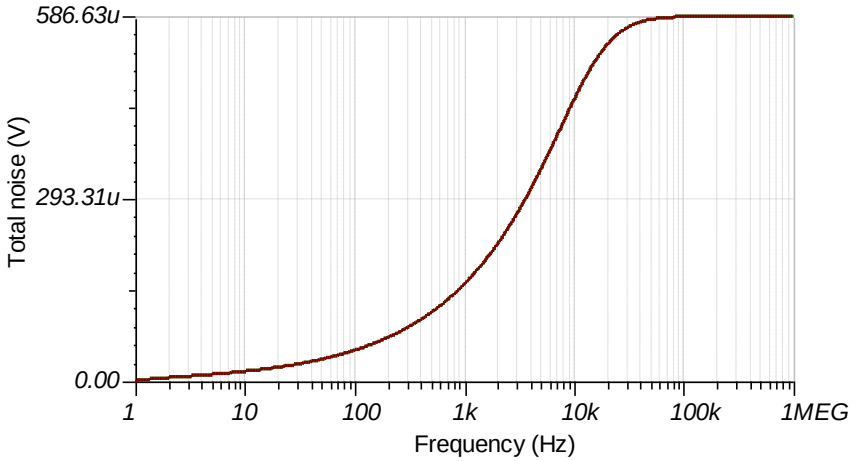
Noise Simulation

Use a simplified noise calculation for a rough estimate. We neglect the noise from the OPA192 as the instrumentation amplifier is in high gain so its noise is dominant.

$$E_n = Gain \cdot \sqrt{{e_{NI}}^2 + \left(\frac{e_{NO}}{Gain}\right)^2} \cdot \sqrt{K_n \cdot f_c}$$

$$E_n = (305.8) \cdot \sqrt{\left(18nV/\sqrt{Hz}\right)^2 + \left(\frac{110nV/\sqrt{Hz}}{305.8}\right)^2} \cdot \sqrt{1.57 \cdot (11.45kHz)} = 738\mu V/\sqrt{Hz}$$

Note that the calculated and simulated match well. Refer to *TI Precision Labs - Op Amps: Noise 4* for detailed theory on amplifier noise calculations, and *Calculating the Total Noise for ADC Systems* for data converter noise.

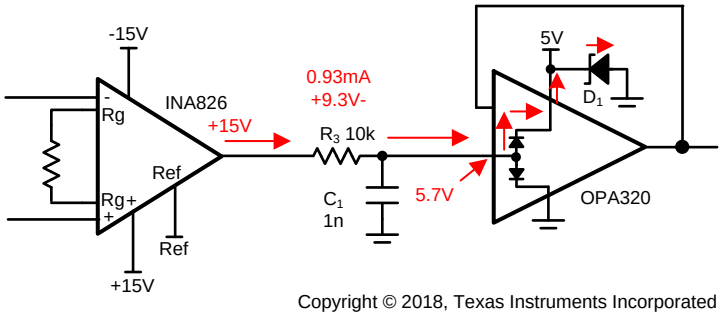


Overvoltage Protection Filter Between Instrumentation Amplifier and Op Amp

The filter between the INA826 and OPA320 serves two purposes. It protects the OPA320 from overvoltage, and acts as a noise or anti-aliasing filter. The INA826 gain should be scaled so that under normal circumstances, the output is inside the range of the OPA320 (that is, 0V to 5V). Thus, normally the overvoltage signals applied to the input of the OPA320 is not seen. However, during power up or in cases where the sensor is disconnected, the INA826 output may be at either power supply rail (that is, ±15V). In overvoltage cases, the resistor (R3) will limit current into the OPA320 for protection. The internal ESD diodes on the OPA320 will turn on during overvoltage events and direct the overvoltage signal to the positive or negative supply. In the following example, the overvoltage signal is directed to the positive supply and the transient voltage suppressor (D_1, SMAJ5.0A) turns on to sink the current. Note that the resistor is scaled to limit the current to the OPA320 absolute maximum input current (10mA). See *TI Precision Labs - Op Amps: Electrical Overstress (EOS)* for detailed theory on this subject.

$$R_3 > \frac{V_{INA} - V_{OpaSupply} - 0.7V}{I_{ABS\_MAX\_OPA}} = \frac{15V - 5.0V - 0.7V}{10mA} = 9.3k\Omega \text{ CHOOSE } 10K\Omega \text{ FOR MARGIN}$$

$$C_1 = \frac{1}{2 \cdot \pi \cdot R_3 \cdot f_c} = \frac{1}{2 \cdot \pi \cdot (10k\Omega) \cdot (15kHz)} = 1.06nF \text{ OR } 1NF \text{ STANDARD VALUE}$$



Optional Input Filter

The following figure shows a commonly used instrumentation amplifier input filter. The differential noise is filtered with C_{dif}, and the common mode noise is filtered with C_{cm1} and C_{cm2}. Note that it is recommended that $C_{dif} \geq 10C_{cm}$. This prevents conversion of common mode noise to differential noise due to component tolerances. The following filter was designed for a differential cutoff frequency of 15kHz.

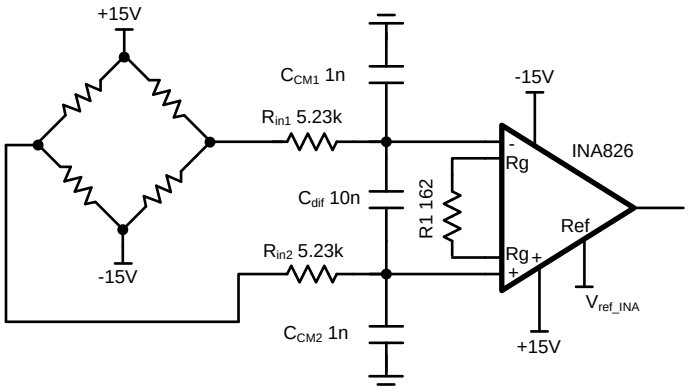
$$\text{LETC}_{\text{DIF}} = 1\text{NF AND } f_{\text{dif}} = 15\text{KHZ}$$

$$\text{R}_{\text{IN}} < \frac{1}{4 \cdot \pi \cdot f_{dif} \cdot C_{dif}} = \frac{1}{4 \cdot \pi \cdot (15kHz) \cdot (1nF)} = 5.305k\Omega \; or \; 5.23k\Omega \; \text{FOR 1\% STANDARD VAI}$$

$$C_{cm} = \frac{1}{10} \cdot C_{dif} = 100\,pF$$

$$f_{cm} = \frac{1}{2 \cdot \pi \cdot R_{in} \cdot C_{cm}} = \frac{1}{2 \cdot \pi \cdot (5.23k\Omega) \cdot (100\,pF)} = 304kHz$$

$$f_{dif} = \frac{1}{4 \cdot \pi \cdot R_{in} \cdot \left(C_{dif} + \frac{1}{2} C_{cm} \right)} = \frac{1}{4 \cdot \pi \cdot (5.23k\Omega) \cdot \left(1nF + \frac{1}{2} \cdot 100\,pF \right)} = 14.5kHz$$



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8860	16-bit resolution, SPI, 1-Msps sample rate, single-ended input, Vref input range 2.5V to 5.0V.	www.ti.com/product/ADS8860	www.ti.com/adcs
OPA192	8-kHz bandwidth, Rail-to-Rail output, 450-nA supply current, unity gain stable	www.ti.com/product/OPA192	www.ti.com/opamp
INA826	Bandwidth 1MHz (G=1), low noise 18nV/rtHz, low offset ±40µV, low offset drift ±0.4µV/ºC, low gain drift 0.1ppm/ºC. (typical values)	www.ti.com/product/INA826	www.ti.com/inas

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

Source Files for this circuit – http://www.ti.com/lit/zip/SBAC184.

Revision History

Revision	Date	Change
A	March 2019	Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page.

Circuit for driving a switched-capacitor SAR ADC with an instrumentation amplifier

Art Kay, Bryan McKay

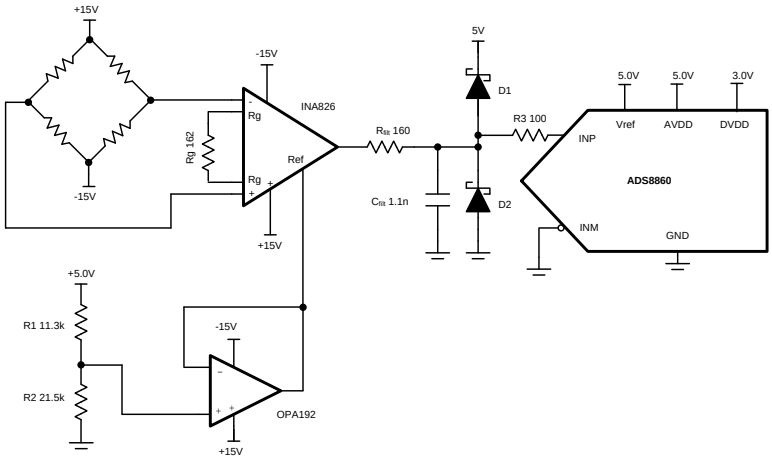
Input	ADC Input	Digital Output ADS8860
–5mV	Out = 0.2V	$0A3D_{H}$ or 2621_{10}
15mV	Out = 4.8V	$F5C3_{H}$ or 62915_{10}

Power Supplies					
AVDD	DVDD	V_{ref_INA}	V_{ref}	V_{cc}	V_{ee}
5.0V	3.0V	3.277V	5.0V	+15V	–15V

Design Description

Instrumentation amplifiers are a common way of translating low level sensor outputs to high level signals to drive an ADC. Typically, instrumentation amplifiers are optimized for low noise, low offset, and low drift. Unfortunately, the bandwidth of many instrumentation amplifiers may not be sufficient to achieve good settling to ADC charge kickback at maximum sampling rates. This document shows how sampling rate can be adjusted to achieve good settling. Furthermore, many instrumentation amplifiers are optimized for high-voltage supplies and it may be required to interface the high-voltage output (that is, ±15V) to a lower voltage ADC (for example, 5V). This design shows how to use Schottky diodes and a series resistor to protect the ADC input from an overvoltage condition. Note that the following circuit shows a bridge sensor, but this method could be used for a wide range of different sensors. A modified version of this circuit, *Driving a Switched-Capacitor SAR With a Buffered Instrumentation Amplifier* shows how a wide bandwidth buffer can be used to achieve higher sampling rate.

This circuit implementation is applicable to all *Bridge Transducers in PLC's* and *Analog Input Modules* that require Precision Signal-Processing and Data-Conversion.



Specifications

Specification	Calculated	Simulated
Sampling rate	200ksps	200ksps, settling to –6µV
Offset (ADC Input)	40µV · 306.7 = 12.27mV	16mV
Offset Drift	(0.4µV/ºC) · 306.7 = 123µV/ºC	NA
Noise	978µV	874µV

Design Notes

1. Select the gain to achieve an input swing that matches the input range of the ADC. Use the instrumentation amplifier reference pin to shift the signal offset to match the input range. This is covered in the *component selection* section.
2. The input Schottky diode configuration is used to prevent driving the input voltage outside of the absolute maximum specifications. The BAT54S Schottky is a good option for design as this device integrates both diodes into one package and the diodes are low leakage and have a low forward voltage. This is covered in the *component selection* section.
3. The buffer amplifier following the voltage divider is required for driving the reference input of most instrumentation amplifiers. Choose precision resistors and a precision low-offset amplifier as the buffer. Refer to *Selecting the right op amp* for more details on this subject.
4. Check the common-mode range of the amplifier using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* software tool.
5. Select C0G capacitors for C_{CM1}, C_{CM2}, C_{DIF}, and C_{filt} to minimize distortion.
6. Use 0.1% 20ppm/°C film resistors or better for the gain set resistor R_g. The error and drift of this resistor will directly translate into gain error and gain drift.
7. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit R_{filt} and C_{filt}. Although this method was designed for op amps, it can be modified for instrumentation amplifiers. Refer to *Introduction to SAR ADC Front-End Component Selection* for details on this subject.

Component Selection

1. Find the gain set resistor for the instrumentation amplifier to set the output swing to 0.2V to 4.8V.

$$Gain = \frac{V_{out\_max} - V_{out\_min}}{V_{in\_max} - V_{in\_min}} = \frac{4.9V - 0.2V}{5mV - (-10mV)} = 306.7$$

$$Gain = 1 + \frac{49.4k\Omega}{R_g}$$

$$R_g = \frac{49.4k\Omega}{Gain - 1.0} = \frac{49.4k\Omega}{(306.7) - 1.0} = 151.6\Omega \text{ or } 162\Omega \text{ for standard 0.1\% resistor}$$

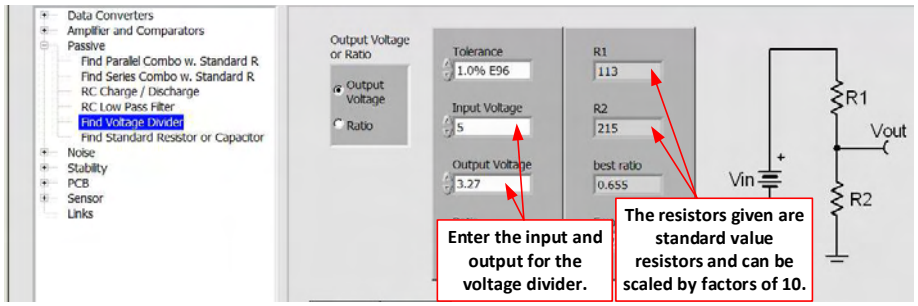
2. Find the INA826 reference voltage (V_{ref}) to shift the output swing to the proper voltage level.

$$V_{out} = Gain \cdot V_{in} + V_{ref\_INA}$$

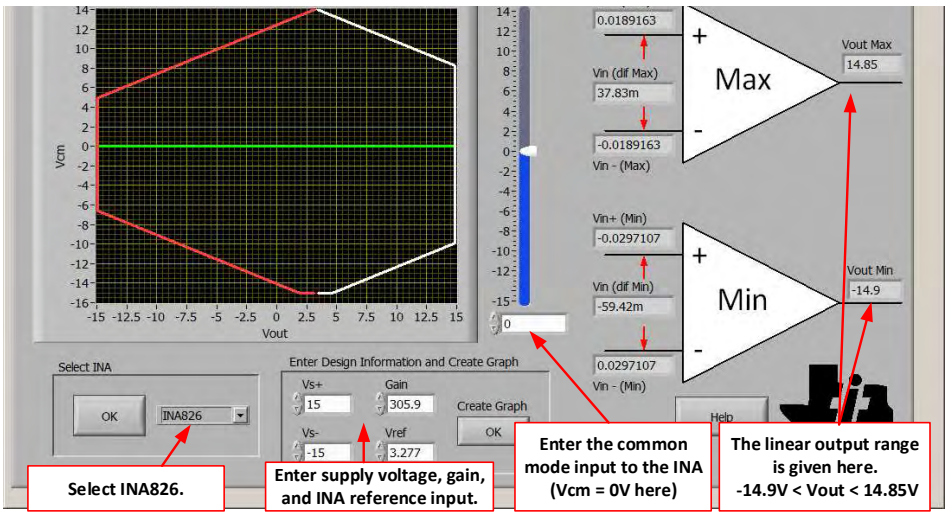
$$V_{ref\_INA} = V_{out} - Gain \cdot V_{in} = 4.8V - \left(1 + \frac{49.4k\Omega}{162\Omega}\right) \cdot (5mV) = 3.27V$$

3. Select standard value resistors to set the INA826 reference voltage (V_{ref} = 3.27V). *Use Analog Engineer's Calculator* ("Passive\Find Voltage Divider" section) to find standard values for the voltage divider.

$$V_{ref\_INA} = \frac{R_2}{R_1 + R_2} \cdot V_{in\_div} = \frac{21.5k\Omega}{11.3k\Omega + 21.5k\Omega} \cdot (5V) = 3.277V$$

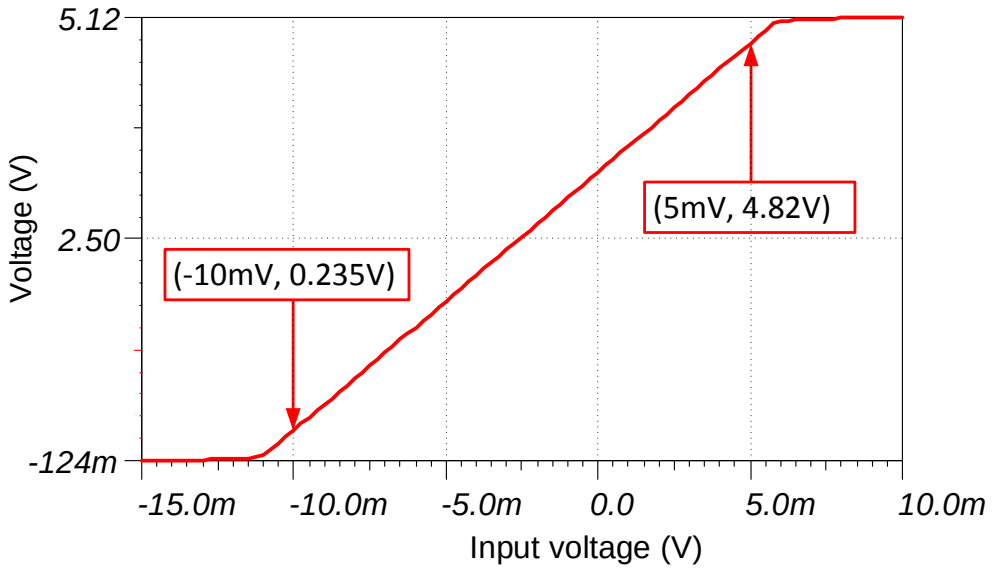


4. Use the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* to determine if the INA826 is violating the common-mode range.



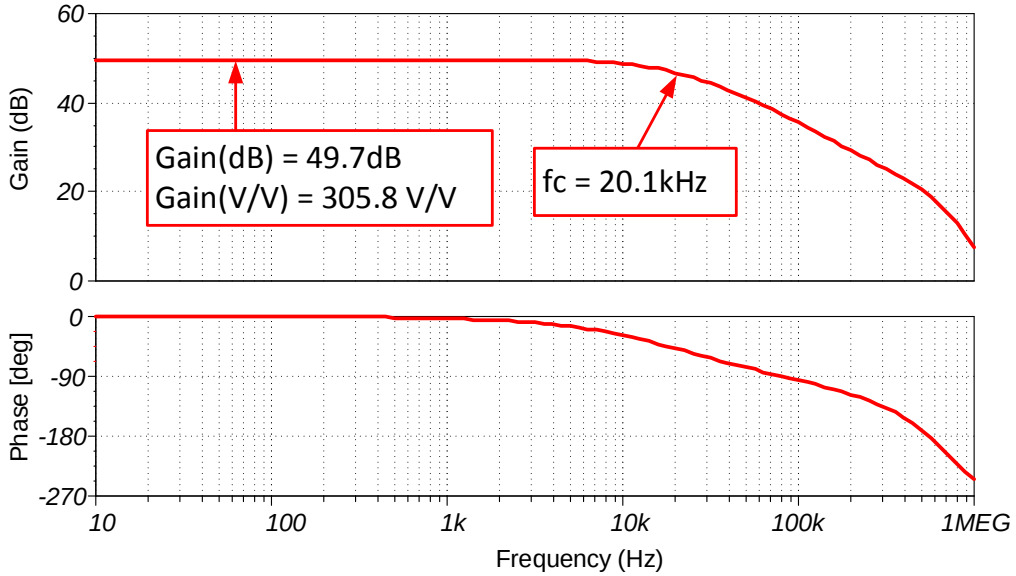
DC Transfer Characteristics

The following graph shows a linear output response for inputs from –5mV to +15mV. Refer to *Determining a SAR ADC's Linear Range when using Instrumentation Amplifiers* for detailed theory on this subject. Note that the output range is intentionally limited to –0.12V to 5.12V using Schottky diodes to protect the ADS8860. Note that Schottky diodes are used because the low forward voltage drop (typically less than 0.3V) keeps the output limit very near the ADC supply voltages. The absolute maximum rating for the ADS8860 is –0.3V < Vin < REF +0.3V.



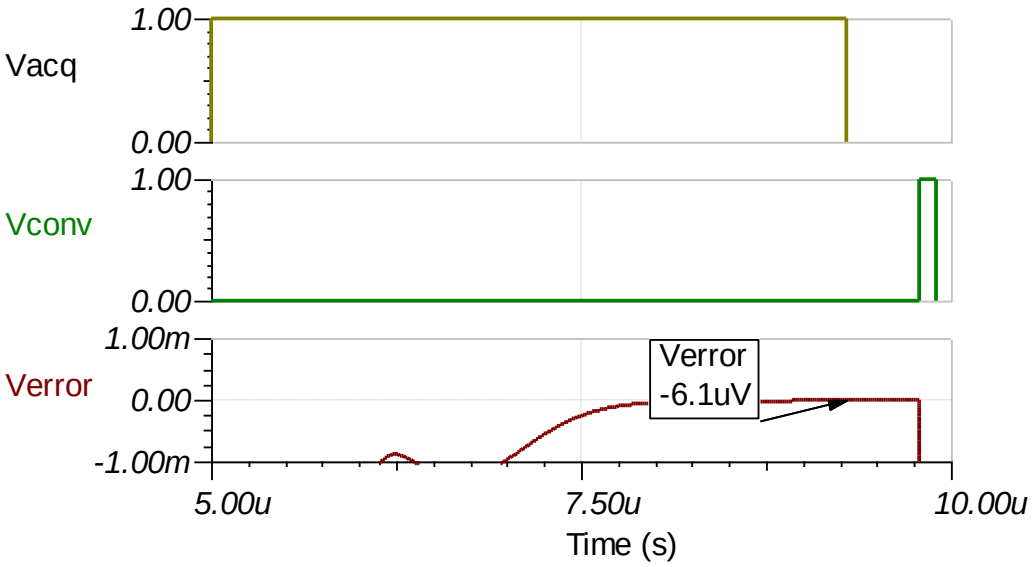
AC Transfer Characteristics

The bandwidth is simulated to be 20.1kHz, and the gain is 49.7dB which is a linear gain of 305.8. See the video series on *Op Amps: Bandwidth 1* for more details on this subject.



Transient ADC Input Settling Simulation

The following simulation shows settling to a +15mV dc input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject



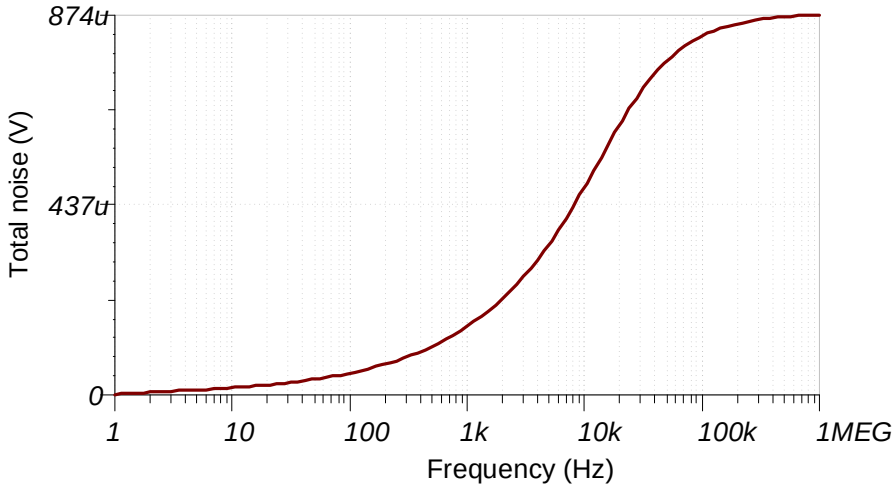
Noise Simulation

The following simplified noise calculation is provided for a rough estimate. We neglect noise from the OPA192 as the instrumentation amplifier is in high gain, so its noise is dominant.

$$E_n = \text{Gain} \cdot \sqrt{e_{NI}^2 + \left(\frac{e_{NO}}{\text{Gain}}\right)^2} \cdot \sqrt{K_n \cdot f_c}$$

$$E_n = (305.8) \cdot \sqrt{\left(18\text{nV}/\sqrt{\text{Hz}}\right)^2 + \left(\frac{110\text{nV}/\sqrt{\text{Hz}}}{305.8}\right)^2} \cdot \sqrt{1.57 \cdot (20.1\text{kHz})} = 978\mu\text{V}/\sqrt{\text{Hz}}$$

Note that calculated and simulated match well. Refer to *TI Precision Labs - Op Amps: Noise 4* for detailed theory on amplifier noise calculations, and *Calculating the Total Noise for ADC Systems* for data converter noise.



Optional Input Filter

The following figure shows a commonly used instrumentation amplifier input filter. The differential noise is filtered with C_{dif}, and the common-mode noise is filtered with C_{cm1} and C_{cm2}. Note that it is recommended that $C_{dif} \geq 10C_{cm}$. This prevents conversion of common-mode noise to differential noise due to component tolerances. The following filter was designed for a differential cutoff frequency of 15kHz.

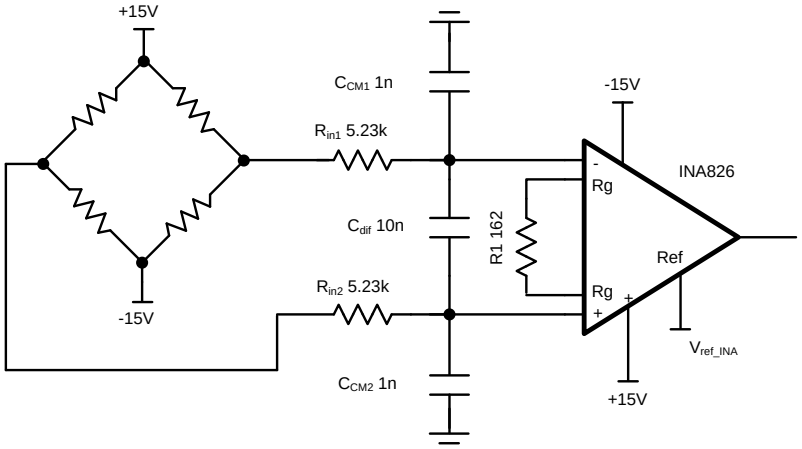
Let $C_{dif} = 1\text{nF}$ and $f_{dif} = 15\,\text{kHz}$

$$R_{in} < \frac{1}{4 \cdot \pi \cdot f_{dif} \cdot C_{dif}} = \frac{1}{4 \cdot \pi \cdot (15\,\text{kHz}) \cdot (1\text{nF})} = 5.305\,\text{k}\Omega \text{ or } 5.23\,\text{k}\Omega \text{ for 1\% standard value}$$

$$C_{cm} = \frac{1}{10} \cdot C_{dif} = 100\,\text{pF}$$

$$f_{cm} = \frac{1}{2 \cdot \pi \cdot R_{in} \cdot C_{cm}} = \frac{1}{2 \cdot \pi \cdot (5.23\text{k}\Omega) \cdot (100\text{pF})} = 304\text{kHz}$$

$$f_{dif} = \frac{1}{4 \cdot \pi \cdot R_{in} \cdot \left(C_{dif} + \frac{1}{2} C_{cm}\right)} = \frac{1}{4 \cdot \pi \cdot (5.23\text{k}\Omega) \cdot \left(1\text{nF} + \frac{1}{2} \cdot 100\text{pF}\right)} = 14.5\,\text{kHz}$$



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8860	16-bit resolution, SPI, 1Msps sample rate, single-ended input, Vref input range 2.5 V to 5.0 V.	www.ti.com/product/ADS8860	www.ti.com/adcs
OPA192	Bandwidth 10MHz, Rail-to-Rail input and output, low noise 5.5nV/rtHz, low offset ±5µV, low offset drift ±0.2µV/ºC. (Typical values)	www.ti.com/product/OPA192	www.ti.com/opamp
INA826	Bandwidth 1MHz (G = 1), low noise 18nV/rtHz, low offset ±40µV, low offset drift ±0.4µV/ºC, low gain drift 0.1ppm/ºC. (Typical values)	www.ti.com/product/INA826	www.ti.com/inas

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

Source files for this design - http://www.ti.com/lit/zip/sbac184.

Revision History

Revision	Date	Change
A	March 2019	Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page.

Circuit for driving an ADC with an instrumentation amplifier in high gain

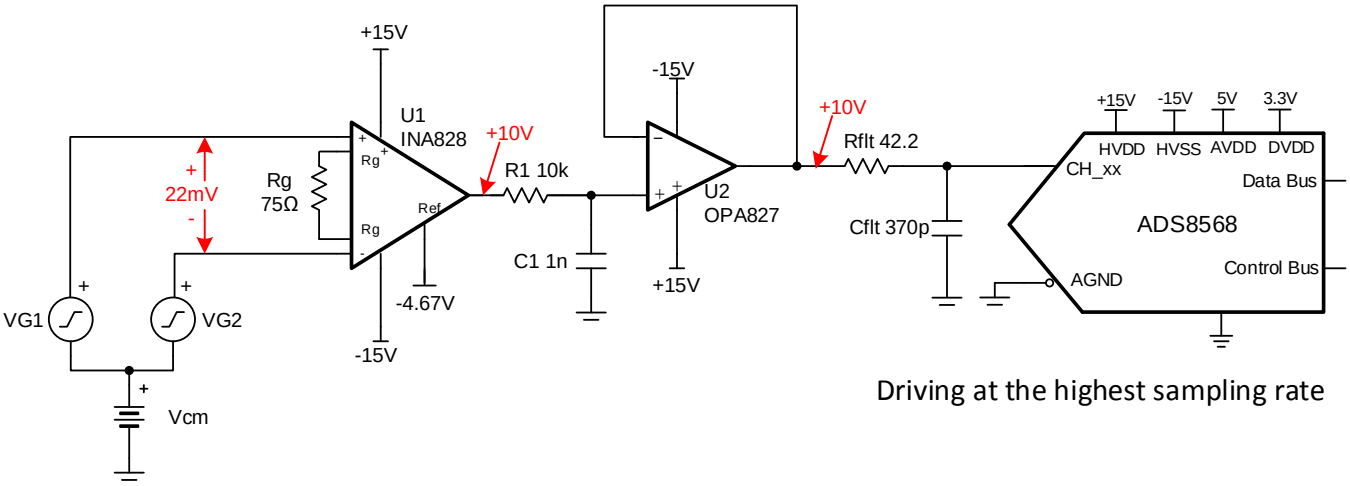
Dale Li, Art Kay

Input	ADC Input	Digital Output ADS8568
VinDiffMin = –8mV	CH_x = –10V	8000H
VinDiffMax = +22mV	CH_x = +10V	7FFFH

Power Supplies			
AVDD		**Vee**	**Vdd**
5.0V	3.3V	+15V	–15V

Design Description

Instrumentation amplifiers are optimized for low noise, low offset, low drift, high CMRR and high accuracy but these instrument amplifiers may not be able to drive a precision ADC to settle the signal properly during the acquisition time of ADC. This design shows an example of how to set the gain and offset shift to amplify a low level asymmetric input signal. Also, the high gain limits the INA828 instrumentation amplifier bandwidth, so an OPA827 op amp is used as a buffer so that the ADS8568 full sampling rate can be achieved. A related cookbook circuit shows a simplified approach that does not include the wide bandwidth buffer (*Driving High Voltage SAR ADC with an Instrumentation Amplifier*), this simplified approach has limited sampling rate as compared to the buffered design in this document. Also *Driving High Voltage SAR ADC with a Buffered Instrumentation Amplifier*, analyzes this design in unity gain. This circuit implementation is applicable to all *Bridge Transducers in PLC's* and *Analog Input Modules* that require precision signal-processing and data-conversion.



Driving at the highest sampling rate

Specifications

Specification	Goal	Calculated	Simulated
Transient Settling Error	>0.5 LSB (152µV)	NA	0.36µV
Noise		1.1mV	1.14mV
System Offset Error		33.6mV	NA
System Offset Drift		334µV/ºC	NA
System Gain Error		0.53%	NA
System Gain Drift		54.2ppm/ºC	NA

Design Notes

1. The bandwidth of instrumentation amplifiers is typically not enough to drive SAR data converters at a higher data rate. This is especially true when the instrumentation amplifier is in high gain. so a wide bandwidth driver is needed because the SAR ADC with switched-capacitor input structure has an input capacitor that needs to be fully charged during each acquisition time. The OPA827 buffer is added to allow the ADC to run at full sampling rate (ADS8568 510kSPS for parallel interface).
2. Check the common-mode range of the amplifier using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* software tool.
3. Select COG capacitors for C_1 and C_{filt} to minimize distortion.
4. The gain set resistor, R_g, should be a 0.1% 20ppm/°C film resistors or better for low gain error and low gain drift.
5. The *TI Precision Labs* video series covers the method for selecting the driver amplifier and the charge bucket circuit R_{filt} and C_{filt}. See *Introduction of SAR ADC Front-End Component Selection* for details.
6. Set the cutoff of the filter between the op amp and instrumentation amplifier for anti aliasing and to minimize noise. See *Aliasing and Anti-aliasing Filters* for more details on aliasing and anti-aliasing filters.
7. Because of the high instrumentation amplifier gain, the DC errors (offset, gain, and drift) are significant. Calibration is a good approach to minimizing these errors. See *Understanding and Calibrating the Offset and Gain for ADC Systems* for more details on calibration.

Component Selection

1. Find the gain based on differential input signal and the ADS8568 full-scale input range.

$$G = \frac{V_{out} - V_{out}}{V_{in} - V_{in}} = \frac{10V - (-10V)}{22mV - (-8mV)} = 666.7$$

$$R_g = \frac{50k\Omega}{G - 1} = \frac{50k\Omega}{666.7} = 75.1\Omega$$

$$R_g = 75.1\Omega \text{ standard value}$$

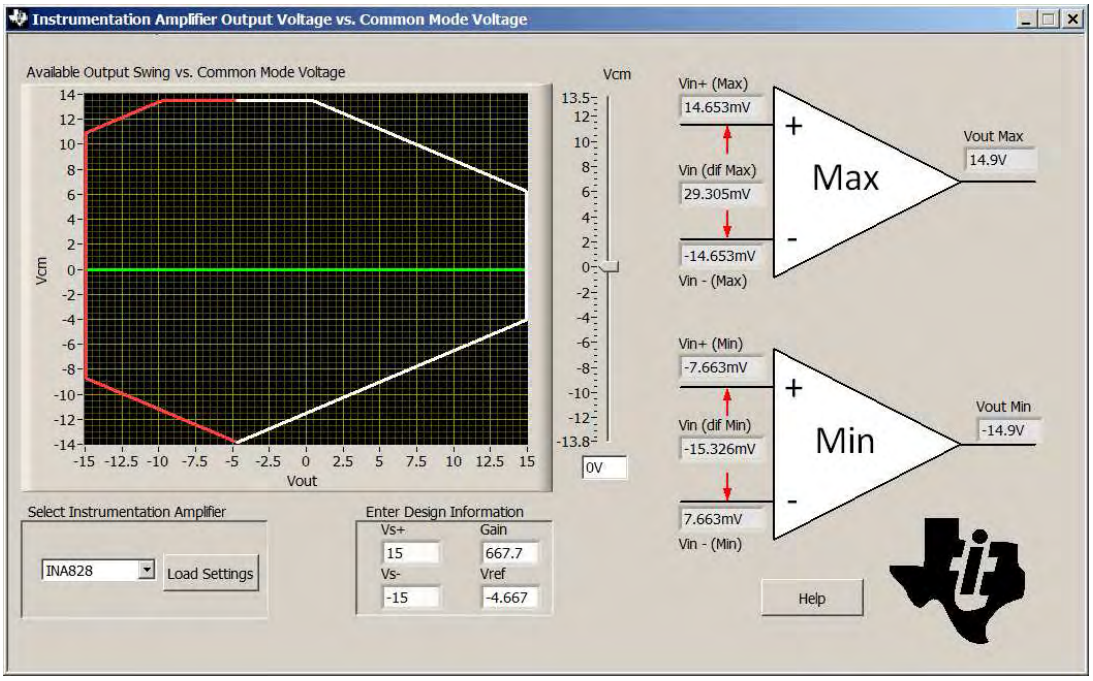
$$G = 1 + \frac{50k\Omega}{R_g} = 667.7$$

2. The input signal in this design is ±10-V high voltage signal, so the gain of INA828 should be set to 1 and no gain resistor (R_g) is needed.

$$V_{out} = G \cdot V_{in} + V_{ref}$$

$$V_{ref} = V_{out} - G \cdot V_{in} = 10V - 667.7 \cdot 22mV = -4.667V$$

3. Use the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* to determine if the INA826 is violating the common-mode range. The common-mode calculator in the following figure indicates that the output swing is ±14.9V for a 0-V common-mode input.

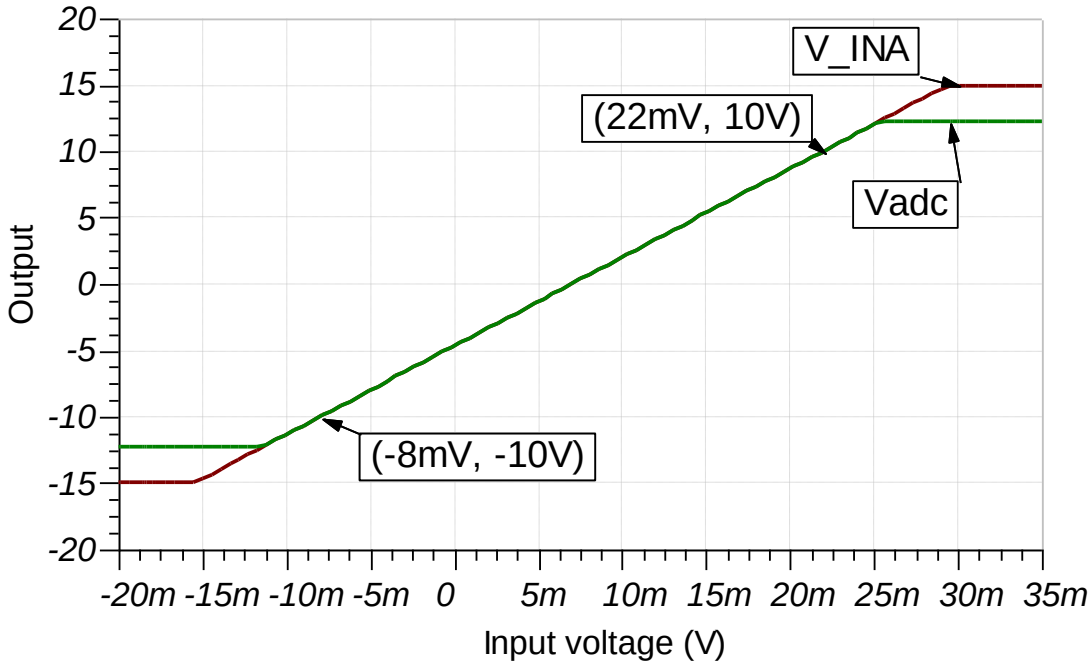


4. Find the value for C_{filt}, and R_{filt} using TINA SPICE and the methods described in *Introduction of SAR ADC Front-End Component Selection* videos. The value of R_{filt} and C_{filt} shown in this document will work for these circuits; however, if you use different amplifiers you will have to use TINA SPICE to find new values.
5. Select the RC filter between the INA828 and OPA827 based on your system requirements (f_{cRC} = 15.9kHz in this example).

$$f_{cRC} = \frac{1}{2\pi \cdot R_1 \cdot C_1} = \frac{1}{2\pi \cdot (10k\Omega) \cdot (1pF)} = 15.9kHz$$

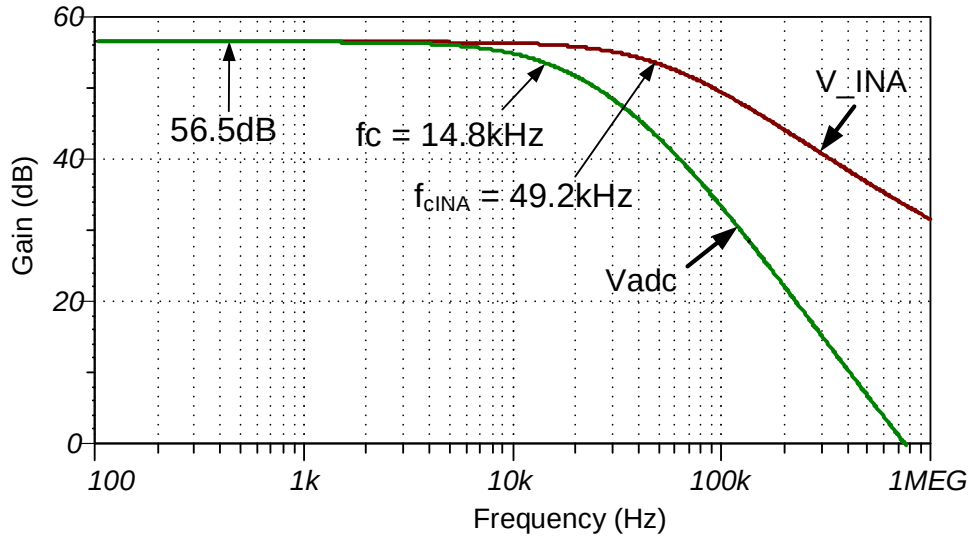
DC Transfer Characteristics

The following graph shows a linear output response for inputs from differential –10V to +10V. See *Determining a SAR ADC's Linear Range when using Instrumentation Amplifiers* for detailed theory on this subject. The full-scale range (FSR) of the ADC falls within the linear range of the Instrumentation Amplifier.



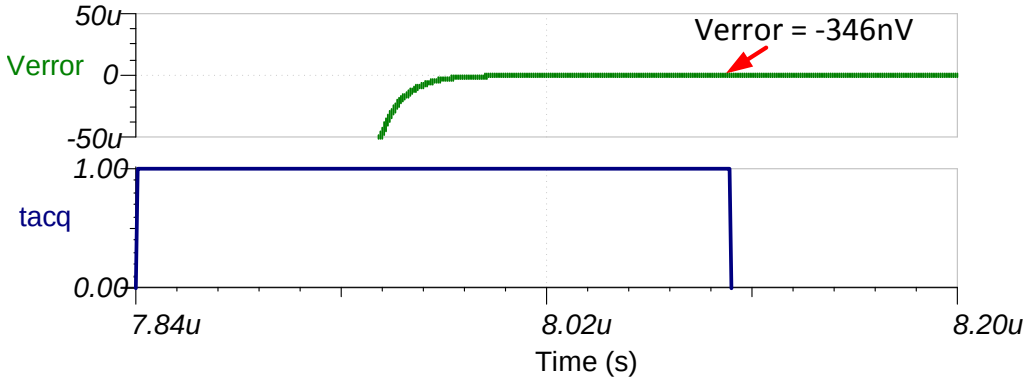
AC Transfer Characteristics

The bandwidth for this design is simulated to be 14.8kHz and the gain is 56.4dB (667.7V/V). The bandwidth limit is set by a combination RC filter (f_{cRC} = 15.9kHz) and the instrumentation amplifier (f_{cINA}=49.2kHz).



Transient ADC Input Settling Simulation (510kSPS)

The OPA827 buffer (22-MHz GBW) is used because it is capable of responding to the rapid transients from the charge kickback of the ADS8568. The op-amp buffer allows the system to achieve the ADS8568 maximum sampling rate of 510kSPS. The following simulation shows settling to a full-scale DC input signal with the INA828 and OPA827 buffer, and ADS8568. This type of simulation shows that the sample and hold kickback circuit is properly selected to meet desired ½ of a LSB (152µV). See *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



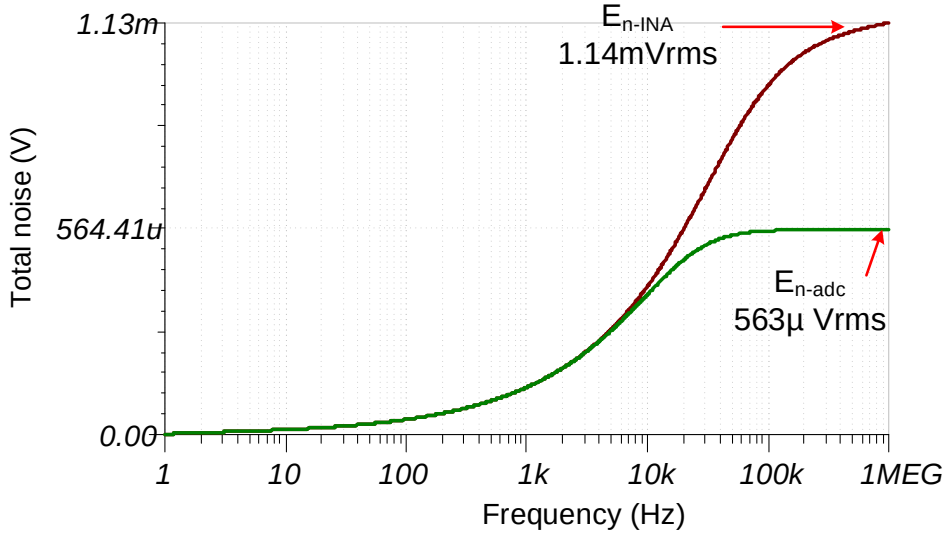
Noise Simulation

The section walks through a simplified noise calculation for a rough estimate. We neglect the noise from the OPA827 as the noise of the INA828 is dominant also neglect resistor noise in this calculation as it is attenuated for frequencies greater than 15.92kHz.

$$E_n = Gain \cdot \sqrt{e_{NI}^2 + \left(\frac{e_{NO}}{Gain}\right)^2} \cdot \sqrt{K_n \cdot f_c}$$

$$E_n = 667.7 \cdot \sqrt{\left(7nV/\sqrt{Hz}\right)^2 + \left(\frac{90nV/\sqrt{Hz}}{667.7}\right)^2} \cdot \sqrt{1.57 \cdot 14.8kHz} = 595\mu Vrms$$

Note that calculated and simulated match well (simulated = 563µV_{RMS}, calculated = 595µV_{RMS}). See *TI Precision Labs - Op Amps: Noise 4* for detailed theory on amplifier noise calculations and *Calculating Total Noise for ADC Systems* for data converter noise.



Gain Error and Offset Estimates:

The following offset and offset drift calculations will be dominated by the instrumentation amplifier since it is in high gain. Gain error calculations include the gain error of the ADC and instrumentation amplifier. For offset and gain error, the maximum room temperature value is used. See *Statistics Behind Error Analysis* for details on system gain and offset error.

System Offset Calculation:

$V_{osi} = 50\mu V,\ V_{oso} = 250\mu V$ max at room temp

$G = 667.7V/V$

$$V_{osRTI} = V_{osi} + \frac{V_{oso}}{G} = 50\mu V + \frac{250\mu V}{667.7} = 50.4\mu V$$

$$V_{osRTO} = G \cdot V_{osRTI} = 667.7 \cdot 50.4\mu V = 33.6mV$$

$V_{os(System)} \approx 33.6mV$ total system offset is dominated by INA828 offset

System Offset Drift Calculation:

$V_{osDrift(INA828RTI)} = 0.5\mu V/^{o}C$

$V_{osDrift(INA828RTO)} = G \cdot V_{osDriftINA828RTI} = 667.7 \cdot 0.5\mu V/°C = 334\mu V/°C$

$V_{osDrift(System)} \approx 334\mu V/°C$ the INA drift dominates because of the high gain.

System Gain Error Calculation:

$GE_{ina} = \pm 0.15\%,$ max room temp INA828

$GE_{Rg} = \pm 0.1\%,$ Rg Tolerance

$GE_{ADS8568} = \pm 0.5\%,$ max room temp ADS8568

$$GE_{total} = \sqrt{(GE_{ina})^2 + (GE_{Rg})^2 + (GE_{ADS8568})^2} = \sqrt{(0.15\%)^2 + (0.1\%)^2 + (0.5\%)^2} = 0.53\%$$

System Gain Drift Calculation:

$$\frac{\Delta GE_{INA}}{\Delta T} \approx 50ppm/°C$$

$$\frac{\Delta GE_{Rg}}{\Delta T} \approx 20ppm/°C$$

$$\frac{\Delta GE_{ADC8568}}{\Delta T} \approx 6ppm/°C$$

$$\frac{\Delta GE_{System}}{\Delta T} \approx \sqrt{(50ppm/°C)^2 + (20ppm/°C)^2 + (6ppm/°C)^2} = 54.2ppm/°C$$

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8568	16-bit resolution, SPI, 500kSPS sample rate, single-ended input, simultaneous sampling, internal reference, programmable range up to ±12V.	http://www.ti.com/product/ADS8568	http://www.ti.com/adcs
INA828	Bandwidth 1MHz (G=1), low noise 18nV/√Hz, low offset ±40µV, low offset drift ±0.4µV/ºC, low gain drift 0.1ppm/ºC. (Typical values)	http://www.ti.com/product/INA828	http://www.ti.com/inas
OPA827	Gain bandwidth 22MHz, low noise 4nV/√Hz, low offset ±75µV, low offset drift ±0.1µV/ºC (Typical values)	http://www.ti.com/product/OPA827	http://www.ti.com/opamp

Link to Key Files

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Source files for this circuit - http://www.ti.com/lit/zip/SBAC215.

Low-input bias-current front end SAR ADC circuit

Mike Stout

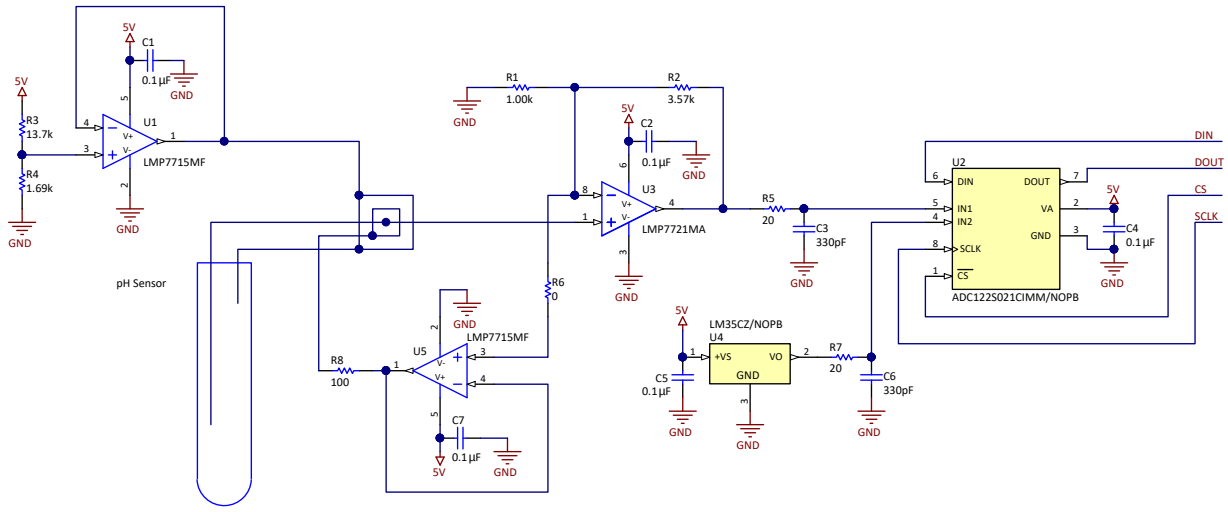
Input	ADC Input	Digital Output ADC122S021
VinMin = 0.03V	IN1 = 0.14	115 = 0x073
VinMax = 1.07V	IN1 = 4.88	3998 = 0xF9E
VinMin = 0V	IN2 = 0V	0 = 0x000
VinMax = 1V	IN2 = 1V	819 = 0x333

Power Supplies	
V+, VA	V–
5V	0V

Design Description

This design shows a low Ibias amplifier being used to drive a SAR ADC. A sensor with high output impedance requires an amplifier with a low input bias current to minimize errors. Examples of applications where this type of sensor might be used include *gas detectors*, *blood gas analyzers*, and *air quality detectors*. In this design, a pH probe is used for the sensor. The output impedance of a pH probe can be from 10MΩ to 1000MΩ. If a pH probe is used that has an output impedance of 10MΩ with an op amp that has 3nA of input bias current, the error due to the input bias current of the op amp will be 30mV. Using the input signal amplitude and gain described in the *component selection* section, this 30mV equates to an error of about 2.9%. If an op amp with an input bias current of 3fA is used, the error is decreased to 30nV.

The output of the pH sensor does not quickly change, so a lower speed ADC can be used. The value from the pH sensor changes as the temperature changes so a two channel ADC was selected so that one channel could be used to monitor the temperature. The ADC122S021 used in this design is a 2-channel, 12-bit, ADC that can sample up to 200ksps.



Specifications

Specification	Calculated	Simulated	Measured
Ibias	20fA	118fA	20fA

Design Notes

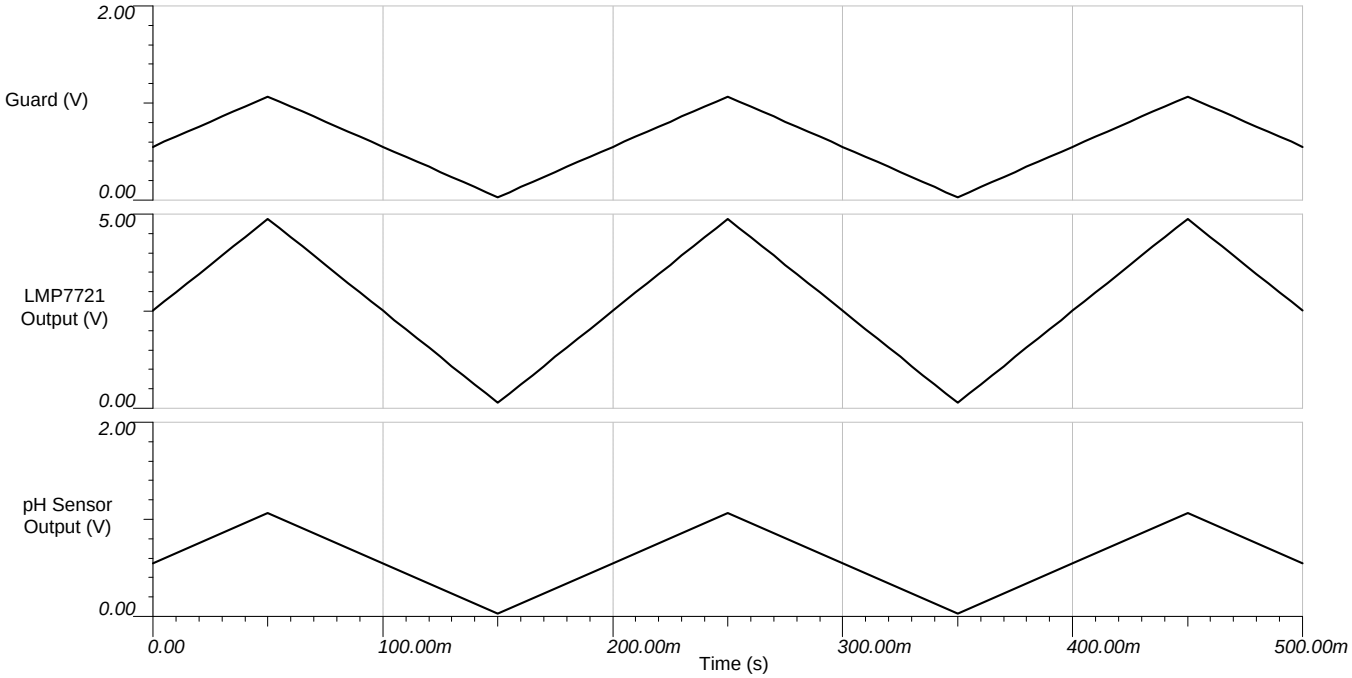
1. Use COG (NPO) capacitors for C3 and C6.
2. Each IC should have a bypass capacitor of 0.1μF.
3. PCB layout is very important. See the *LMP7721 Multi-Function Evaluation Board Users' Guide*.
4. The PCB must be clean. See the *LMP7721 Multi-Function Evaluation Board Users' Guide*.
5. For more information on low leakage design, see *Design femtoampere circuits with low leakage*.

Component Selection

1. The output voltage of a pH sensor changes as the temperature changes. At 0°C it outputs 54.2mV/pH, at 25°C it outputs 59.16mV/pH, and at 100°C it outputs 74.04mV/pH. This means that the maximum swing of the pH sensor around the bias point of the pH sensor will be ±518.3mV at 100°C. The maximum output of the LMP7721 should be limited to ±2.4V to allow for headroom. That sets the gain of the LMP7721 at:
   2.4V / 0.5183V = 4.6V/V
   Setting resistors R2 = 3.57kΩ and R1 = 1kΩ, will set this gain.
2. Since the input of the LMP7721 must be from 0V to 5V, the pH sensor needs to be biased above ground. Resistors R3 = 13.7kΩ and R4 = 1.69kΩ in a voltage divider configuration will set the input of U1 to:
   5V · 1.69kΩ / (1.69kΩ + 13.7kΩ) = 549mV
   U1 has a gain of 1V/V so the bias of the pH sensor will also be at 549mV. Since the pH sensor can swing –518.3mV below the bias point, this keeps the input of the LMP7721 above ground. The output of the LMP7721 will be centered at:
   0.549V · 4.6V/V = 2.52V
   and can swing ±2.4V above and below the center point.
3. U5 is used to set the voltage of the guard ring. It is set with a gain of 1V/V and the input is the signal on the –IN pin of the LMP7721.
4. The output of the LMP7721 is connected to one of the inputs of the ADC122S021 SAR ADC. The sampling capacitor of the ADC is 33pF and the external capacitor placed next to the pin of the ADC should be 10 times larger, or 330pF. A small resistor of 20Ω is added in series to isolate the capacitor from the LMP7721.
5. Because the output of the pH sensor changes as the temperature changes the LM35, a temperature sensor, is connected to channel 2 of the ADC122S021. A 330-pF capacitor along with a 20-Ω series resistor is used on the output of the temperature sensor.

DC Transfer Characteristics

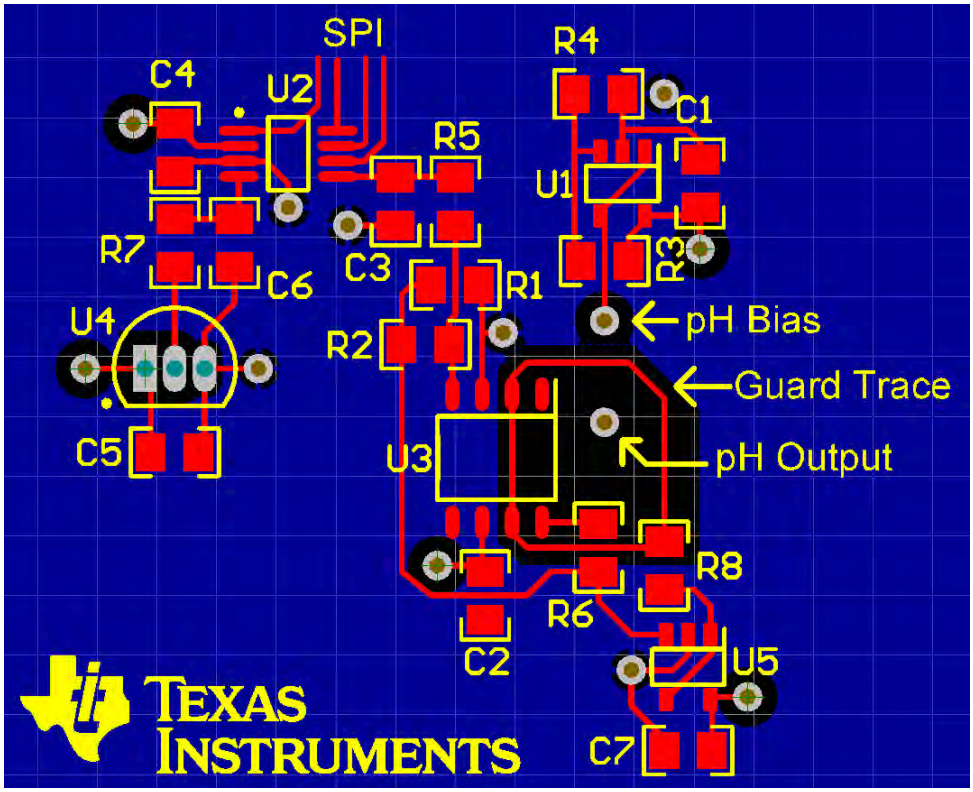
The following graph shows the pH sensor input to the LMP7721, the Guard voltage, and the LMP7721 output. This data is for 100°C, when the pH sensor output has the largest possible output swing.



Layout

The PCB layout is very important for a low Ibias circuit. Current leakage will occur between two traces when there a voltage potential between the traces. This is the reason for the guard trace. The guard trace is set to a voltage close to the input voltage to minimize the leakage between the input of the LMP7721 and the outside world. The LMP7721 includes two unused pins (pins 2 and 7) that can be used to simplify the layout of a guard trace.

The following image shows a sample layout. The output of the pH sensor and the +IN input of the LMP7721 are separated from the rest of the circuit by the guard trace, which is close to the input voltage. This will minimize the leakage on the input of the LMP7721. The bias of the pH sensor is located outside of the guard. Leakage between the bias point and the rest of the circuit is not important. Solder mask should not cover the area inside the guard trace. If there is a ground plane on the bottom side of the board or other internal planes, they should have a 'keep out' area underneath the guard area.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADC122S021	12 bit, SPI, 2 channel, 50ksps to 200ksps, single ended input	www.ti.com/product/adc122s021	www.ti.com/adcs
LMP7721	Ultra-low input bias current of 3fA, with a specified limit of ±20fA at 25°C, offset voltage ±26µV, GBW 17MHz	www.ti.com/product/lmp7721	www.ti.com/opamps
LMP7715	Input offset voltage ±150µV, input bias current 100fA, input voltage noise 5.8nV/√Hz, gain bandwidth product 17MHz	www.ti.com/product/lmp7715	www.ti.com/opamps
LM35	Calibrated directly in degrees Celsius, Linear + 10-mV/°C scale factor, 0.5°C ensured accuracy (at 25°C), rated for full –55°C to 150°C range	www.ti.com/product/lm35	www.ti.com/temperature

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Revision History

Revision	Date	Change
A	March 2019	Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page.

High-side current shunt monitor circuit to 3-V single-ended ADC

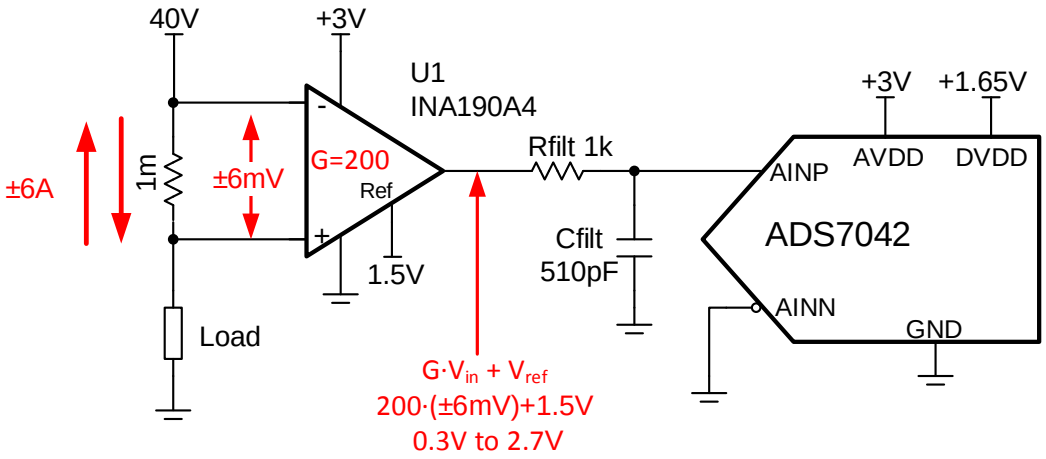
Art Kay

Input	ADC Input	Digital Output ADS7042
–6A	0.3V	$19A_H$, 410_d
+6A	2.7V	$E66_H$, 3686_d

Power Supplies		
AVDD / V_{REF}	**DVDD**	**Vsup**
3.0V	1.65V	40V

Design Description

Current shunt monitors are amplifiers that are optimized to read small shunt voltages over very wide common mode ranges. This example application uses the INA190A4 to translate a ±6-A current into a 0-V to 3-V range for the ADC. Note that this is a high sided current measurement with a 40V common mode range. Detailed theory on current sensing is covered in *Using current sense amplifiers to solve today's current sensing design challenges*. Compared to other current shunt devices the INA190 has very low offset voltage, bias current, and drift. This excellent DC performance allows smaller for smaller input voltage ranges without compromising accuracy as the offset is small compared to the input signal. The use of small shunt resistors is an advantage as the power dissipated in the shunt is smaller for smaller resistors for a given current level. The ADS7042 is a 12 bit 1MSPS SAR ADC with a 3V analog input range. The design shown in this document can be modified for other data converters and input ranges. This design can be used a wide range of applications where current needs to be monitored such as notebook computers, cell phones, and battery management.



Specifications

Specification	Goal	Calculated	Simulated
Transient Settling	< 0.5LSB = 366µV	NA	0.94µV
Noise	NA	3.5mVrms	3.16mV
Bandwidth	NA	33kHz	35kHz

Design Notes

1. The tolerance in the shunt resistor, R_{SENSE}, will translate into a gain error. Choose the tolerance according to your error budget. Note that the maximum specified gain error for the INA190A4 is 0.3% and a common tolerance 1-m resistor is 0.5% to 1.0%.
2. Selection of the shunt resistor is covered in the component selection section. The objective is to minimize power dissipation while maintaining good accuracy.
3. Use a C0G capacitor for C_{FILT} to minimize distortion.
4. The example design is for a bidirectional current source (for example, ±6A). A similar approach can be followed for an unidirectional current source (for example, 0A to 12A). The main difference is that the reference input pin would connect to ground as opposed to 1/2 V_{REF}.

Component Selection

1. Choose Rsense Resistor and find Gain for the current sense amplifier (bidirectional current)

$$R_{sh} < \frac{P_{max}}{(I_{max})^2} = \frac{50mW}{(6A)^2} = 1.38m\Omega$$

$$Choose\ Rsh\ =\ 1m\Omega$$

$$\pm V_{out(\text{range})} = \pm\frac{V_{REF}}{2} = \pm\frac{3V}{2} = \pm 1.5V$$

$$G_{INA} = \frac{\pm V_{out(\text{range})}}{I_{load(\max)} \cdot R_{sh}} = \frac{\pm 1.5V}{6A \cdot 1m\Omega} = 250V/V$$

Select INA190A4, $G\ =\ 200V/V$, Common Mode Range : $-0.2\ V\ to\ 40\ V$

2. Calculate the current sense amplifier output range

$$V_{INA\_outmax} = G_{INA} \cdot \left(I_{load(\max)} \cdot R_{sh}\right) + \frac{V_{REF}}{2} = 200V/V \cdot (6A \cdot 1m\Omega) + \frac{3V}{2} = 2.7V$$

$$V_{INA\_outmin} = G_{INA} \cdot \left(I_{load(\min)} \cdot R_{sh}\right) + \frac{V_{REF}}{2} = 200V/V \cdot (-6A \cdot 1m\Omega) + \frac{5V}{2} = 0.3V$$

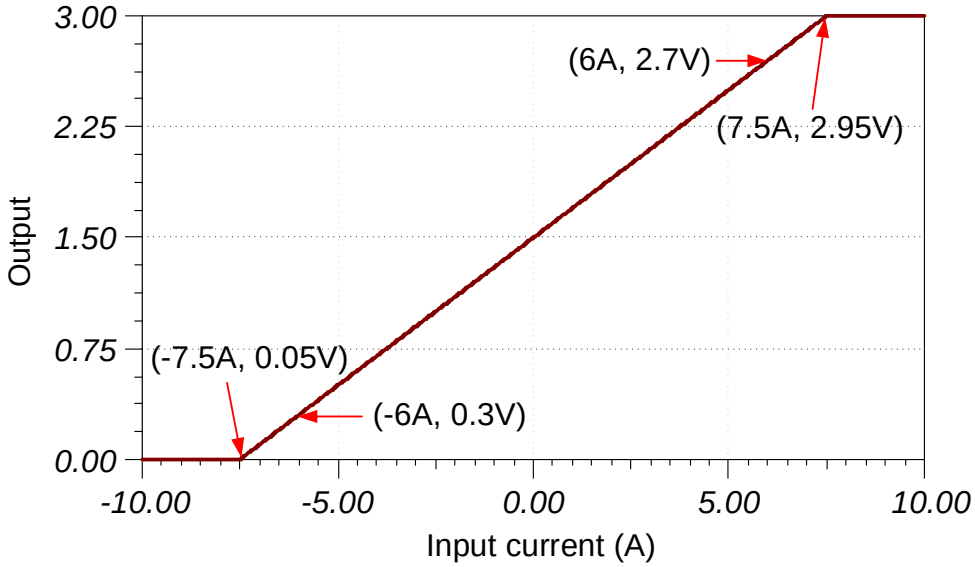
3. Find the INA190 output swing from the data sheet.
   Swing to Positive Rail = 3V - 40mV = 2.96V
   Swing to Negative Rail = 1mV
   The output is scaled for 0.3V to 2.7V, so this design has significant margin.
   If desired, a larger shunt resistor could be used to expand the usable range.
4. Offset Error impact on system error.
   OutputOffsetINA = $V_{os} \cdot Gain = 15\mu V \cdot 200 = 3mV$
   OfsetADS7042 = $3LSB \cdot 366\,\mu V/LSB = 1.1mV$

$$TotalOffsetRSS = \sqrt{(3mV)^2 + (1.1mV)^2} = 3.2mV$$

$$Error(\%FSR) = \frac{3.2mV}{3V} \cdot 100 = 0.11\%\ \text{of FSR}$$

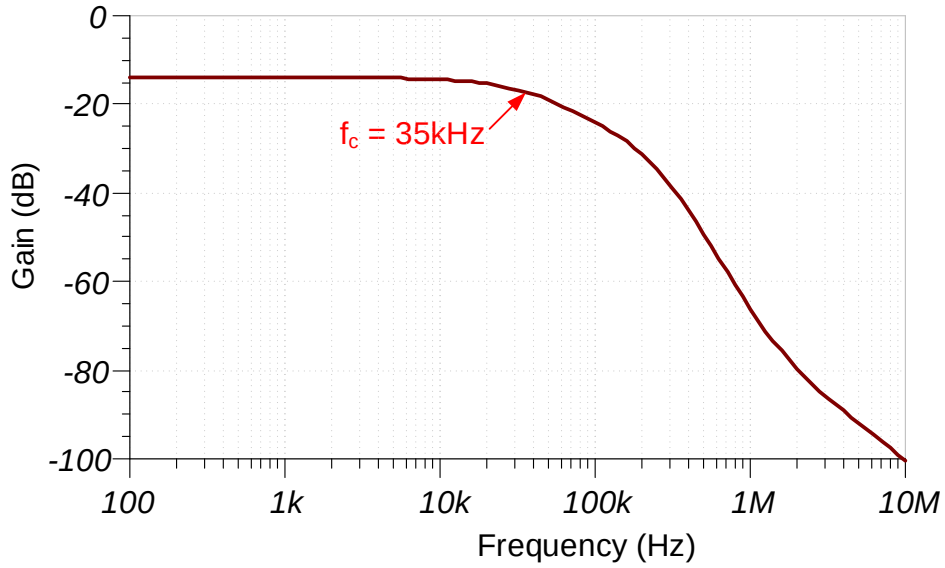
DC Transfer Characteristics

The following graph shows a linear output response for inputs from –7.5A to +7.5A. The required linear range is ±6A, so this circuit meets the requirement with design margin.



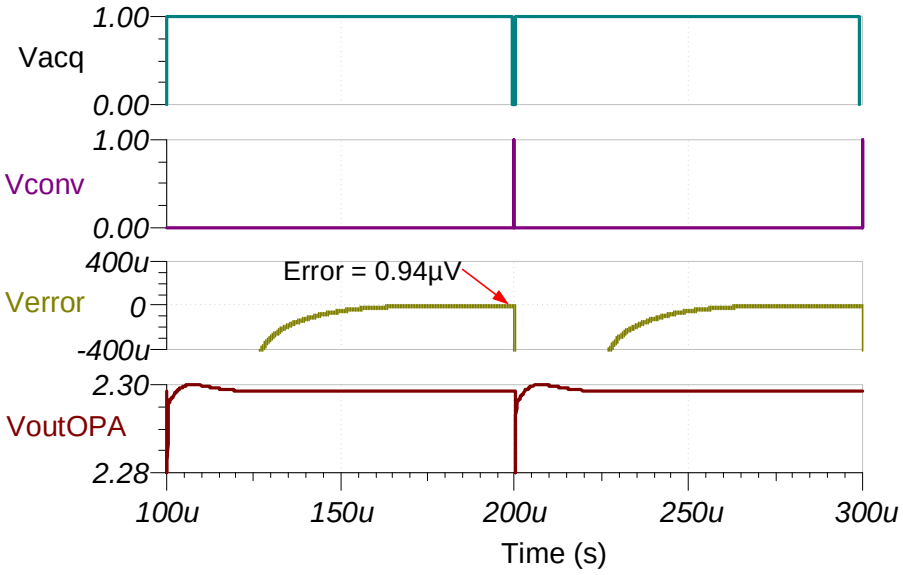
AC Transfer Characteristics

The data sheet specified bandwidth of 33kHz for the INA190A4 closely matches the simulated 35kHz bandwidth. The input ADC filter is designed to minimize charge kickback and does not limit the bandwidth ($f_{c(ADC\ filter)}$ = 312kHz). See *TI Precision Labs - Op Amps: Bandwidth 1* for more details on this subject.



Transient ADC Input Settling Simulation

The transient ADC simulation is performed for a near full scale input (VinADC = 2.3V), for a 100-kHz sampling rate. Note that the sampling rate needed to be adjusted as the INA190 does not have sufficient bandwidth to respond to the transient charge kickback from the ADC at full sampling rate. Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



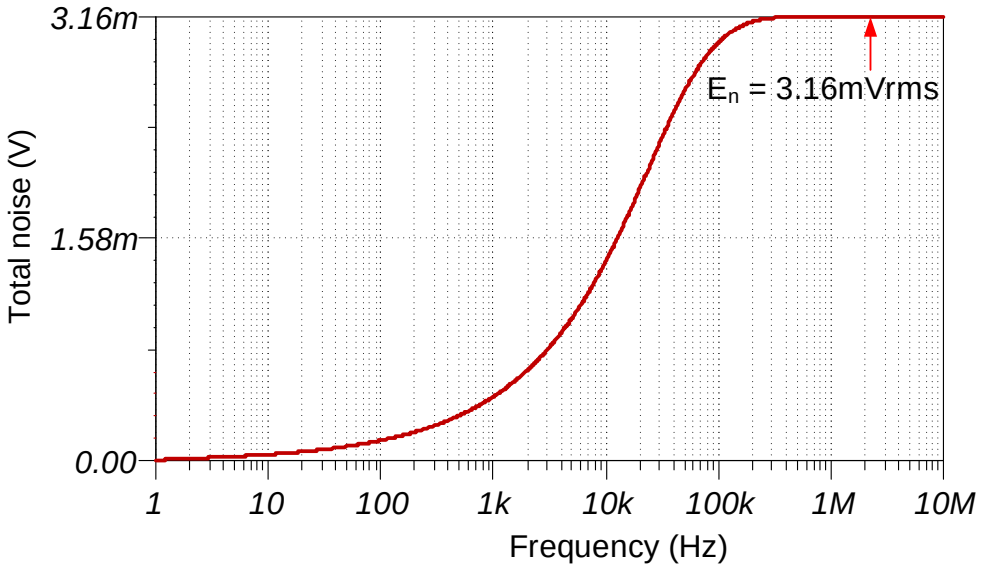
Noise Simulation

The noise hand calculation follows. This calculation assumes that the filter is a first order but inspection of the bandwidth simulation shows a more complex response.

$$E_n = G_n \cdot e_n \cdot \sqrt{K_n \cdot f_c}$$

$$E_n = 200 \cdot 75\,nV/\sqrt{Hz} \cdot \sqrt{1.57 \cdot 35kHz} = 3.5mVrms$$

Note that the calculated and simulated match well. Refer to *TI Precision Labs - Op Amps: Noise 4* for detailed theory on amplifier noise calculations, and Calculating the Total Noise for ADC Systems for data converter noise.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS7042	12-bit resolution, SPI, 1MSPS sample rate, single-ended input, AVDD/Vref input range 1.6V to 3.6V.	http://www.ti.com/product/ADS7042	http://www.ti.com/adcs
INA190	Low Supply voltage (1.7 V to 5.5 V), Wide Common-Mode (-0.2V to 40 V), Low Offset Voltage (Vos<15µV Max), Low Bias Current (500pA typ).	http://www.ti.com/product/INA190	http://www.ti.com/amplifier-circuit/current-sense/analog-output/products.html

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

TINA source files – http://www.ti.com/lit/zip/sbac230.

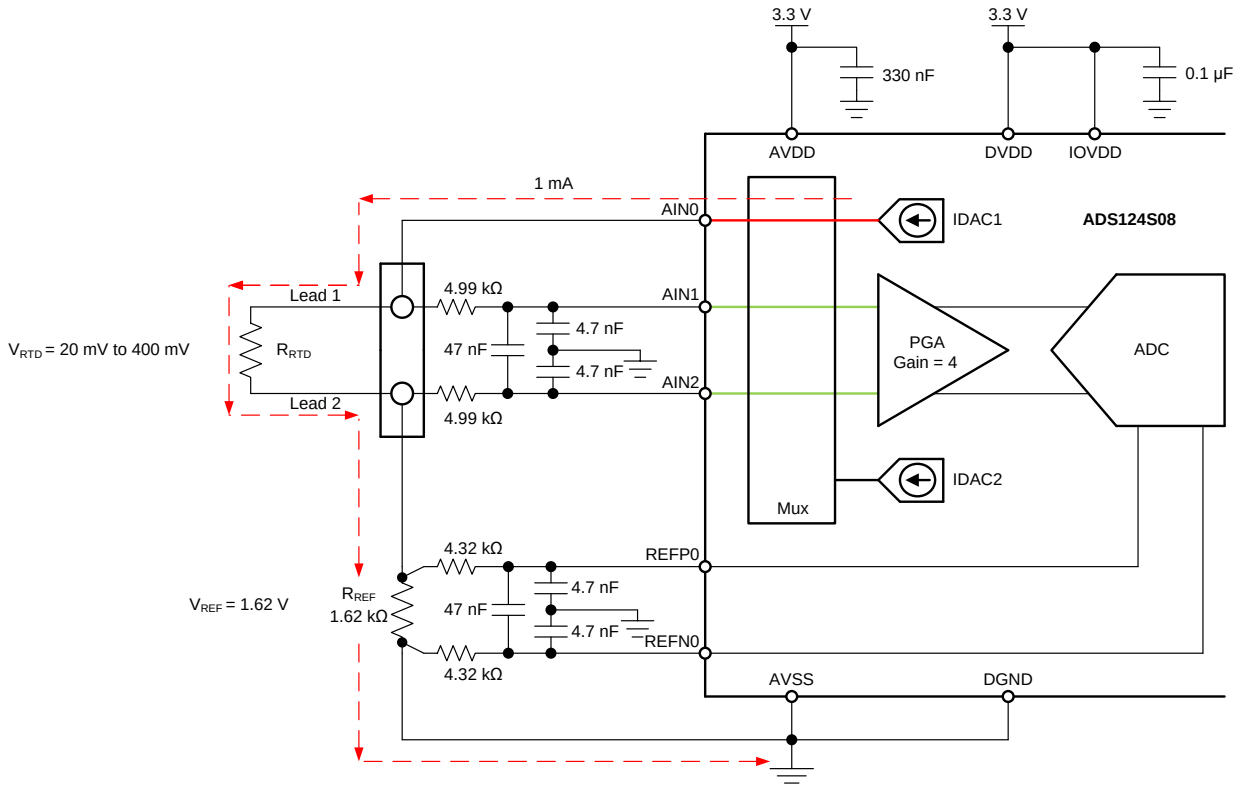
Two-wire PT100 RTD measurement circuit with low-side reference

Joseph Wu

Power Supplies		
AVDD	**AVSS, DGND**	**DVDD, IOVDD**
3.3V	0V	3.3V

Design Description

This cookbook design describes a temperature measurement for a two-wire RTD using the ADS124S08. This design uses a ratiometric measurement for a PT100 type RTD with a temperature measurement range from –200°C to 850°C. Included in this design are ADC configuration register settings and pseudo code to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab instrumentation*, and *factory automation*. For more information about making precision ADC measurements with a variety of RTD wiring configurations, see *A Basic Guide to RTD Measurements*.



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. AVDD must be decoupled with at least a 330-nF capacitor to AVSS. DVDD and IOVDD (when not connected to DVDD) must be decoupled with at least a 0.1-µF capacitor to DGND. See the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet for details on power supply recommendations.
2. Do not route the excitation currents through input filter resistors, using the same pin as an ADC input and as the output for an IDAC current source. Excitation currents reacting with series resistance adds error to the measurement.
3. A 1-µF capacitor is required between REFOUT and REFCOM to enable the internal reference for the IDAC current.
4. Use a precision reference resistor with high accuracy and low drift. Because the measurement is ratiometric, accuracy is dependent on the error of this reference resistor. A 0.01% resistor contributes a gain error similar to that as the ADC.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. An example design and analysis of these filters is found in the *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices* application report.
7. This design shows connections to three input pins of the ADC multiplexer. Remaining analog inputs may be used for RTD, thermocouple, or other measurements.
8. The two-wire RTD measurement is the least accurate of RTD measurements because the lead resistance error cannot be removed. For measurements with more accurate RTD wiring configurations, see *A Basic Guide to RTD Measurements*.

Component Selection

1. Identify the range of operation for the RTD.

   As an example, a PT100 RTD has a range of approximately 20Ω to 400Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full scale range of the measurement.
2. Determine values for the IDAC excitation current and reference resistor.

   The excitation current source in this design is selected to be 1mA. This maximizes the value of the RTD voltage while keeping the self-heating of the RTD low. The typical range of RTD self-heating coefficients is 2.5mW/°C for small, thin-film elements and 65mW/°C for larger, wire-wound elements. With 1-mA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4mW and keeps the measurement errors from self-heating to less than 0.01˚C.

   After selecting the IDAC current magnitude, set R_{REF} = 1620Ω. This sets the reference at 1.62V and the maximum RTD voltage is 400mV. The reference voltage acts as a level shift to place the input measurement to near mid-supply, putting the measurement in the PGA input operating range. With these values, the PGA gain can be set to 4 so that the maximum RTD voltage is near the positive full scale range without exceeding it.

   The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

   Using the maximum RTD resistance, the ADC input voltages are calculated in the following equations.

   $V_{AIN1} = I_{IDAC1} \bullet (R_{RTD} + R_{REF}) = 1mA \bullet (400Ω + 1620Ω) = 2.02V$

   $V_{AIN2} = I_{IDAC1} \bullet R_{REF} = 1mA \bullet 1620Ω = 1.62V$

   $V_{INMAX} = 1mA \bullet 400Ω = 400mV$
3. Verify that the design is within the range of operation of the ADC.

   First, verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given that the gain is 4 and that

AVDD is 3.3V and AVSS is 0V. As the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet shows, the absolute input voltage must satisfy the following:

$AVSS + 0.15V + [|V_{INMAX}| \bullet (Gain - 1) / 2] < V_{AIN1}, V_{AIN2} < AVDD - 0.15V - [|V_{INMAX}| (Gain - 1) / 2]$

$0V + 0.15V + [|V_{INMAX}| \bullet (Gain - 1) / 2] < V_{AIN1}, V_{AIN2} < 3.3V - 0.15V - [|V_{INMAX}| (Gain - 1) / 2]$

$0.75 < V_{AIN1}, V_{AIN2} < 2.55V$

Because the maximum and minimum input voltages seen at AIN1 and AIN2 (2.02 V and 1.62 V) are between 0.75V and 2.55V, the inputs are in the PGA operating range.

Second, verify that the voltage at the IDAC output pin is within the current source compliance voltage. The IDAC pin is AIN0, which have the same voltage as AIN1. At the maximum voltage, V_{AIN0} is 2.02V. As shown in the Electrical Characteristics table in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the output voltage of the IDAC must be between AVSS and AVDD − 0.6V for an IDAC current of 1mA. In this example, with AVDD = 3.3V, the IDAC output must be:

$AVSS < V_{AIN0} = V_{AIN1} < AVDD - 0.6V$

$0V < V_{AIN0} < 2.7V$

With the previous result, the output compliance of the IDAC is satisfied.

4. Select values for the differential and common-mode filtering for the ADC inputs and reference inputs.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering. While series filter resistors offer some amount of input protection, keep the input resistors lower than 10kΩ, to allow for proper input sampling for the ADC.

   With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors be reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

   In this design, the data rate is chosen to be 20SPS using the low-latency filter of the ADS124S08. This filtering provides a low noise measurement with single-cycle settling and the ability to reject 50-Hz and 60-Hz line noise. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations.

   $f_{IN\_DIFF} = 1 / [2 \bullet \pi \bullet C_{IN\_DIFF} (R_{RTD} + 2 \bullet R_{IN})]$

   $f_{IN\_CM} = 1 / [2 \bullet \pi \bullet C_{IN\_CM} (R_{RTD} + R_{IN} + R_{REF})]$

   For the ADC input filtering, R_{IN} = 4.99kΩ, C_{IN_DIFF} = 47nF, and C_{IN_CM} = 4.7nF. This sets the differential filter bandwidth to 330 Hz and the common-mode filter bandwidth to 5kHz.

   Similarly, the bandwidth for the reference input filtering is approximated in the following equations.

   $f_{REF\_DIFF} = 1 / [2 \bullet \pi \bullet C_{REF\_DIFF} \bullet (R_{REF} + 2 \bullet R_{IN\_REF})]$

   $f_{REF\_CM} = 1 / [2 \bullet \pi \bullet C_{REF\_CM} \bullet (R_{REF} + R_{IN\_REF})]$

   For the reference input filtering, R_{IN_REF} = 4.32kΩ, C_{REF_DIFF} = 47nF, and C_{REF_CM} = 4.7nF. This sets the differential filter bandwidth to 330 Hz and the common-mode filter bandwidth to 5.7kHz. Matching the ADC input and reference input filtering may not be possible. However, keeping the bandwidths close may reduce the noise in the measurement.

   For an in-depth analysis of component selection for input filtering, see the *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices* application report.

Measurement Conversion

RTD measurements are typically ratiometric measurements. Using a ratiometric measurement, the ADC output code does not need to be converted to a voltage. This means that the output code gives a measurement only as a ratio of the value of the reference resistor and does not require a precise value for the excitation current. The only requirement is that the current through the RTD and reference resistor are the same.

Equations for the measurement conversion are shown for a 24-bit ADC:

$$\text{Output Code} = 2^{23} \bullet \text{Gain} \bullet (V_{RTD} / V_{REF}) = 2^{23} \bullet \text{Gain} \bullet (I_{IDAC1} \bullet R_{RTD}) / (I_{IDAC1} \bullet R_{REF}) = 2^{23} \bullet \text{Gain} \bullet (R_{RTD} / R_{REF}) \quad (1)$$

$$R_{RTD} = R_{REF} \bullet [\text{Output Code} / (\text{Gain} \bullet 2^{23})] \quad (2)$$

The ADC converts the measurement to the RTD equivalent resistance. Because of non-linearity in the RTD response, the conversion of the resistance to temperature requires an calculation from equation or lookup table. For more information about the conversion of RTD resistance to temperature, see *A Basic Guide to RTD Measurements*.

Register Settings

Configuration Register Settings for a Two-Wire PT100 RTD Measurement Circuit with Low-Side Reference Using the ADS124S08

Register Address	Register Name	Setting	Description
02h	INPMUX	12h	Select AIN_P = AIN1 and AIN_N = AIN2
03h	PGA	0Ah	PGA enabled, Gain = 4
04h	DATARATE	14h	Continuous conversion mode, low-latency filter, 20-SPS data rate
05h	REF	02h	Positive and negative reference buffers enabled, REFP0 and REFN0 reference inputs selected, internal reference always on
06h	IDACMAG	07h	IDAC magnitude set to 1mA
07h	IDACMUX	F0h	IDAC1 set to AIN0, IDAC2 disabled
08h	VBIAS	00h	VBIAS not used for any input
09h	SYS	10h	Normal mode of operation

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS124S0x in continuous conversion mode. The dedicated $\overline{\text{DRDY}}$ pin indicates availability of new conversion data. Pseudo code is shown without the use of the STATUS byte and CRC data verification. ADS124S08 firmware example code is available from the ADS124S08 product folder.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
Set CS low;
    Send 06;    // RESET command to make sure the device is properly reset after power-up
Set CS high;
Set CS low;    // Configure the device
    Send 42    // WREG starting at 02h address
    05    // Write to 6 registers
    12    // Select AINP = AIN1 and AINN = AIN2
    0A    // PGA enabled, Gain = 4
    14    // Continuous conversion mode, low-latency filter, 20-SPS data rate
    02    // Positive and negative reference buffers enabled,
          // REFP0 and REFN0 reference selected, internal reference always on
    07    // IDAC magnitude set to 1 mA
    F0;    // IDAC1 set to AIN0, IDAC2 disabled
Set CS high;
Set CS low;     // For verification, read back configuration registers
    Send 22    // RREG starting at 02h address
    05    // Read from 6 registers
    00 00 00 00 00 00;    // Send 6 NOPs for the read
Set CS high;
Set CS low;
    Send 08;    // Send START command to start converting in continuous conversion mode;
Set CS high;
Loop
    {
    Wait for DRDY to transition low;
    Set CS low;
        Send 12    // Send RDATA command
        00 00 00;    // Send 3 NOPs (24 SCLKs) to clock out data
    Set CS high;
    }
Set CS low;
    Send 0A;    //STOP command stops conversions and puts the device in standby mode;
Set CS to high;
```

RTD Circuit Comparison Table

RTD Circuit Topology	Advantages	Disadvantages
Two-wire RTD, low-side reference	Least expensive	Least accurate, no lead-resistance cancellation
Three-wire RTD, low-side reference, two IDAC current sources	Allows for lead-resistance cancellation	Sensitive to IDAC current mismatch, mismatch can be removed by swapping IDAC currents and averaging two measurements
Three-wire RTD, low-side reference, one IDAC current source	Allows for lead-resistance cancellation	Requires two measurements, first for RTD measurement, second for lead-resistance cancellation
Three-wire RTD, high-side reference, two IDAC current sources	Allows for lead-resistance cancellation, less sensitive to IDAC mismatch than using low side reference	Requires extra resistor for biasing, added voltage may not be compatible with low supply operation
Four-wire RTD, low-side reference	Most accurate, no lead-resistance error	Most expensive

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS124S08	24-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS124S08	Link to similar devices
ADS114S08[(1)]	16-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS114S08	Link to similar devices

(1) The ADS114S08 is a 16-bit version of the ADS124S08 and may be used in similar applications.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, ADS124S08 Evaluation Module
- Texas Instruments, *ADS1x4S08 Evaluation Module User's Guide*
- Texas Instruments, ADS1x4S08 Firmware Example Code
- Texas Instruments, *A Basic Guide to RTD Measurements Application Report*
- Texas Instruments, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices Application Report*

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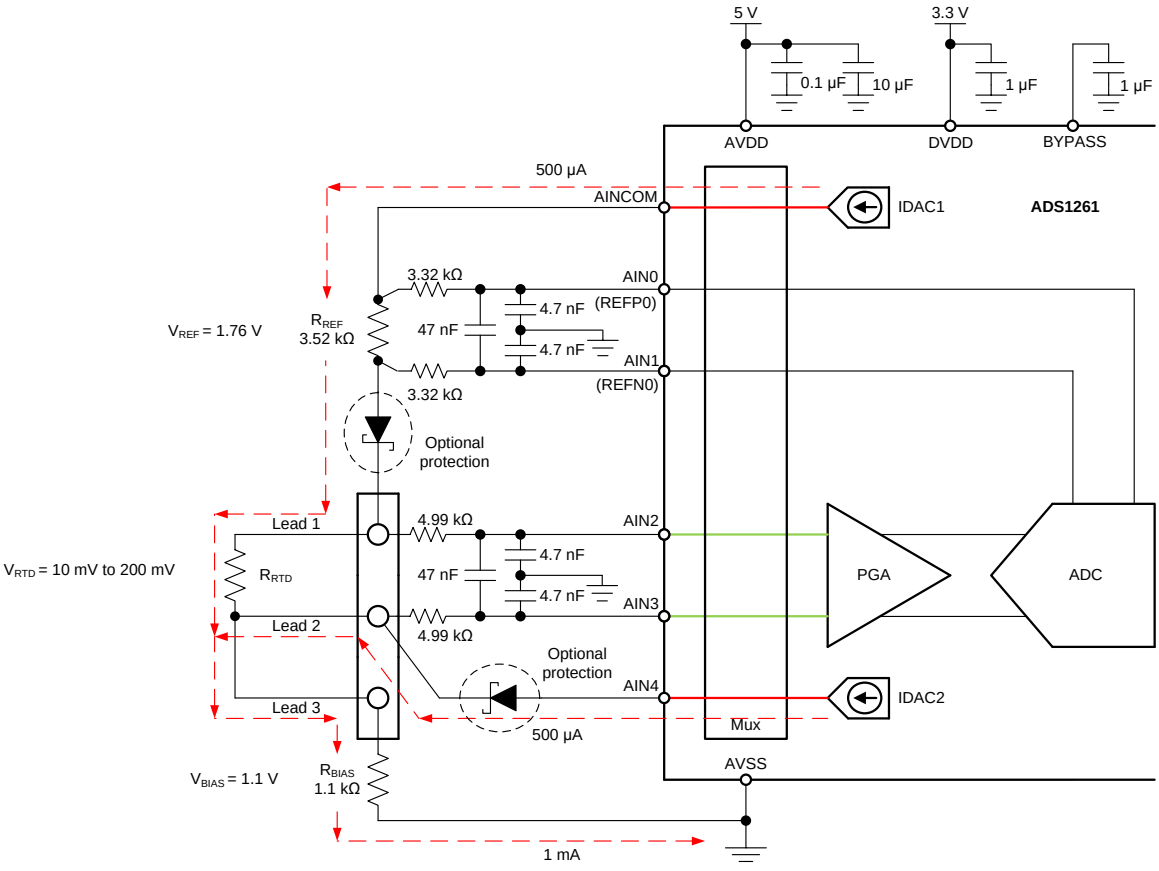
Three-wire PT100 RTD measurement circuit with high-side reference and two IDAC current sources

Joseph Wu, Chris Hall

Power Supplies		
AVDD	**AVSS, DGND**	**DVDD**
5V	0V	3.3V

Design Description

This cookbook design describes a temperature measurement for a three-wire RTD using the ADS1261. This design uses a ratiometric measurement with a high-side reference using two matched excitation current sources for a PT100 type RTD with a temperature measurement range from –200°C to 850°C. Included in this design are ADC configuration register settings and pseudo code to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab instrumentation*, and *factory automation*. For more information about making precision ADC measurements with a variety of RTD wiring configurations, see *A Basic Guide to RTD Measurements*.



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. Place 0.1-µF and 10-µF capacitors between AVDD and AVSS (ground). Connect a 1-µF capacitor from DVDD to the ground plane. Connect a 1-µF capacitor from BYPASS to the ground plane. See the ADS126x Precision, 5-Channel and 10-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADCs With PGA and Monitors data sheet for details on power-supply recommendations.
2. Do not route the excitation currents through input filter resistors, using the same pin as an ADC input and as the output for an IDAC current source. Excitation currents reacting with series resistance adds error to the measurement.
3. A 10-µF capacitor is required between REFOUT and REFCOM to enable the internal reference for the IDAC current.
4. Use a precision reference resistor with high accuracy and low drift. Because the measurement is ratiometric, accuracy is dependent on the error of this reference resistor. A 0.01% resistor contributes a gain error similar to that as the ADC.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. An example design and analysis of these filters is found in *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.
7. This design shows connections to six input pins of the ADC multiplexer. Remaining analog inputs may be used for other measurements, such as bridge measurements with AC excitation.
8. Because of lead-resistance cancellation, the three-wire measurement offers more accuracy than comparable two-wire RTD measurements. Using a high-side reference for this design significantly reduces the error from IDAC current mismatch seen in three-wire RTD measurements using a low-side reference. For measurements with other RTD wiring configurations, see *A Basic Guide to RTD Measurements*.

Component Selection

1. Identify the range of operation for the RTD.

   As an example, a PT100 RTD has a range of approximately 20Ω to 400Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full scale range of the measurement.

2. Use two matched IDAC current sources to cancel the lead-resistance error.

   Two matched IDAC current sources are used for lead-resistance cancellation. Assuming the resistances of lead 1 and lead 2 are the same, and the currents of IDAC1 and IDAC2 are the same, then the lead-resistance error is cancelled. Cancellation can be shown through the measured voltages at AIN2 and AIN3.

   IDAC1 drives current into the reference resistor R_{REF} and the RTD through lead 1. IDAC2 drives current into lead 2. First, assume that the input protection shown in the circuit has no voltage drop. The voltages at AIN2 and AIN3 are calculated with the following equations.

   $$V_{AIN2} = I_{IDAC1} \bullet (R_{LEAD1} + R_{RTD}) + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{BIAS})$$

   $$V_{AIN3} = I_{IDAC2} \bullet R_{LEAD2} + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{BIAS})$$

   The measurement of the ADC is the difference between AIN2 and AIN3, which is the subtraction of the previous equations.

   $$V_{AIN2} - V_{AIN3} = [I_{IDAC1} \bullet (R_{LEAD1} + R_{RTD} + R_{BIAS}) + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{BIAS})] - [I_{IDAC2} \bullet R_{LEAD2} + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{BIAS})]$$

   Then, the R_{LEAD3} and R_{BIAS} terms drop out.

   $$V_{AIN2} - V_{AIN3} = I_{IDAC1} \bullet (R_{LEAD1} + R_{RTD}) - I_{IDAC2} \bullet R_{LEAD2}$$

   If R_{LEAD1} and R_{LEAD2} are equal and I_{IDAC1} and I_{IDAC2} are equal (to become I_{IDAC}), then the lead resistance errors cancel to leave the following equation:

   $$V_{AIN2} - V_{AIN3} = I_{IDAC} \bullet R_{RTD}$$

3. Determine values for the IDAC excitation currents and reference resistor.

   The excitation current source in this design is selected to be 500μA. This maximizes the value of the RTD voltage while keeping the self-heating of the RTD low. The typical range of RTD self-heating coefficients is 2.5mW/°C for small, thin-film elements and 65mW/°C for larger, wire wound elements. With 500-μA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4mW and keeps the measurement errors from self-heating to less than 0.005°C.

   After selecting the IDAC current magnitude, set R_{REF} = 3.52kΩ. Using a 500-μA excitation current sets the reference at 1.76V and the maximum RTD voltage is 200mV. With these values, the PGA gain can be set to 8 so that the maximum RTD voltage is near the positive full scale range without exceeding it.

   The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in R_{REF} reflects the same error in the RTD measurement. The REFP and REFN pins (AIN0 and AIN1) are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

   Note that for a high-side reference, the current flowing through the reference resistor and the RTD are the same. For a three-wire RTD measurement with a low-side reference, the IDAC current mismatch is a large contributor to the error. In this design, the mismatch only leads to a smaller error in the lead-resistor cancellation, rather than a larger gain error in the RTD measurement.

4. Set R_{BIAS} and verify that the design is within the range of operation of the ADC.

   Once the reference resistance, IDAC current magnitudes, and ADC gain are set, select the R_{BIAS} resistance to set the bias voltage of the input measurement. Normally, R_{BIAS} is selected to set the input to the mid-supply voltage. However, there is a large total sum of the voltage drop across the reference resistor, the RTD resistance, the bias resistor, and any optional input protection used in the circuit. It is important that the R_{BIAS} input offset is high enough to keep the RTD measurement voltage in the PGA input range, but not too high so that the excitation current output pin is within the compliance voltage of the IDAC.

   Setting R_{BIAS} of 1.1kΩ meets this requirement. Using the maximum RTD resistance of 400Ω, the ADC input voltages are calculated in the following equations. The small lead resistances can be ignored for this calculation.

   $V_{AIN2} = (I_{IDAC1} \bullet R_{RTD}) + [(I_{IDAC1} + I_{IDAC2}) \bullet R_{BIAS}] = 1.3V$

   $V_{AIN3} = (I_{IDAC1} + I_{IDAC2}) \bullet R_{BIAS} = 1mA \bullet 1.1k\Omega = 1.1V$

   $V_{INMAX} = 500\mu A \bullet 400\Omega = 200mV$

   First, verify that the voltage at AIN2 and AIN3 are within the input range of the PGA given that the gain is 8 and that AVDD is 5V and AVSS is 0V. As shown in the ADS126x Precision, 5-Channel and 10-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADCs With PGA and Monitors data sheet, the absolute input voltage must satisfy the following:

   $AVSS + 0.3V + [|V_{INMAX}| \bullet (Gain - 1) / 2] < V_{AIN2}, V_{AIN3} < V_{AVDD} - 0.3V - [|V_{INMAX}| \bullet (Gain - 1) / 2]$

   $0.3V + [|0.2V| \bullet (8 - 1) / 2] < V_{AIN2}, V_{AIN3} < 5V - 0.3V - [|0.2V| \bullet (8 - 1) / 2]$

   $1V < V_{AIN2}, V_{AIN3} < 4V$

   Because the maximum and minimum input voltage seen at AIN2 and AIN2 (1.1V and 1.3V) are between 1V and 4V, the inputs are in the PGA operating range.

   Second, verify that the IDAC output pin voltages are within the compliance voltage. The IDAC current output voltage is highest and most limited by output compliance when the RTD voltage is at a maximum as the following equation shows. As before, we can ignore the low voltage contribution of the lead resistance.

   $V_{IDAC1} = V_{BIAS} + V_{RTD} + V_D + V_{REF}$

   $V_{IDAC1} = 1V + 0.2V + 0.3V + 1.76V = 3.26V$

   The maximum RTD voltage is 200mV and a drop of 300mV is assumed for an input protection Schottky diode (V_D).

   The IDAC current compliance range is listed in the *Electrical Characteristics* table under the *Current Sources* section of the ADS126x Precision, 5-Channel and 10-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADCs With PGA and Monitors data sheet. The IDAC current compliance range is given by the following equation.

   $AVSS < V_{IDAC1} < AVDD - 1.1V$

In this example design, AVDD is 5V and reduces the following:

$0V < V_{IDAC1} < 3.9V$

With the previous equation, the output compliance of the IDAC1 pin is satisfied. Because the IDAC2 pin is always at a lower voltage than IDAC1 voltage, both current sources are in the compliance range.

The schematic is shown with two optional input protection diodes. These low V_F diodes provide input fault protection for the IDAC current sources, and may be replaced with series resistances. If series resistance is used, then the added diode voltage of 0.3V is replaced with the voltage from I_{IDAC} across the new series resistance for equations verifying the IDAC output pin compliance voltage.

Third, verify that the reference voltage is within the reference voltage input range for the ADC. For the ADS1261, the differential reference input voltage range is shown in the *Recommended Operating Conditions* of the ADS126x Precision, 5-Channel and 10-Channel, 40-kSPS, 24-Bit, Delta-Sigma ADCs With PGA and Monitors data sheet as the following equation.

$0.9V < V_{REFP} – V_{REFN} < AVDD – AVSS$

$0.9V < 1.76V < 5V$

Also verify the absolute negative reference input voltage and verify the absolute positive reference input voltage with the following equations. Calculations show that the reference voltages are within the input range of the ADC reference.

$AVSS – 0.05V < V_{REFN} = V_{BIAS} + V_{RTD} + V_D < V_{REFP} – 0.9V$

$–0.05V < 1.5V < 4.1V$

$V_{REFN} < V_{REFP} = V_{BIAS} + V_{RTD} + V_D + V_{REF} < AVDD + 0.05V$

$1.5V < 3.26V < 5.05V$

5. Select values for the differential and common-mode input filtering for the ADC inputs and reference inputs.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering. While series filter resistors offer some amount of input protection, keep the input resistors lower than 10kΩ, to allow for proper input sampling for the ADC.

   With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors be reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

   In this design, the data rate is chosen to be 20SPS using the low-latency filter of the ADS1261. This filtering provides a low noise measurement with single-cycle settling and the ability to reject 50-Hz and 60-Hz line noise. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations.

   $f_{IN\_DIFF} = 1 / [2 • \pi • C_{IN\_DIFF} (R_{RTD} + 2 • R_{IN})]$

   $f_{IN\_CM} = 1 / [2 • \pi • C_{IN\_CM} (R_{RTD} + R_{IN} + R_{BIAS})]$

   For the ADC input filtering, R_{IN} = 4.99kΩ, C_{IN_DIFF} = 47nF, and C_{IN_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5.4kHz.

   Similarly, the bandwidth for the reference input filtering is approximated in the following equations.

   $f_{REF\_DIFF} = 1 / [2 • \pi • C_{REF\_DIFF} • (R_{REF} + 2 • R_{IN\_REF})]$

   $f_{REF\_CM} = 1 / \{2 • \pi • C_{REF\_CM} • [R_{IN\_REF} + (½ • R_{REF}) + R_{RTD} + R_{BIAS}]\}$

   For the reference input filtering, R_{IN_REF} = 3.32kΩ, C_{REF_DIFF} = 47nF, and C_{REF_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5.3kHz. Matching the ADC input and reference input filtering is not always possible in a design. However, keeping the bandwidths close may reduce noise in the measurement.

   For an in-depth analysis of component selection for input filtering, see *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.

Measurement Conversion

RTD measurements are typically ratiometric measurements. Using a ratiometric measurement, the ADC output code does not need to be converted to a voltage. This means that the output code gives a measurement only as a ratio of the value of the reference resistor and does not require a precise value for the excitation current. The only requirement is that the current through the RTD and reference resistor are the same.

Equations for the measurement conversion are shown for a 24-bit ADC:

$$\text{Output Code} = 2^{23} \bullet \text{Gain} \bullet (V_{RTD} / V_{REF}) = 2^{23} \bullet \text{Gain} \bullet (I_{IDAC1} \bullet R_{RTD}) / (I_{IDAC1} \bullet R_{REF}) = 2^{23} \bullet \text{Gain} \bullet (R_{RTD} / R_{REF})$$

$$R_{RTD} = R_{REF} \bullet [\text{Output Code} / (\text{Gain} \bullet 2^{23})]$$

The ADC converts the measurement to the RTD equivalent resistance. Because of non-linearity in the RTD response, the conversion of the resistance to temperature requires an calculation from equation or lookup table. For more information about the conversion of RTD resistance to temperature, see *A Basic Guide to RTD Measurements*.

Register Settings

Configuration Register Settings for a 3-Wire RTD Measurement with High-Side Reference and Two IDAC Current Sources Using the ADS1261

Register Address	Register Name	Setting	Description
02h	MODE0	24h	20SPS, FIR digital filter
03h	MODE1	01h	Normal mode, Continuous conversion, 50 μs delay between conversions
04h	MODE2	00h	GPIOs disabled
05h	MODE3	00h	No power-down, no STATUS or CRC byte, timeout disabled
06h	REF	1Ah	Internal reference enabled, REFP = AIN0, REFN = AIN1
0Dh	IMUX	4Ah	IDAC2 = AIN4, IDAC1 = AINCOM
0Eh	IMAG	44h	IMAG2 = IMAG1 = 500μA
0Fh	RESERVED	00h	Reserved
10h	PGA	03h	PGA enabled, Gain = 8
11h	INPMUX	34h	Select AIN_P = AIN2 and AIN_N = AIN3
12h	INPBIAS	00h	VBIAS voltages and burnout current sources disabled

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS1261 in continuous conversion mode. The dedicated $\overline{\text{DRDY}}$ pin indicates availability of new conversion data. Pseudo code is shown without the use of the STATUS byte and CRC data verification. ADS1261 example code is available from the ADS1261 product folder.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
Set CS low;
    Send 06;    //RESET command to make sure the device is properly reset after power-up
Set CS high;
Set CS low;    // Configure the device
    Send 42    // WREG starting at 02h address
    04    // Write to 5 registers
    24    // 20SPS, FIR digital filter
    01    // Normal mode, Continuous conversion, 50µs delay between conversions
    00    // GPIOs disabled
    00    // No power-down, no STATUS or CRC byte, timeout disabled
    1A;    // Internal reference enabled, REFP = AIN0, REFN = AIN1
Set CS high;
Set CS low;    // Configure the device, IDACs
    Send 4D    // WREG starting at 0Dh address
    05    // Write to 6 registers
    4A    // IMUX2 = AIN4, IMUX1 = AINCOM
    44    // IMAG2 = IMAG1 = 500µA
    00    // RESERVED
    03    // PGA enabled, Gain = 8
    34    // Select AINP = AIN2 and AINN = AIN3
    00;    // VBIAS voltages and burn-out current sources disabled
Set CS high;
Set CS low;    // For verification, read back configuration registers
    Send 22    // RREG starting at 02h address
    10    // Read from 17 registers
    00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00;    // Send 17 NOPs for the read
Set CS high;
Set CS low;
    Send 08;    // Send START command to start converting in continuous conversion mode;
Set CS high;
Loop
    {
    Wait for DRDY to transition low;
    Set CS low;
        Send 12    // Send RDATA command
        00 00 00;    // Send 3 NOPs (24 SCLKs) to clock out data
    Set CS high;
    }
Set CS low;
Send 0A;    //STOP command stops conversions and puts the device in standby mode;
Set CS to high;
```

RTD Circuit Comparison Table

RTD Circuit Topology	Advantages	Disadvantages
Two-wire RTD, low-side reference	Least expensive	Least accurate, no lead-resistance cancellation
Three-wire RTD, low-side reference, two IDAC current sources	Allows for lead-resistance cancellation	Sensitive to IDAC current mismatch, mismatch can be removed by swapping IDAC currents and averaging two measurements
Three-wire RTD, low-side reference, one IDAC current source	Allows for lead-resistance cancellation	Requires two measurements, first for RTD measurement, second for lead-resistance cancellation
Three-wire RTD, high-side reference, two IDAC current sources	Allows for lead-resistance cancellation, less sensitive to IDAC mismatch than using low side reference	Requires extra resistor for biasing, added voltage may not be compatible with low supply operation
Four-wire RTD, low-side reference	Most accurate, no lead-resistance error	Most expensive

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS1261	24-bit 40kSPS 10-ch delta-sigma ADC w/ PGA, Vref, 2 × IDACs, and AC excitation for factory automation	http://www.ti.com/product/ADS1261	Link to similar devices Link to similar 16-bit devices

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, ADS1261 Evaluation Module
- Texas Instruments, *ADS1261 and ADS1235 Evaluation Module User's Guide*
- Texas Instruments, ADS1261 Example C Code Software
- Texas Instruments, *A Basic Guide to RTD Measurements*
- Texas Instruments, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*

For direct support from TI Engineers use the E2E community:

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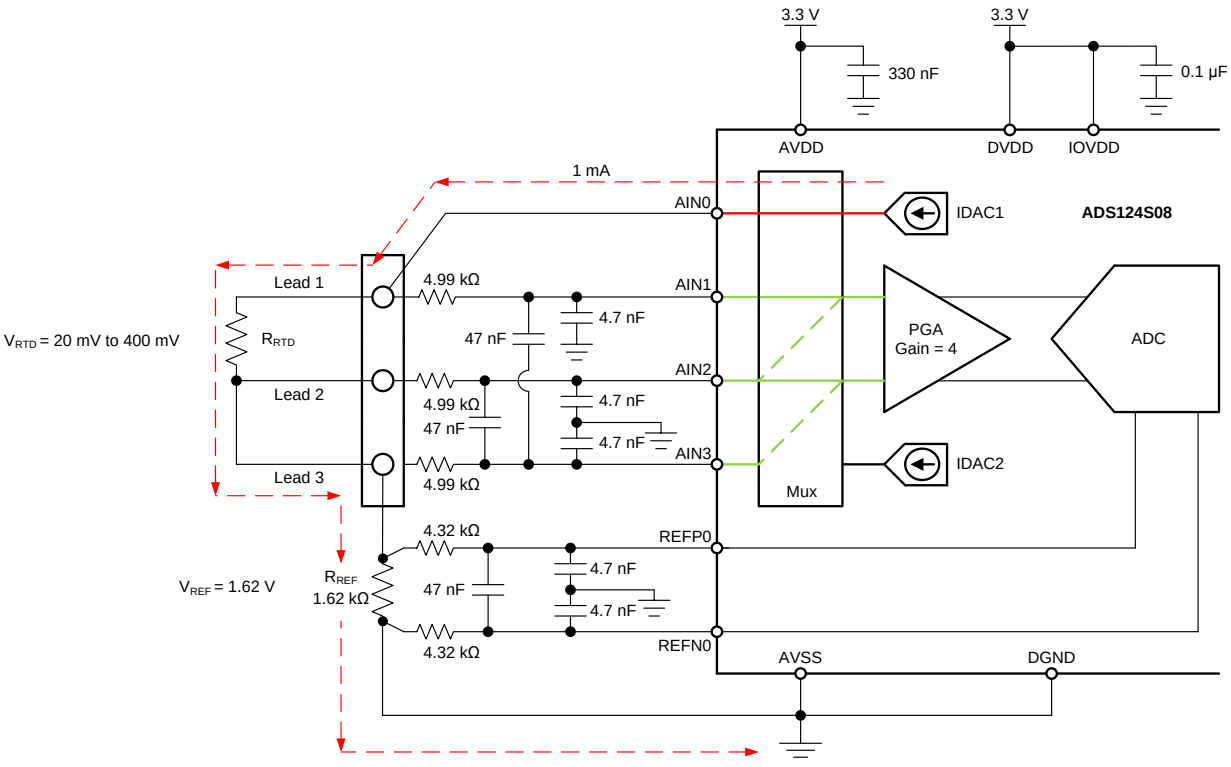
Three-wire PT100 RTD measurement circuit with low-side reference and one IDAC current source

Joseph Wu

Power Supplies		
AVDD	**AVSS, DGND**	**DVDD, IOVDD**
3.3V	0V	3.3V

Design Description

This cookbook design describes a temperature measurement for a three-wire RTD with a low-side reference using the ADS124S08. In comparison to a *Three-Wire PT100 RTD Measurement Circuit With Low- Side Reference and Two IDAC Current Sources* with a single measurement, this design uses a single IDAC excitation current source and a second measurement to remove the lead resistance error. This design uses a ratiometric measurement for a PT100 type RTD with a temperature measurement range from –200°C to 850°C. Included in this design are ADC configuration register settings and pseudo code to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab instrumentation*, and *factory automation*. For more information about making precision ADC measurements with a variety of RTD wiring configurations, see *A Basic Guide to RTD Measurements*.



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. AVDD must be decoupled with at least a 330-nF capacitor to AVSS. DVDD and IOVDD (when not connected to DVDD) must be decoupled with at least a 0.1-µF capacitor to DGND. See the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet for details on power supply recommendations.
2. Do not route the excitation currents through input filter resistors, using the same pin as an ADC input and as the output for an IDAC current source. Excitation currents reacting with series resistance adds error to the measurement.
3. A 1-µF capacitor is required between REFOUT and REFCOM to enable the internal reference for the IDAC current.
4. Use a precision reference resistor with high accuracy and low drift. Because the measurement is ratiometric, accuracy is dependent on the error of this reference resistor. A 0.01% resistor contributes a gain error similar to that as the ADC.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. An example design and analysis of these filters is found in *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.
7. This design shows connections to four input pins of the ADC multiplexer. Remaining analog inputs may be used for RTD, thermocouple, or other measurements.
8. The three-wire RTD measurement offers more accuracy than comparable two-wire RTD measurements but also gives better immunity from the IDAC current mismatch than with a three-wire RTD measurement using matched IDAC current sources. For measurements with other RTD wiring configurations, see *A Basic Guide to RTD Measurements*.

Component Selection

1. Identify the range of operation for the RTD.

   As an example, a PT100 RTD has a range of approximately 20Ω to 400Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full scale range of the measurement.
2. Determine values for the IDAC excitation current and reference resistor.

   Start with a design where the excitation current is driven into lead 1 of the RTD, flowing through the RTD, and out the RTD through lead 3. At this point, ignore the lead resistance error, so that the measurement from AIN1 to AIN2 only measures the RTD resistance.

   The excitation current source in this design is selected to be 1mA. This maximizes the value of the RTD voltage while keeping the self-heating of the RTD low. The typical range of RTD self-heating coefficients is 2.5mW/°C for small, thin-film elements and 65mW/°C for larger, wire-wound elements. With 1-mA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4mW and keeps the measurement errors from self-heating to less than 0.01˚C.

   After selecting the IDAC current magnitude, set R_{REF} = 1620Ω. This sets the reference at 1.62V and the maximum RTD voltage is 400mV. The reference voltage acts as a level shift to place the input measurement to near mid-supply, putting the measurement in the PGA input operating range. With these values, the PGA gain can be set to 4 so that the maximum RTD voltage is near the positive full scale range without exceeding it.

   The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

   Using the maximum RTD resistance, the ADC input voltages are calculated in the following equations. The small lead resistances can be ignored for this calculation.

$V_{AIN1} = I_{IDAC1} \bullet (R_{RTD} + R_{REF}) = 1mA \bullet (400\Omega + 1620\Omega) = 2.02V$

$V_{AIN2} = I_{IDAC1} \bullet R_{REF} = 1mA \bullet 1620\Omega = 1.62V$

$V_{INMAX} = 1mA \bullet 400\Omega = 400mV$

3. Verify that the design is within the range of operation of the ADC.

   First, verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given that the gain is 4 and that AVDD is 3.3V and AVSS is 0V. As shown in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the absolute input voltage must satisfy the following:

   $AVSS + 0.15V + [|V_{INMAX}| \bullet (Gain - 1) / 2] < V_{AIN1}, V_{AIN2} < AVDD - 0.15V - [|V_{INMAX}| (Gain - 1) / 2]$

   $0V + 0.15V + [|V_{INMAX}| \bullet (Gain - 1) / 2] < V_{AIN1}, V_{AIN2} < 3.3V - 0.15V - [|V_{INMAX}| (Gain - 1) / 2]$

   $0.75V < V_{AIN1}, V_{AIN2} < 2.55\ V$

   Because the maximum and minimum input voltages seen at AIN1 and AIN2 (2.02V and 1.62V) are between 0.75V and 2.55V, the inputs are in the PGA operating range.

   Second, verify that the voltage at the IDAC output pin is within the current source compliance voltage. The IDAC pin is AIN0, which have the same voltage as AIN1. At the maximum voltage, V_{AIN0} is 2.02V. As shown in the Electrical Characteristics table in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the output voltage of the IDAC must be between AVSS and AVDD − 0.6V for an IDAC current of 1mA. In this example, with AVDD = 3.3V, the IDAC output must be:

   $AVSS < V_{AIN0} = V_{AIN1} < AVDD - 0.6V$

   $0V < V_{AIN0} < 2.7V$

   With the previous result, the output compliance of the IDAC is satisfied.

4. Use two different measurements to measure the RTD resistance and cancel the lead-resistance error.

   The first measurement of the ADC is measured across AIN1 and AIN2, with the lead resistances included.

   $Measurement\ 1 = V_{AIN1} - V_{AIN2} = I_{IDAC1} \bullet (R_{RTD} + R_{LEAD1})$

   Because the IDAC current does not pass through lead 2, its resistance is never part of the measurement. The input multiplexer of the ADC is then set to make a second measurement across AIN2 and AIN3. This measures the voltage drop across the resistance from lead 3.

   $Measurement\ 2 = V_{AIN2} - V_{AIN3} = I_{IDAC1} \bullet R_{LEAD3}$

   Measurement 2 is subtracted from measurement 1 to get the following result.

   $Measurement\ 1 - Measurement\ 2 = [I_{IDAC1} \bullet (R_{RTD} + R_{LEAD1})] - (I_{IDAC1} \bullet R_{LEAD3})$

   If the lead resistances are equal, then the lead-resistance error drops out to get the final result.

   $Measurement\ 1 - Measurement\ 2 = I_{IDAC1} \bullet R_{RTD}$

5. Select values for the differential and common-mode filtering for the ADC inputs and reference inputs.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering. While series filter resistors offer some amount of input protection, keep the input resistors lower than 10 kΩ, to allow for proper input sampling for the ADC.

   With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors be reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

   In this design, the data rate is chosen to be 20SPS using the low-latency filter of the ADS124S08. This filtering provides a low noise measurement with single-cycle settling and the ability to reject 50-Hz and 60-Hz line noise. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations.

   $f_{IN\_DIFF} = 1 / [2 \bullet \pi \bullet C_{IN\_DIFF} (R_{RTD} + 2 \bullet R_{IN})]$

   $f_{IN\_CM} = 1 / [2 \bullet \pi \bullet C_{IN\_CM} (R_{RTD} + R_{IN} + R_{REF})]$

   For the ADC input filtering, R_{IN} = 4.99kΩ, C_{IN_DIFF} = 47nF, and C_{IN_CM} = 4.7nF. This sets the differential

filter bandwidth to 330Hz and the common-mode filter bandwidth to 5kHz.

Similarly, the bandwidth for the reference input filtering is approximated in the following equations.

$f_{REF\_DIFF} = 1 / [2 \cdot \pi \cdot C_{REF\_DIFF} \cdot (R_{REF} + 2 \cdot R_{IN\_REF})]$

$f_{REF\_CM} = 1 / [2 \cdot \pi \cdot C_{REF\_CM} \cdot (R_{REF} + R_{IN\_REF})]$

For the reference input filtering, R_{IN_REF} = 4.32kΩ, C_{REF_DIFF} = 47nF, and C_{REF_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5.7kHz. Matching the ADC input and reference input filtering may not be possible. However, keeping the bandwidths close may reduce the noise in the measurement.

For an in-depth analysis of component selection for input filtering, see *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.

Measurement Conversion

RTD measurements are typically ratiometric measurements. Using a ratiometric measurement, the ADC output code does not need to be converted to a voltage. This means that the output code gives a measurement only as a ratio of the value of the reference resistor and does not require a precise value for the excitation current. The only requirement is that the current through the RTD and reference resistor are the same.

Equations for the measurement conversion are shown for a 24-bit ADC. First, the result from measurement 1 is shown.

$\text{Output Code 1} = 2^{23} \cdot \text{Gain} \cdot [(V_{RTD} + V_{LEAD1}) / V_{REF}] = 2^{23} \cdot \text{Gain} \cdot [I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1})] / (I_{IDAC1} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot [(R_{RTD} + R_{LEAD1}) / R_{REF}]$

$R_{RTD} + R_{LEAD1} = R_{REF} \cdot [\text{Output Code} / (\text{Gain} \cdot 2^{23})]$

Then the result from measurement 2 is shown.

$\text{Output Code 2} = 2^{23} \cdot \text{Gain} \cdot (V_{LEAD3} / V_{REF} = 2^{23} \cdot \text{Gain} \cdot (I_{IDAC1} \cdot R_{LEAD3}) / (I_{IDAC1} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot (R_{LEAD1} / R_{REF})$

$R_{LEAD3} = R_{REF} \cdot [\text{Output Code} / (\text{Gain} \cdot 2^{23})]$

If the lead resistances are assumed to be equal, then the subtract the result of measurement 2 from measurement 1 to get the equivalent RTD resistance.

$R_{RTD} = R_{REF} \cdot [(\text{Output Code 1} - \text{Output Code 2}) / (\text{Gain} \cdot 2^{23})]$

The ADC converts the measurement to the RTD equivalent resistance. Because of non-linearity in the RTD response, the conversion of the resistance to temperature requires an calculation from equation or lookup table. For more information about the conversion of RTD resistance to temperature, see *A Basic Guide to RTD Measurements*.

Register Settings

Configuration Register Settings for a Three-Wire PT100 RTD Measurement Circuit with Low-Side Reference and One IDAC Current Source Using the ADS124S08

Register Address	Register Name	Setting	Description
02h[(1)]	INPMUX	12h	Select AIN_P = AIN1 and AIN_N = AIN2
03h	PGA	0Ah	PGA enabled, Gain = 4
04h	DATARATE	14h	Continuous conversion mode, low-latency filter, 20-SPS data rate
05h	REF	02h	Positive and negative reference buffers enabled, REFP0 and REFN0 reference inputs selected, internal reference always on
06h	IDACMAG	07h	IDAC magnitude set to 1mA
07h	IDACMUX	F0h	IDAC1 set to AIN0, IDAC2 disabled
08h	VBIAS	00h	VBIAS not used for any input
09h	SYS	10h	Normal mode of operation
02h[(2)]	INPMUX	23h	Select AINP = AIN2 and AINN = AIN3

(1) This input multiplexer setting is for measurement 1.

(2) This input multiplexer setting is for measurement 2, as a measurement of the lead-resistance error.

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS124S0x in continuous conversion mode. The dedicated $\overline{\text{DRDY}}$ pin indicates availability of new conversion data. Pseudo code is shown without the use of the STATUS byte and CRC data verification. ADS124S08 firmware example code is available from the ADS124S08 product folder.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
Set CS low;
    Send 06;    // RESET command to make sure the device is properly reset after power-up
Set CS high;
Set CS low;    // Configure the device
    Send 42    // WREG starting at 02h address
    05    // Write to 6 registers
    12    // Select AINP = AIN1 and AINN = AIN2
    0A    // PGA enabled, Gain = 4
    14    // Continuous conversion mode, low-latency filter, 20-SPS data rate
    02    // Positive and negative reference buffers enabled,
          // REFP0 and REFN0 reference selected, internal reference always on
    07    // IDAC magnitude set to 1mA
    F0;    // IDAC1 set to AIN0, IDAC2 disabled
Set CS high;
Set CS low;     // For verification, read back configuration registers
    Send 22    // RREG starting at 02h address
    05    // Read from 6 registers
    00 00 00 00 00 00;    // Send 6 NOPs for the read
Set CS high;
Set CS low;
    Send 08;    // Send START command to start converting in continuous conversion mode;
Set CS high;
Loop
    {
    Set CS low;    // Configure the device for measurement 1
    Send 42    // WREG starting at 02h address
        00    // Write to 1 register
        12;    // Select AINP = AIN1 and AINN = AIN2
    Set CS high;
    Wait for DRDY to transition low;
    Set CS low;
        Send 12    // Send RDATA command
        00 00 00;    // Send 3 NOPs (24 SCLKs) to clock out data
    Set CS high;
    Set CS low;    // Configure the device for measurement 2
    Send 42    // WREG starting at 02h address
        00    // Write to 1 register
        23;    // Select AINP = AIN2 and AINN = AIN3
    Set CS high;
    Wait for DRDY to transition low;
    Set CS low;
        Send 12    // Send RDATA command
        00 00 00;    // Send 3 NOPs (24 SCLKs) to clock out data
    Set CS high;
    Subtract measurement 2 from measurement 1;    // Remove lead-resistance error
    }
Set CS low;
    Send 0A;    //STOP command stops conversions and puts the device in standby mode;
Set CS to high;
```

RTD Circuit Comparison Table

RTD Circuit Topology	Advantages	Disadvantages
Two-wire RTD, low-side reference	Least expensive	Least accurate, no lead-resistance cancellation
Three-wire RTD, low-side reference, two IDAC current sources	Allows for lead-resistance cancellation	Sensitive to IDAC current mismatch, mismatch can be removed by swapping IDAC currents and averaging two measurements
Three-wire RTD, low-side reference, one IDAC current source	Allows for lead-resistance cancellation	Requires two measurements, first for RTD measurement, second for lead-resistance cancellation
Three-wire RTD, high-side reference, two IDAC current sources	Allows for lead-resistance cancellation, less sensitive to IDAC mismatch than using low side reference	Requires extra resistor for biasing, added voltage may not be compatible with low supply operation
Four-wire RTD, low-side reference	Most accurate, no lead-resistance error	Most expensive

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS124S08	24-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS124S08	Link to similar devices
ADS114S08 (1)	16-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS114S08	Link to similar devices

(1) The ADS114S08 is a 16-bit version of the ADS124S08 and may be used in similar applications.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, ADS124S08 Evaluation Module
- Texas Instruments, *ADS1x4S08 Evaluation Module User's Guide*
- Texas Instruments, ADS1x4S08 Firmware Example Code
- Texas Instruments, *A Basic Guide to RTD Measurements*
- Texas Instruments, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*

For direct support from TI Engineers use the E2E community:

e2e.ti.com

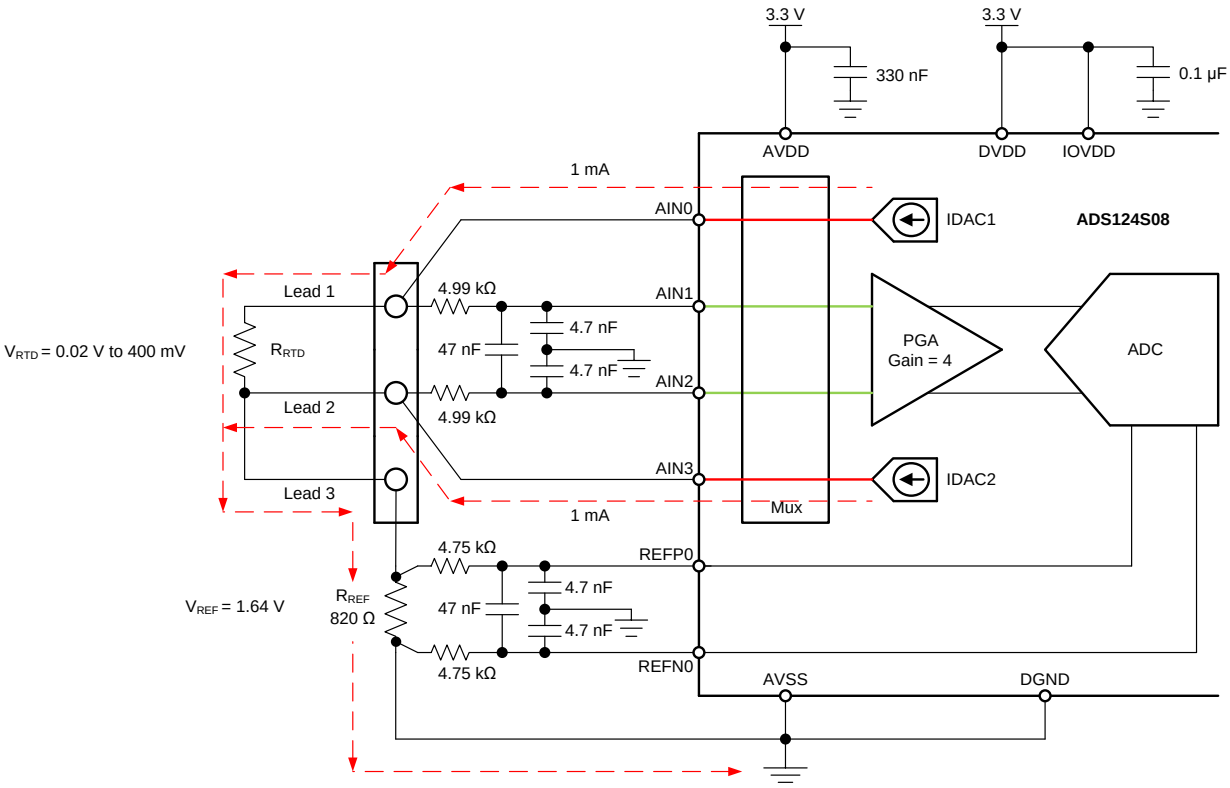
Three-wire PT100 RTD measurement circuit with low-side reference and two IDAC current sources

Joseph Wu

Power Supplies		
AVDD	**AVSS**	**DVDD, IOVDD**
3.3V	0V	3.3V

Design Description

This cookbook design describes a temperature measurement for a three-wire RTD using the ADS124S08. This design uses two matched IDAC excitation currents for lead-resistance cancellation. This topology creates a ratiometric measurement for a PT100 type RTD with a temperature measurement range from –200°C to 850°C. Included in this design are ADC register settings and pseudo code is provided to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab instrumentation*, and *factory automation*. For more information about making precision ADC measurements with a variety of RTD wiring configurations, see *A Basic Guide to RTD Measurements*.



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. AVDD must be decoupled with at least a 330-nF capacitor to AVSS. DVDD and IOVDD (when not connected to DVDD) must be decoupled with at least a 0.1-µF capacitor to DGND. See the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet for details on power supply recommendations.
2. Do not route the excitation currents through input filter resistors, using the same pin as an ADC input and as the output for an IDAC current source. Excitation currents reacting with series resistance adds error to the measurement.
3. A 1-µF capacitor is required between REFOUT and REFCOM to enable the internal reference for the IDAC current.
4. Use a precision reference resistor with high accuracy and low drift. Because the measurement is ratiometric, accuracy is dependent on the error of this reference resistor. A 0.01% resistor contributes a gain error similar to that as the ADC.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. An example design and analysis of these filters is found in *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.
7. This design shows connections to four input pins of the ADC multiplexer. Remaining analog inputs may be used for RTD, *thermocouple*, or other measurements.
8. Because of lead-resistance cancellation, the three-wire measurement offers more accuracy than comparable *two-wire RTD measurements*. For measurements with other RTD wiring configurations, see *A Basic Guide to RTD Measurements*.

Component Selection

1. Identify the range of operation for the RTD.

   As an example, a PT100 RTD has a range of approximately 20Ω to 400Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full scale range of the measurement.
2. Use two matched IDAC current sources to cancel the lead-resistance error.

   Two matched IDAC current sources are used for lead-resistance cancellation. Assuming the resistances of lead 1 and lead 2 are the same, and the currents of IDAC1 and IDAC2 are the same, then the lead-resistance error may be cancelled. Cancellation can be shown through the measured voltages at AIN1 and AIN2.

   IDAC1 drives current into the RTD through lead 1. IDAC2 drives a matched current into lead 2. The voltage at AIN1 is calculated with the following equation.

   $$V_{AIN1} = I_{IDAC1} \bullet (R_{LEAD1} + R_{RTD}) + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{REF})$$

   At the same time, voltage at AIN2 is also calculated.

   $$V_{AIN2} = I_{IDAC2} \bullet R_{LEAD2} + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{REF})$$

   The measurement of the ADC is the difference between AIN1 and AIN2, which is the subtraction of the first two equations to get the following.

   $$V_{AIN1} - V_{AIN2} = [I_{IDAC1} \bullet (R_{LEAD1} + R_{RTD}) + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{REF})] - [I_{IDAC2} \bullet R_{LEAD2} + (I_{IDAC1} + I_{IDAC2}) \bullet (R_{LEAD3} + R_{REF})]$$

   The R_{LEAD3} and R_{REF} terms drop out.

   $$V_{AIN1} - V_{AIN2} = I_{IDAC1} \bullet (R_{LEAD1} + R_{RTD}) - I_{IDAC2} \bullet R_{LEAD2}$$

   So if R_{LEAD1} and R_{LEAD2} are equal and I_{IDAC1} and I_{IDAC2} are equal (to become I_{IDAC}), then the lead resistance errors cancel.

   $$V_{AIN1} - V_{AIN2} = I_{IDAC} \bullet R_{RTD}$$

3. Determine values for the IDAC excitation currents and reference resistor.

   The excitation current source in this design is selected to be 1mA. This maximizes the value of the RTD voltage while keeping the self-heating of the RTD low. The typical range of RTD self-heating coefficients is 2.5mW/°C for small, thin-film elements and 65mW/°C for larger, wire-wound elements. With 1-mA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4mW and keeps the measurement errors from self-heating to less than 0.01˚C.

   After selecting the IDAC current magnitude, set R_{REF} = 820Ω. Using two matched 1-mA excitation currents sets the reference at 1.64V and the maximum RTD voltage is 400mV. The reference voltage acts as a level shift to place the input measurement to near mid-supply, putting the measurement in the PGA input operating range. With these values, the PGA gain can be set to 4 so that the maximum RTD voltage is near the positive full scale range without exceeding it.

   The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

   Using the maximum RTD resistance, the ADC input voltages are calculated in the following equations. The small lead resistances can be ignored for this calculation.

   $V_{AIN1} = (I_{IDAC1} \bullet R_{RTD}) + [(I_{IDAC1} + I_{IDAC2}) \bullet R_{REF}] = (1mA \bullet 400\Omega) + (2mA \bullet 820\Omega) = 2.04V$

   $V_{AIN2} = (I_{IDAC1} + I_{IDAC2}) \bullet R_{REF} = 2mA \bullet 820\Omega = 1.64V$

   $V_{INMAX} = 1mA \bullet 400\Omega = 400mV$

4. Verify that the design is within the range of operation of the ADC.

   First, verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given that the gain is 4 and that AVDD is 3.3V and AVSS is 0V. As shown in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the absolute input voltage must satisfy the following:

   $AVSS + 0.15V + [|V_{INMAX}| \bullet (Gain - 1) / 2] < V_{AIN1}, V_{AIN2} < AVDD - 0.15V - [|V_{INMAX}| (Gain - 1) / 2]$

   $0V + 0.15V + [|V_{INMAX}| \bullet (Gain - 1) / 2] < V_{AIN1}, V_{AIN2} < 3.3V - 0.15V - [|V_{INMAX}| (Gain - 1) / 2]$

   $0.75V < V_{AIN1}, V_{AIN2} < 2.55V$

   Because the maximum and minimum input voltages seen at AIN1 and AIN2 (2.04V and 1.64V) are between 0.75V and 2.55V, the inputs are in the PGA operating range.

   Second, verify that the voltage seen at the IDAC output is within the current source compliance voltage. The IDAC1 pin is AIN0 which has the same voltage as AIN1. At the maximum voltage, V_{AIN0} is 2.04V. As shown in the Electrical Characteristics table in the ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference data sheet, the output voltage of the IDAC pin must be between AVSS and AVDD − 0.6V for an IDAC current of 1mA. In this example, with AVDD = 3.3V, the IDAC output must be:

   $AVSS < V_{AIN0} = V_{AIN1} < AVDD - 0.6V$

   $0V < V_{AIN0} < 2.7V$

   With the previous result, the output compliance of the IDAC1 is satisfied. Because the IDAC2 pin is always at a lower voltage than the IDAC1 voltage, both current sources are in the compliance range.

5. Select values for the differential and common-mode input filtering for the ADC inputs and reference inputs.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering. While series filter resistors offer some amount of input protection, keep the input resistors lower than 10kΩ, to allow for proper input sampling for the ADC.

   With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors be reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

In this design, the data rate is chosen to be 20SPS using the low-latency filter of the ADS124S08. This filtering provides a low noise measurement with single-cycle settling and the ability to reject 50-Hz and 60-Hz line noise. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations.

$f_{IN\_DIFF} = 1 / [2 \cdot \pi \cdot C_{IN\_DIFF} (R_{RTD} + 2 \cdot R_{IN})]$

$f_{IN\_CM} = 1 / [2 \cdot \pi \cdot C_{IN\_CM} (R_{RTD} + R_{IN} + R_{REF})]$

For the ADC input filtering, $R_{IN} = 4.99k\Omega$, $C_{IN\_DIFF} = 47nF$, and $C_{IN\_CM} = 4.7nF$. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5.6kHz.

Similarly, the bandwidth for the reference input filtering is approximated in the following equations.

$f_{REF\_DIFF} = 1 / [2 \cdot \pi \cdot C_{REF\_DIFF} \cdot (R_{REF} + 2 \cdot R_{IN\_REF})]$

$f_{REF\_CM} = 1 / [2 \cdot \pi \cdot C_{REF\_CM} \cdot (R_{REF} + R_{IN\_REF})]$

For the reference input filtering, $R_{IN\_REF} = 4.75k\Omega$, $C_{REF\_DIFF} = 47nF$, and $C_{REF\_CM} = 4.7nF$. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 6.1kHz. Matching the ADC input and reference input filtering may not be possible. However, keeping the bandwidths close may reduce noise in the measurement.

For an in-depth analysis of component selection for input filtering, see *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*.

6. If IDAC current mismatch error is significant, use two measurements to chop the error (optional).

   One of the original assumptions in the lead-resistance cancellation is that IDAC1 and IDAC2 match. If the two IDAC currents do not match, the mismatch causes an error that appears as gain error. The voltage across the RTD comes from the current of IDAC1, while the voltage across the reference resistor comes from the current of IDAC1 + IDAC2. For the ADS124S08, the typical IDAC current mismatch for a 1-mA IDAC current is 0.07%. This mismatch error leads to a gain error of 0.35% in the measurement. To remove this current mismatch error, the IDAC excitation currents may be chopped. This involves taking two measurements with the IDAC currents swapped.

   For chopping, first take a measurement with IDAC1 set to AIN0 and IDAC2 set to AIN3. Then set IDAC1 to AIN3 and IDAC2 to AIN0, swapping the current sources, and take a second measurement. In the first case, IDAC1 drives the RTD, in the second case IDAC2 drives the RTD. In both cases, the sum of IDAC1 and IDAC2 drive the reference resistor. By averaging the two chopped cases, the mismatch error is removed from the measurement. For a more detailed analysis of chopping see the IDAC Current Chopping section of the *A Basic Guide to RTD Measurements* application report.

Measurement Conversion

RTD measurements are typically ratiometric measurements. Using a ratiometric measurement, the ADC output code does not need to be converted to a voltage. This means that the output code gives a measurement only as a ratio of the value of the reference resistor and does not require a precise value for the excitation current. The only requirement is that the current through the RTD and reference resistor are the same.

Equations for the measurement conversion are shown for a 24-bit ADC (without IDAC current chopping):

$\text{Output Code} = 2^{23} \cdot \text{Gain} \cdot (V_{RTD} / V_{REF}) = 2^{23} \cdot \text{Gain} \cdot (I_{IDAC1} \cdot R_{RTD}) / (I_{IDAC1} \cdot R_{REF}) = 2^{23} \cdot \text{Gain} \cdot (R_{RTD} / R_{REF})$

$R_{RTD} = R_{REF} \cdot [\text{Output Code} / (\text{Gain} \cdot 2^{23})]$

The ADC converts the measurement to the RTD equivalent resistance. Because of non-linearity in the RTD response, the conversion of the resistance to temperature requires an calculation from equation or lookup table. For more information about the conversion of RTD resistance to temperature, see *A Basic Guide to RTD Measurements*.

Register Settings

Configuration Register Settings for a Three-Wire PT100 RTD Measurement with Low-Side Reference and Two IDAC Current Sources Using the ADS124S08

Register Address	Register Name	Setting	Description
02h	INPMUX	12h	Select AIN_P = AIN1 and AIN_N = AIN2
03h	PGA	0Ah	PGA enabled, Gain = 4
04h	DATARATE	14h	Continuous conversion mode, low-latency filter, 20-SPS data rate
05h	REF	02h	Positive and negative reference buffers enabled, REFP0 and REFN0 reference inputs selected, internal reference always on
06h	IDACMAG	07h	IDAC magnitude set to 1mA
07h	IDACMUX	30h	IDAC1 set to AIN0, IDAC2 set to AIN3
08h	VBIAS	00h	VBIAS not used for any input
09h	SYS	10h	Normal mode of operation
07h (1)	IDACMUX	03h	IDAC1 set to AIN3, IDAC2 set to AIN0

(1) This second IDACMUX setting and conversion is used for chopping IDAC excitation current sources (optional).

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS124S0x in continuous conversion mode. The dedicated $\overline{\text{DRDY}}$ pin indicates availability of new conversion data. Pseudo code is shown without the use of the STATUS byte and CRC data verification. ADS124S08 *firmware example code* is available from the ADS124S08 product folder.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
Set CS low;
    Send 06;    // RESET command to make sure the device is properly reset after power-up
Set CS high;
Set CS low;    // Configure the device
    Send 42    // WREG starting at 02h address
    05    // Write to 6 registers
    12    // Select AINP = AIN1 and AINN = AIN2
    0A    // PGA enabled, Gain = 8
    14    // Continuous conversion mode, low-latency filter, 20-SPS data rate
    02    // Positive and negative reference buffers enabled,
          // REFP1 and REFN1 reference selected, internal reference always on
    07    // IDAC magnitude set to 1mA
    30;    // IDAC1 set to AIN0, IDAC2 set to AIN3
Set CS high;
Set CS low;     // For verification, read back configuration registers
    Send 22    // RREG starting at 02h address
    05    // Read from 6 registers
    00 00 00 00 00 00;    // Send 6 NOPs for the read
Set CS high;
Set CS low;
    Send 08;    // Send START command to start converting in continuous conversion mode;
Set CS high;
Loop
    {
    Set CS low;    // Configure the device for first chopped measurement
        Send 47    // WREG starting at 07h address
        00    // Write to 1 register
        30;    // IDAC1 set to AIN0, IDAC2 set to AIN3
    Set CS high;
    Wait for DRDY to transition low;
    Set CS low;
        Send 12    // Send RDATA command
        00 00 00;    // Send 3 NOPs (24 SCLKs) to clock out data, Record Measurement 1
    Set CS high;
    Set CS low;    // Configure the device for chopped current sources (optional)
        Send 47    // WREG starting at 07h address
        00    // Write to 1 register
        03;    // IDAC1 set to AIN3, IDAC2 set to AIN0
    Set CS high;
    Wait for DRDY to transition low;
    Set CS low;
        Send 12    // Send RDATA command
        00 00 00;    // Send 3 NOPs (24 SCLKs) to clock out data, Record Measurement 2
    Set CS high;
    Average Measurement 1 and Measurement 2;
    }
Set CS low;
    Send 0A;    //STOP command stops conversions and puts the device in standby mode;
Set CS to high;
```

RTD Circuit Comparison Table

RTD Circuit Topology	Advantages	Disadvantages
Two-wire RTD, low-side reference	Least expensive	Least accurate, no lead-resistance cancellation
Three-wire RTD, low-side reference, two IDAC current sources	Allows for lead-resistance cancellation	Sensitive to IDAC current mismatch, mismatch can be removed by swapping IDAC currents and averaging two measurements
Three-wire RTD, low-side reference, one IDAC current source	Allows for lead-resistance cancellation	Requires two measurements, first for RTD measurement, second for lead-resistance cancellation
Three-wire RTD, high-side reference, two IDAC current sources	Allows for lead-resistance cancellation, less sensitive to IDAC mismatch than using low side reference	Requires extra resistor for biasing, added voltage may not be compatible with low supply operation
Four-wire RTD, low-side reference	Most accurate, no lead-resistance error	Most expensive

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS124S08	24-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS124S08	Link to similar devices
ADS114S08 (1)	16-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS114S08	Link to similar devices

(1) The ADS114S08 is a 16-bit version of the ADS124S08 and may be used in similar applications.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, ADS124S08 Evaluation Module
- Texas Instruments,
- *ADS1x4S08 Evaluation Module User's Guide*
- Texas Instruments, ADS1x4S08 Firmware Example Code
- Texas Instruments, *A Basic Guide to RTD Measurements*
- Texas Instruments, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices*

For direct support from TI Engineers use the E2E community:

e2e.ti.com

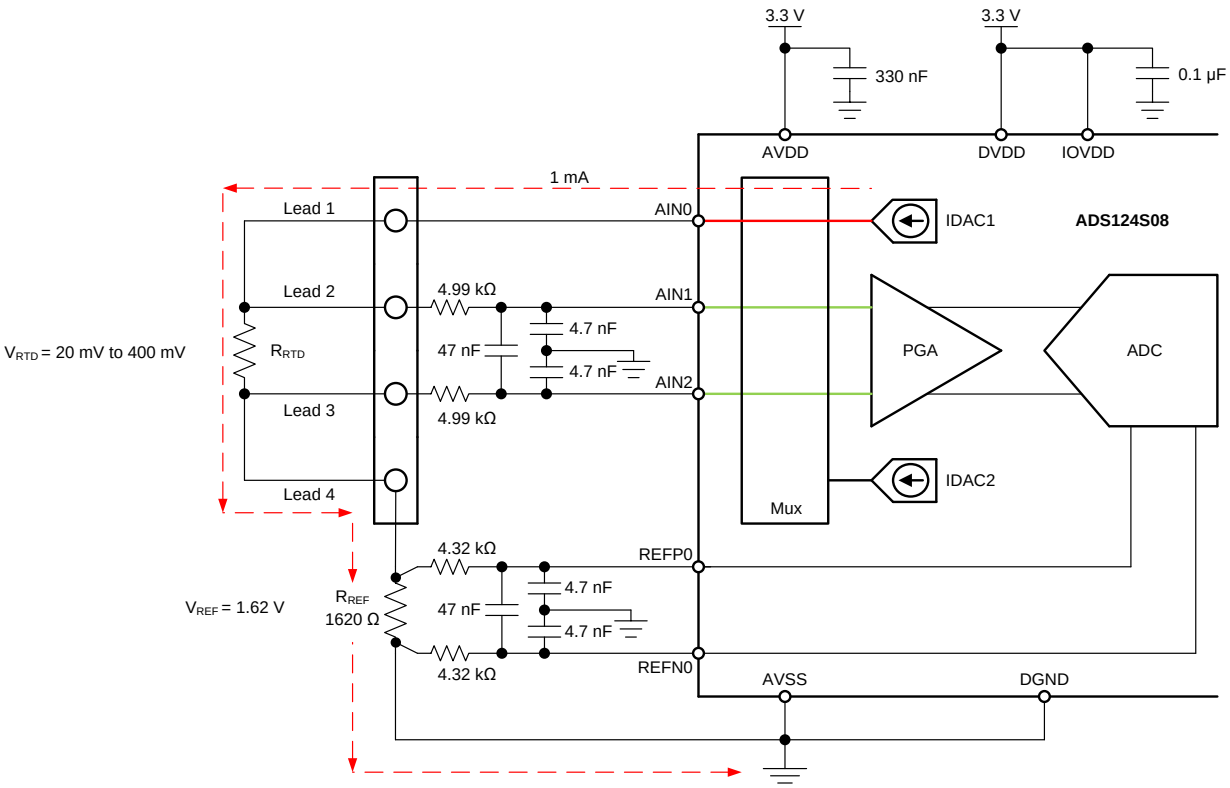
Four-wire PT100 RTD measurement circuit with low-side reference

Joseph Wu

Power Supplies		
AVDD	**AVSS, DGND**	**DVDD, IOVDD**
3.3V	0V	3.3V

Design Description

This cookbook design describes a temperature measurement for a four-wire RTD using the ADS124S08. This design uses a ratiometric measurement for a PT100 type RTD with a temperature measurement range from –200°C to 850°C. The four-wire RTD measurement is the most accurate of the RTD wiring configurations because the lead-resistance is not a factor in the measurement. Included in this design are ADC configuration register settings and pseudo code to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab instrumentation*, and *factory automation*. For more information about making precision ADC measurements with a variety of RTD wiring configurations, see *A Basic Guide to RTD Measurements*.



Design Notes

1. Use supply decoupling capacitors for both the analog and digital supplies. AVDD must be decoupled with at least a 330-nF capacitor to AVSS. DVDD and IOVDD (when not connected to DVDD) must be decoupled with at least a 0.1-µF capacitor to DGND. See the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet for details on power supply recommendations.
2. Do not route the excitation currents through input filter resistors, using the same pin as an ADC input and as the output for an IDAC current source. Excitation currents reacting with series resistance adds error to the measurement.
3. A 1-µF capacitor is required between REFOUT and REFCOM to enable the internal reference for the IDAC current.
4. Use a precision reference resistor with high accuracy and low drift. Because the measurement is ratiometric, accuracy is dependent on the error of this reference resistor. A 0.01% resistor contributes a gain error similar to that as the ADC.
5. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.
6. Input filtering for the ADC inputs and the reference inputs are selected using standard capacitor values and 1% resistor values. An example design and analysis of these filters is found in the *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices* application report.
7. This design shows connections to three input pins of the ADC multiplexer. Remaining analog inputs may be used for RTD, thermocouple, or other measurements.
8. The design for the four-wire RTD measurement is identical to the two-wire RTD measurement but requires four terminal connections and eliminates the lead-resistance error. For measurements with different RTD wiring configurations, see *A Basic Guide to RTD Measurements*.

Component Selection

1. Identify the range of operation for the RTD.

   As an example, a PT100 RTD has a range of approximately 20Ω to 400Ω if the temperature measurement range is from −200°C to 850°C. The reference resistor must be larger than the maximum RTD value. The reference resistance and PGA gain determines the positive full scale range of the measurement.
2. Determine values for the IDAC excitation current and reference resistor.

   In this design, the IDAC current source drives the RTD through lead 1. The current exits the RTD through lead 4 and is shunted by R_{REF} to create a ratiometric measurement. The measurement is made between lead 2 and lead 3 by the ADC, making a Kelvin connection to remove the lead resistance error. With this four-terminal sensing, the 4-wire RTD measurement is the most accurate of the RTD wiring configurations.

   The excitation current source in this design is selected to be 1mA. This maximizes the value of the RTD voltage while keeping the self-heating of the RTD low. The typical range of RTD self-heating coefficients is 2.5mW/°C for small, thin-film elements and 65mW/°C for larger, wire-wound elements. With 1-mA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4mW and keeps the measurement errors from self-heating to less than 0.01˚C.

   After selecting the IDAC current magnitude, set R_{REF} = 1620Ω. This sets the reference at 1.62V and the maximum RTD voltage is 400mV. The reference voltage acts as a level shift to place the input measurement to near mid-supply, putting the measurement in the PGA input operating range. With these values, the PGA gain can be set to 4 so that the maximum RTD voltage is near the positive full scale range without exceeding it.

   The reference resistor, R_{REF} must be a precision resistor with high accuracy and low drift. Any error in R_{REF} reflects the same error in the RTD measurement. The REFP0 and REFN0 pins are shown connecting to the R_{REF} resistor as a Kelvin connection to get the best measurement of the reference voltage. This eliminates any series resistance as an error from the reference resistance measurement.

Using the maximum RTD resistance, the ADC input voltages are calculated in the following:

$V_{AIN1} = I_{IDAC1} \bullet (R_{RTD} + R_{REF}) = 1mA \bullet (400\Omega + 1620\Omega) = 2.02V$

$V_{AIN2} = I_{IDAC1} \bullet R_{REF} = 1mA \bullet 1620\Omega = 1.62V$

$V_{INMAX} = 1mA \bullet 400\Omega = 400mV$

3. Verify that the design is within the range of operation of the ADC.

   First, verify that V_{AIN1} and V_{AIN2} are within the input range of the PGA given that the gain is 4 and that AVDD is 3.3V and AVSS is 0V. As the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet shows, the absolute input voltage must satisfy the following:

   $AVSS + 0.15V + [|V_{INMAX}| \bullet (Gain - 1) / 2] < V_{AIN1}, V_{AIN2} < AVDD - 0.15V - [|V_{INMAX}| (Gain - 1) / 2]$

   $0V + 0.15V + [|V_{INMAX}| \bullet (Gain - 1) / 2] < V_{AIN1}, V_{AIN2} < 3.3V - 0.15V - [|V_{INMAX}| (Gain - 1) / 2]$

   $0.75 < V_{AIN1}, V_{AIN2} < 2.55V$

   Because the maximum and minimum input voltages seen at AIN1 and AIN2 (2.02 V and 1.62 V) are between 0.75V and 2.55V, the inputs are in the PGA operating range.

   Second, verify that the voltage at the IDAC output pin is within the current source compliance voltage. The IDAC pin is AIN0, which have the same voltage as AIN1. At the maximum voltage, V_{AIN0} is 2.02V. As shown in the Electrical Characteristics table in the *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference* data sheet, the output voltage of the IDAC must be between AVSS and AVDD − 0.6V for an IDAC current of 1mA. In this example, with AVDD = 3.3V, the IDAC output must be:

   $AVSS < V_{AIN0} = V_{AIN1} < AVDD - 0.6V$

   $0V < V_{AIN0} < 2.7V$

   With the above result, the output compliance of the IDAC is satisfied.

4. Select values for the differential and common-mode filtering for the ADC inputs and reference inputs.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering. While series filter resistors offer some amount of input protection, keep the input resistors lower than 10kΩ, to allow for proper input sampling for the ADC.

   With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors be reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

   In this design, the data rate is chosen to be 20SPS using the low-latency filter of the ADS124S08. This filtering provides a low noise measurement with single-cycle settling and the ability to reject 50-Hz and 60-Hz line noise. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations.

   $f_{IN\_DIFF} = 1 / [2 \bullet \pi \bullet C_{IN\_DIFF} (R_{RTD} + 2 \bullet R_{IN})]$

   $f_{IN\_CM} = 1 / [2 \bullet \pi \bullet C_{IN\_CM} (R_{RTD} + R_{IN} + R_{REF})]$

   For the ADC input filtering, R_{IN} = 4.99kΩ, C_{IN_DIFF} = 47nF, and C_{IN_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5kHz.

   Similarly, the bandwidth for the reference input filtering is approximated in the following equations.

   $f_{REF\_DIFF} = 1 / [2 \bullet \pi \bullet C_{REF\_DIFF} \bullet (R_{REF} + 2 \bullet R_{IN\_REF})]$

   $f_{REF\_CM} = 1 / [2 \bullet \pi \bullet C_{REF\_CM} \bullet (R_{REF} + R_{IN\_REF})]$

   For the reference input filtering, R_{IN_REF} = 4.32kΩ, C_{REF_DIFF} = 47nF, and C_{REF_CM} = 4.7nF. This sets the differential filter bandwidth to 330Hz and the common-mode filter bandwidth to 5.7kHz. Matching the ADC input and reference input filtering may not be possible. However, keeping the bandwidths close may reduce the noise in the measurement.

   For an in-depth analysis of component selection for input filtering, see the *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices* application report.

Measurement Conversion

RTD measurements are typically ratiometric measurements. Using a ratiometric measurement, the ADC output code does not need to be converted to a voltage. This means that the output code gives a measurement only as a ratio of the value of the reference resistor and does not require a precise value for the excitation current. The only requirement is that the current through the RTD and reference resistor are the same.

Equations for the measurement conversion are shown for a 24-bit ADC:

$$\text{Output Code} = 2^{23} \bullet \text{Gain} \bullet (V_{RTD} / V_{REF}) = 2^{23} \bullet \text{Gain} \bullet (I_{IDAC1} \bullet R_{RTD}) / (I_{IDAC1} \bullet R_{REF}) = 2^{23} \bullet \text{Gain} \bullet (R_{RTD} / R_{REF})$$

$$R_{RTD} = R_{REF} \bullet [\text{Output Code} / (\text{Gain} \bullet 2^{23})]$$

The ADC converts the measurement to the RTD equivalent resistance. Because of non-linearity in the RTD response, the conversion of the resistance to temperature requires an calculation from equation or lookup table. For more information about the conversion of RTD resistance to temperature, see *A Basic Guide to RTD Measurements*.

Register Settings

Configuration Register Settings for a Four-Wire PT100 RTD Measurement Circuit with Low-Side Reference Using the ADS124S08

Register Address	Register Name	Setting	Description
02h	INPMUX	12h	Select AIN_P = AIN1 and AIN_N = AIN2
03h	PGA	0Ah	PGA enabled, Gain = 4
04h	DATARATE	14h	Continuous conversion mode, low-latency filter, 20-SPS data rate
05h	REF	02h	Positive and negative reference buffers enabled, REFP0 and REFN0 reference inputs selected, internal reference always on
06h	IDACMAG	07h	IDAC magnitude set to 1mA
07h	IDACMUX	F0h	IDAC1 set to AIN0, IDAC2 disabled
08h	VBIAS	00h	VBIAS not used for any input
09h	SYS	10h	Normal mode of operation

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS124S0x in continuous conversion mode. The dedicated $\overline{\text{DRDY}}$ pin indicates availability of new conversion data. Pseudo code is shown without the use of the STATUS byte and CRC data verification. ADS124S08 firmware example code is available from the ADS124S08 product folder.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Configure microcontroller GPIO for /DRDY as a falling edge triggered interrupt input
Set CS low;
    Send 06;    // RESET command to make sure the device is properly reset after power-up
Set CS high;
Set CS low;    // Configure the device
    Send 42    // WREG starting at 02h address
    05    // Write to 6 registers
    12    // Select AINP = AIN1 and AINN = AIN2
    0A    // PGA enabled, Gain = 4
    14    // Continuous conversion mode, low-latency filter, 20-SPS data rate
    02    // Positive and negative reference buffers enabled,
          // REFP0 and REFN0 reference selected, internal reference always on
    07    // IDAC magnitude set to 1 mA
    F0;    // IDAC1 set to AIN0, IDAC2 disabled
Set CS high;
Set CS low;     // For verification, read back configuration registers
    Send 22    // RREG starting at 02h address
    05    // Read from 6 registers
    00 00 00 00 00 00;    // Send 6 NOPs for the read
Set CS high;
Set CS low;
    Send 08;    // Send START command to start converting in continuous conversion mode;
Set CS high;
Loop
    {
    Wait for DRDY to transition low;
    Set CS low;
        Send 12    // Send RDATA command
        00 00 00;    // Send 3 NOPs (24 SCLKs) to clock out data
    Set CS high;
    }
Set CS low;
    Send 0A;    //STOP command stops conversions and puts the device in standby mode;
Set CS to high;
```

RTD Circuit Comparison Table

RTD Circuit Topology	Advantages	Disadvantages
Two-wire RTD, low-side reference	Least expensive	Least accurate, no lead-resistance cancellation
Three-wire RTD, low-side reference, two IDAC current sources	Allows for lead-resistance cancellation	Sensitive to IDAC current mismatch, mismatch can be removed by swapping IDAC currents and averaging two measurements
Three-wire RTD, low-side reference, one IDAC current source	Allows for lead-resistance cancellation	Requires two measurements, first for RTD measurement, second for lead-resistance cancellation
Three-wire RTD, high-side reference, two IDAC current sources	Allows for lead-resistance cancellation, less sensitive to IDAC mismatch than using low side reference	Requires extra resistor for biasing, added voltage may not be compatible with low supply operation
Four-wire RTD, low-side reference	Most accurate, no lead-resistance error	Most expensive

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS124S08	24-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS124S08	Link to similar devices
ADS114S08[(1)]	16-Bit, 4kSPS, 12-Ch Delta-Sigma ADC With PGA and Voltage Reference for Precision Sensor Measurement	www.ti.com/product/ADS114S08	Link to similar devices

(1) The ADS114S08 is a 16-bit version of the ADS124S08 and may be used in similar applications.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, ADS124S08 Evaluation Module
- Texas Instruments, *ADS1x4S08 Evaluation Module User's Guide*
- Texas Instruments, ADS1x4S08 Firmware Example Code
- Texas Instruments, *A Basic Guide to RTD Measurements Application Report*
- Texas Instruments, *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices Application Report*

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e2e.ti.com

Two-channel, K-type thermocouple measurement circuit with internal temperature sensor CJC

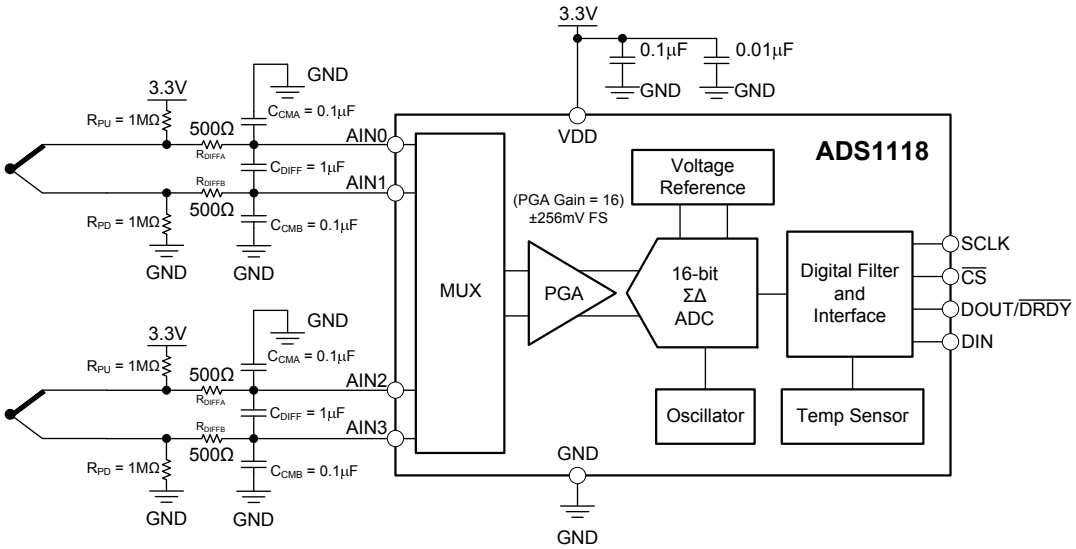
Joseph Wu

Input Measurement	ADC Input Voltage	ADC Digital Output
T = –270°C	AINP – AINN = –6.5mV	$FCC0_H$ or -832_{10}
T = 1370°C	AINP – AINN = 55mV	$1B80_H$ or 7040_{10}

Power Supplies	
VDD	**GND**
3.3V	0V

Design Description

This cookbook design describes a temperature measurement circuit with two thermocouples using the ADS1118. Thermocouple voltage measurements are made with the ADS1118 internal voltage reference, while cold-junction compensation (CJC) measurements are made with the onboard temperature sensor. Two channels of the ADC are used for two K-type thermocouples with a temperature measurement range from –270°C to 1370°C. Included in this design are ADC register settings to configure the device and pseudo code is provided to configure and read from the device. This circuit can be used in applications such as *analog input modules* for PLCs, *lab instrumentation*, and *factory automation*. For more information about using precision ADCs with thermocouples, see *A Basic Guide to Thermocouple Measurements*.



Design Notes

1. Use supply decoupling capacitors for the supply. VDD must be decoupled with at least a 0.1-µF capacitor to GND. See *ADS1118 Ultrasmall, Low-Power, SPI™-Compatible, 16-Bit Analog-to-Digital Converter with Internal Reference and Temperature Sensor* for details on power supply recommendations.
2. When possible, use C0G (NPO) ceramic capacitors for input filtering. The dielectric used in these capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes. Because of size, this may not always be practical and X7R capacitors are the next best alternative.
3. Cold-junction compensation is required for accurate measurement of the thermocouple temperature.
4. The K-type thermocouple is chosen for its large input range and thermocouple voltage. Other thermocouples have different sensitivities and error tolerances. For measurements with other thermocouples and a guide to use them, see *A Basic Guide to Thermocouple Measurements*.
5. Conversion tables and polynomial equations used to determine thermocouple temperature from the thermoelectric voltage is found at the NIST website at http://srdata.nist.gov/its90/menu/menu.html. Additionally, some thermocouple conversions may be determined from the Analog Engineer's Calculator.

Component Selection

1. Identify the range of operation for the thermocouple.

   The K-type thermocouple has a range of approximately −6.5mV to +55mV if the temperature measurement range is from −270°C to 1370°C. This range is used to maximize the resolution of the measurement, considering the full-scale range of the ADC.

2. Determine gain and input range of the ADC.

   In the ADS1118, the programmable gain amplifier (PGA) is implemented through scaled capacitive sampling, not as a true amplifier. With this PGA, the input range extends to the full supply range, but has less amplification and lower input impedance. In this device, the maximum amplification gives a full scale range of ±0.256V. This is much larger than the range of −6.5mV to +55mV for the thermocouple. While it is not possible to over-range the PGA, the measurement uses a limited portion of the full scale range. Comparing the thermocouple range to the full-range, the percent of the usable ADC range can be calculated:

   % of usable ADC range = [55mV–(–6.5mV)]/[0.256mV–(–0.256mV)] • 100% = 12.0%

   Number of ADC codes in measurement range = 0.12 • 2^{16} = 7864

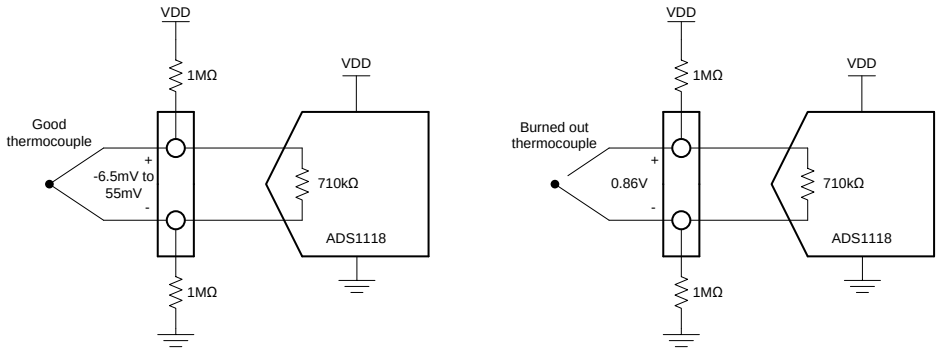
   With a range of −270°C to 1370°C for the thermocouple, 7864 codes are used to represent a temperature range of 1640°C. This equates to approximately 0.21°C per ADC code which should be enough for most thermocouple applications.

   In other precision ADCs, the PGA is implemented similar to an instrumentation amplifier. If using a different ADC, calculate the maximum gain allowed without over-ranging the PGA based on the maximum thermocouple output voltage. Then ensure that the thermocouple biasing is near mid-supply so that the input signal is in the common-mode input range of the PGA.

3. Set up the resistor biasing to establish the input DC level and burnout detection.

   Equal biasing resistors are tied from either end of the thermocouple and to GND and VDD. In normal operation, the resistors set the DC biasing point of the thermocouple to near mid-supply. If the thermocouple burns out and becomes an open circuit, the resistors pull apart the thermocouple leads to either supply. These resistors are set high (often 500kΩ to 10MΩ) to reduce the bias current going through the thermocouple. Resistor bias current reacting with the thermocouple lead resistance cause measurement error. However, the resistors must also be low enough to provide sufficient bias current to overcome any input current from the resistor.

   In this design, biasing resistors are chosen to be 1MΩ. This value sets the resistor biasing current to a low 1.65µA. However, in the case of a burned out thermocouple, 1MΩ provides enough current to separate the ADC inputs against the 710kΩ equivalent input impedance of the ADS1118.



In the case of the good thermocouple, the thermocouple voltage has a range of –6.5mV to 55mV. The remaining 3.3V of the VDD supply is dropped equally between the biasing resistors. With 1-MΩ bias resistors, the thermocouple voltage has a DC operating point near mid-supply at 1.65V.

In the case of a burned out thermocouple, the open circuit creates a voltage divider with the two 1MΩ around the 710-kΩ equivalent input impedance. The ADC input voltage with a burned out thermocouple may be calculated as:

ADC input voltage = 3.3V • [710kΩ / (1MΩ + 710kΩ + 1MΩ)] = 0.85V

If the thermocouple burns out, the ADC input voltage is 0.86V, which is much larger that the positive full-scale reading of the ADC. The ADC reports a reading of 7FFFh to indicate a burnout condition.

4. Select values for the differential and common-mode filtering for the ADC inputs and reference inputs.

   If there is input filtering, the input current reacts with any series filter resistance to create an error. For the ADS1118, the input current is modeled as an equivalent differential input impedance. As previously mentioned, the equivalent differential input impedance is typically 710kΩ. For this reason, the input series resistance is kept low or the added voltage appears as a gain error.

   This design includes differential and common-mode input RC filtering. The bandwidth of the differential input filtering is set to be at least 10 × higher than the data rate of the ADC. The common-mode capacitors are selected to be 1/10 of the value the differential capacitor. Because of capacitor selection, the bandwidth of common-mode input filtering is approximately 20 × higher than the differential input filtering.

   With input filtering, differential signals are attenuated at a lower frequency than the common-mode signals, which are significantly rejected by the PGA of the device. Mismatches in common-mode capacitors cause an asymmetric noise attenuation, appearing as a differential input noise. With a lower bandwidth for differential signals, the effects from the mismatch of input common-mode capacitors are reduced. Input filtering for the ADC inputs and reference inputs are designed for the same bandwidth.

   In this design, the data rate is chosen to be 8SPS. For the ADC input filtering, the bandwidth frequency for the differential and common-mode filtering is approximated in the following equations:

   $f_{IN\_DIFF} = 1 / [2 • \pi • C_{DIFF} • (2 • R_{DIFF})]$

   $f_{IN\_CM} = 1 / (2 • \pi • C_{CM} • R_{DIFF})$

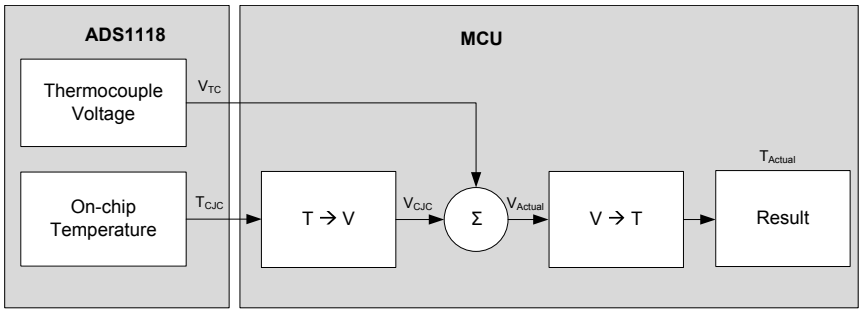
   For the ADC input filtering, R_{IN} = 500Ω, C_{IN_DIFF} = 1µF, and C_{IN_CM} = 0.1µF. This sets the differential filter bandwidth to 160Hz and the common-mode filter bandwidth to 3.2kHz.

5. Use cold-junction compensation to calculate the actual thermocouple voltage based on the cold-junction temperature.

   To get a precise measurement from a thermocouple, cold-junction compensation must be performed to get an accurate temperature measurement. An accurate measurement of the cold-junction where the thermocouple leads are tied is required. You cannot simply add the temperature of the cold-junction to the temperature computed from the thermocouple voltage. To accurately determine the thermocouple temperature, the proper method is to:

   1. Convert the cold-junction temperature (T_{CJ}) to a voltage (V_{CJ})
   2. Add the cold-junction voltage to the measured thermocouple voltage ($V_{CJ} + V_{TC}$)
   3. Convert the summed cold-junction voltage and thermocouple voltage to the thermocouple temperature (T_{TC})

The following flow diagram shows the conversion method to determine the actual temperature of the thermocouple based on the ADC measurements.



Conversion tables and polynomial equations used to determine thermocouple temperature from the thermoelectric voltage are found at the NIST website at http://srdata.nist.gov/its90/menu/menu.html.

Because the ADS1118 has an accurate internal temperature sensor, a measurement can be used. The internal temperature sensor has a typical accuracy of 0.2°C for a range of 0°C to 70°C. This accuracy is ideal for the cold-junction measurement. However, the device requires a good thermal contact to the connection for the thermocouple cold-junction. Any error in the cold-junction measurement yields an error in the resulting temperature measurement.

For more information about thermocouples and the cold-junction compensation measurement, see *A Basic Guide to Thermocouple Measurements*.

Measurement Conversion

Conversions for the thermocouple voltage are relatively straight forward based on the full-scale range setting of the ADC. In this design, the smallest full-scale range is used (±0.256V).

Measurement 1 (Thermocouple 1):

Output Code 1 = $[2^{15} \bullet (V_{AIN0} - V_{AIN1}) / (0.256V)]$

Thermocouple 1 Voltage = $V_{AIN0} - V_{AIN1}$ = $[(\text{Output Code 1}) \bullet 0.256V / 2^{15}]$

Measurement 2 (Thermocouple 2):

Output Code 2 = $[2^{15} \bullet (V_{AIN2} - V_{AIN3}) / (0.256V)]$

Thermocouple 2 Voltage = $V_{AIN2} - V_{AIN3}$ = $[(\text{Output Code 2}) \bullet 0.256V / 2^{15}]$

Conversions for the internal temperature sensor require some data manipulation. Temperature data from the ADC are represented as a 14-bit result that is left-justified within the 16-bit conversion result. Data are output starting with the most significant byte (MSB). When reading the two data bytes, the first 14 bits are used to indicate the temperature measurement result. One 14-bit LSB equals 0.03125°C and negative numbers are represented in binary twos complement format.

Measurement 3 (Internal Temperature Sensor):

Output Code 3 = [(Temperature) / (0.03125°C)]

Temperature = [(Output Code 3) • (0.03125°C)]

Output Code 3 is the first 14 bits of the two byte output data from the ADC. For more information about the ADS1118 and the internal temperature sensor see *ADS1118 Ultrasmall, Low-Power, SPI™-Compatible, 16-Bit Analog-to-Digital Converter with Internal Reference and Temperature Sensor*.

Register Settings

Measurement 1 (Thermocouple 1 Voltage): Config Register (8D0Bh)

Bit	Field	Setting	Description
15	SS	1	Start a single conversion
14:12	MUX[2:0]	000	AINP is AIN0 and AINN is AIN1 for thermocouple 1
11:9	PGA[2:0]	110	FSR is ±0.256V
8	MODE	1	Power-down and single-shot mode
7:5	DR[2:0]	000	8SPS
4	TS_MODE	0	ADC mode
3	PULL_UP_EN	1	Pullup resistor enabled on DOUT/$\overline{\text{DRDY}}$ pin
2:1	NOP[1:0]	01	Valid data, update the Config register
0	Reserved	1	Always write 1h

Measurement 2 (Thermocouple 2 Voltage): Config Register (BD0Bh)

Bit	Field	Setting	Description
15	SS	1	Start a single conversion
14:12	MUX[2:0]	011	AINP is AIN2 and AINN is AIN3 for thermocouple 2
11:9	PGA[2:0]	110	FSR is ±0.256V
8	MODE	1	Power-down and single-shot mode
7:5	DR[2:0]	000	8SPS
4	TS_MODE	0	ADC mode
3	PULL_UP_EN	1	Pullup resistor enabled on DOUT/$\overline{\text{DRDY}}$ pin
2:1	NOP[1:0]	01	Valid data, update the Config register
0	Reserved	1	Always write 1h

Measurement 3 (Internal Temperature Sensor): Config Register (8D1Bh)

Bit	Field	Setting	Description
15	SS	1	Start a single conversion
14:12	MUX[2:0]	011	AINP is AIN2 and AINN is AIN3 (ignored by TS_MODE)
11:9	PGA[2:0]	110	FSR is ±0.256V (ignored by TS_MODE)
8	MODE	1	Power-down and single-shot mode
7:5	DR[2:0]	000	8SPS
4	TS_MODE	1	Temperature sensor mode (bypasses MUX[2:0])
3	PULL_UP_EN	1	Pullup resistor enabled on DOUT/$\overline{\text{DRDY}}$ pin
2:1	NOP[1:0]	01	Valid data, update the Config register
0	Reserved	1	Always write 1h

Pseudo Code Example

The following shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC in order to take subsequent readings from the ADS1118 in single-shot conversion mode.

Data read back and device configuration are done with 32-bit transmission cycle with Config register read back. The ADS1118 is configured to measure the thermocouple voltages with a full-scale range of ±256mV and a data rate of 8SPS. The device cycles from reading the voltage of thermocouple 1, the voltage of thermocouple 2, and then the ADS1118 internal temperature sensor. After taking all three readings, cold-junction compensation is used to convert the thermocouple voltages to the thermocouple temperatures.

```
Configure microcontroller for SPI mode 1 (CPOL = 0, CPHA = 1)
Set CS low; // Start conversions
Send 8D0B8D0B;  //Start conversion for thermocouple 1
                // Use 32-bit data transmission cycle with Config register readback
                // The first iteration of the loop has no data readback
Set CS high;
Loop
{
    Wait 69ms // Wait for typical data period +10% for internal oscillator variation
    Set CS low;
        Send BD0BBD0B; // Read data for thermocouple 1, start conversion for thermocouple 2,
    Set CS high;
    Wait 69ms;
    Set CS low;
        Send 8D1B8D1B; // Read data for thermocouple 2, start conversion for temperature sensor,
    Set CS high;
    Wait 69ms;
    Set CS low;
        Send 8D0B8D0B // Read data temperature sensor, Start conversion for thermocouple 1
    Set CS high;
    // Cold-junction compensation to determine thermocouple temperature
    Convert thermocouple 1 ADC data to voltage;
    Convert thermocouple 2 ADC data to voltage;
    Convert temperature sensor data to temperature;
    Convert temperature sensor data to thermoelectric voltage; // By lookup table or calculation
    Add thermocouple 1 voltage to temperature thermoelectric voltage;
    Convert resulting voltage for thermocouple 1 to temperature; // By lookup table or calculation
    Add thermocouple 2 voltage to temperature thermoelectric voltage;
    Convert resulting voltage for thermocouple 2 to temperature; // By lookup table or calculation
}
```

Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS1118	Ultrasmall, low-power, SPI™-compatible, 16-bit analog-to-digital converter with internal reference and temperature sensor	http://www.ti.com/product/ADS1118	Link to similar devices (1)

(1) For cold-junction compensation, ensure that the device has a internal temperature sensor with specified limits. Alternately, an external temperature sensor may be used with an ADC channel for the cold-junction measurement.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Additional Resources

- Texas Instruments, ADS1118 Evaluation Module
- Texas Instruments, *ADS1118EVM User Guide and Software Tutorial*
- Texas Instruments, *A Basic Guide to Thermocouple Measurements*
- Texas Instruments, Analog Engineer's Calculator
- Texas Instruments, *Precision Thermocouple Measurement with the ADS1118*
- Texas Instruments, Simple Thermocouple Measurement Solution Reference Design, <1°C Accurate

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