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Circuit for driving a high-voltage SAR with an instrumentation amplifier

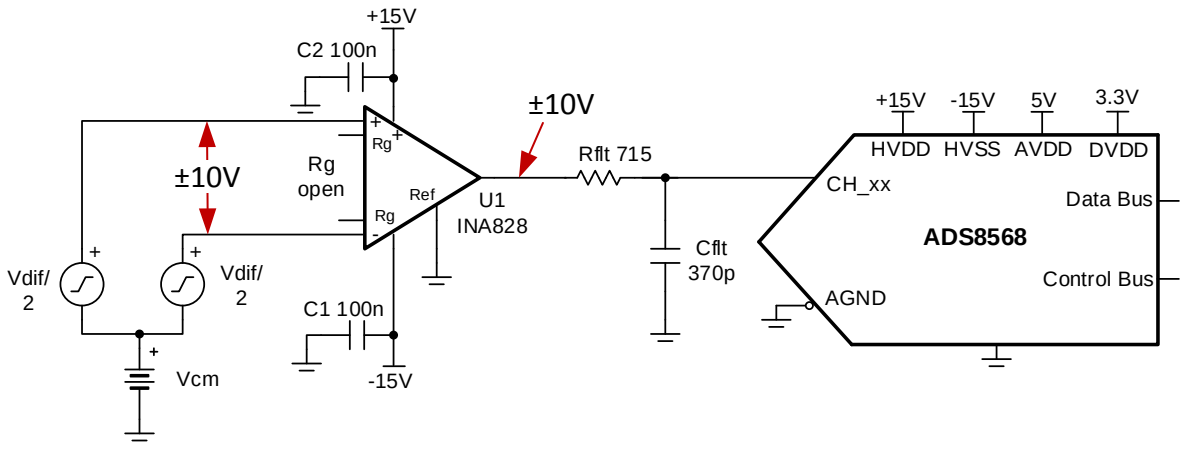
Dale Li

Input	ADC Input	Digital Output ADS7042
–10V	–10V	8000H
+10V	+10V	7FFFH

Power Supplies				
AVDD	**DVDD**	**V_{ref}**	**V_{cc}**	**V_{ee}**
5.0V	3.0V	5.0V	+15V	–15V

Design Description

Instrumentation amplifiers are optimized for low noise, low offset, low drift, high CMRR and high accuracy. The INA828 instrumentation amplifier preforms a differential to single-ended conversion for a ±10-V range. The INA828 has excellent DC performance (that is, offset, drift), as well as good bandwidth. The ADS8568 is ideally suited to work with the INA828 as the ADC can be configured for a ±10-V single-ended input. To achieve the best settling, limit the sampling rate to 200kSPS or lower. For higher sampling rates see *Driving High-Voltage SAR ADC with a Buffered Instrumentation Amplifier*. Also, this design example uses unity gain (G=1) to translate a ±10-V differential input signal to a ±10-V single-ended output. For smaller input signals or higher gains, see *Circuit for Driving an ADC with an Instrumentation Amplifier in High Gain*. This circuit implementation is applicable to *Industrial Transportation* and *Analog Input Modules* that require precision signal-processing and data-conversion.



Specifications

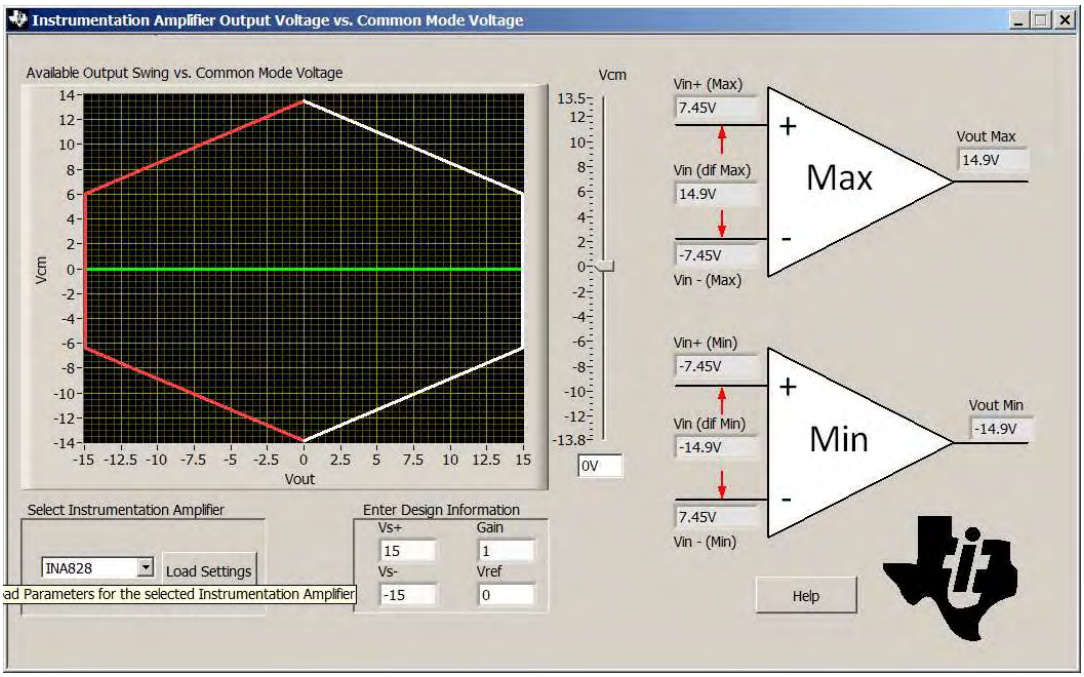
Specification	Goal	Calculated	Simulated
Transient Settling Error	< 1/2 LSB (±152µV)	NA	–105µV
Noise	< 20µV	103µV	86.6µV

Design Notes

1. The bandwidth of instrumentation amplifiers is typically not enough to drive SAR data converters at higher data rate. In this example, the sampling rate is reduced from 510kSPS to 200kSPS to achieve good settling. For full sampling rate see *Driving High-Voltage SAR ADC with a Buffered Instrumentation Amplifier*.
2. Check the common mode and output range of the instrumentation amplifier using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* software tool.
3. Use a COG type capacitor for C_{filt} to minimize distortion.
4. The *Precision Labs* video series covers methods for selecting the charge bucket circuit C_{flt} and R_{flt}. See the *Introduction to SAR ADC Front-End Component Selection* for details on this subject.

Component Selection

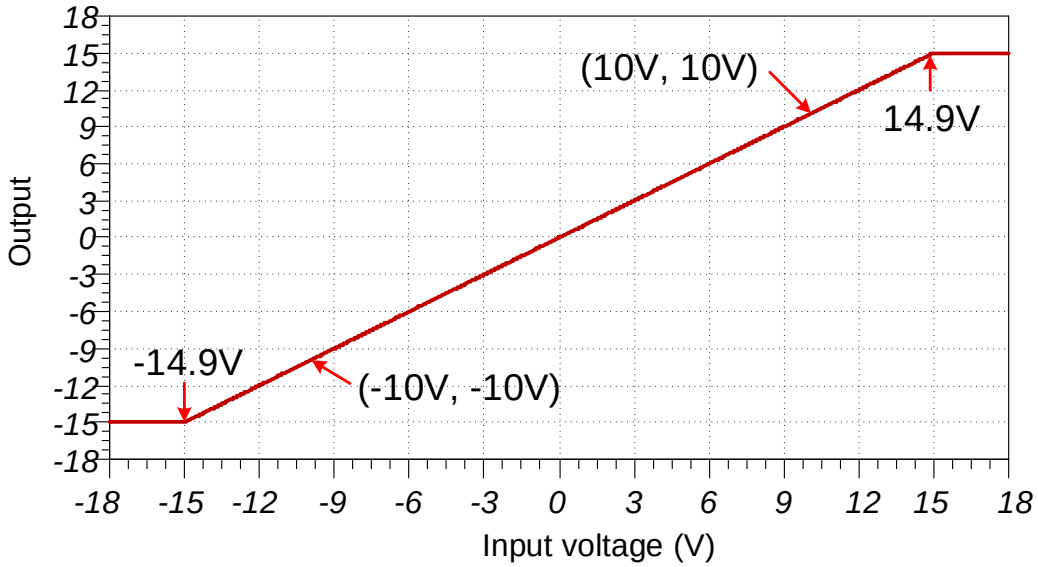
1. The ADS8568 can accept a ±10-V single-ended input signal. The INA828 is used to translate a ±10-V differential signal to a ±10-V single-ended signal. So the INA828 is in unity gain for this example, and no external gain set resistor R_g is needed. See *Circuit for Driving an ADC with an Instrumentation Amplifier in High Gain* in cases where the input signal range is small and gain is required.
2. The INA826 reference voltage (V_{ref}) input is used to shift asymmetrical input ranges to match the input range of the ADC. In this case the input range is symmetrical so the V_{ref} pin is grounded (V_{ref} = 0V). See *Circuit for Driving an ADC with an Instrumentation Amplifier in High Gain* for an example where the V_{ref} pin is used to adjust asymmetrical input signals.
3. Use the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* to determine if the INA828 is violating the common-mode range. The common-mode calculator in the following figure indicates that the output swing is ±14.9V for a 0-V common mode input.



4. Find the value for C_{filt}, and R_{filt} using TINA SPICE and the methods described in *Introduction to SAR ADC Front-End Component Selection*. The value of R_{filt} and C_{filt} shown in this document will work for these circuits; however, if you use different amplifiers you will have to use TINA SPICE to find new values.

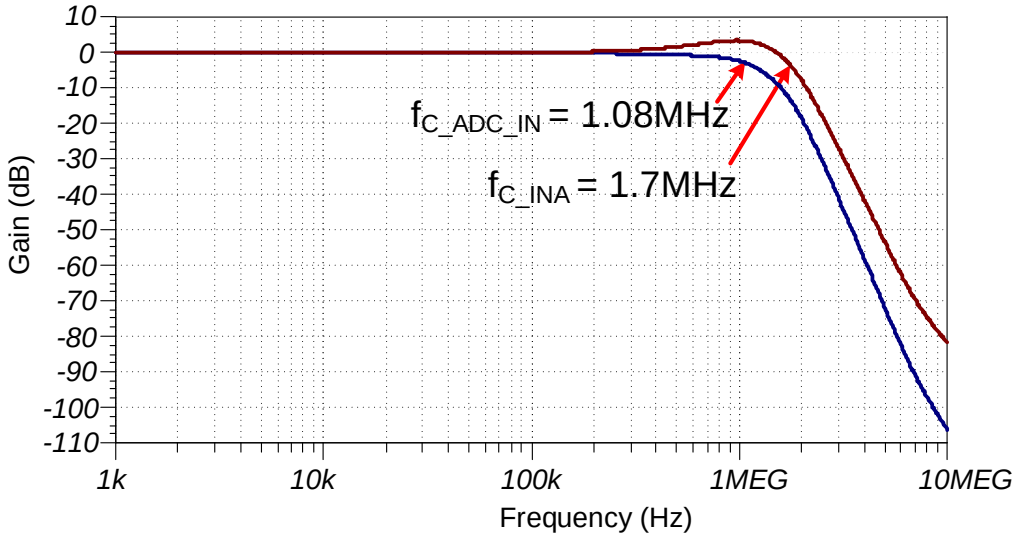
DC Transfer Characteristics

The following graph shows a linear output response for inputs from differential –14.9V to +14.9V. The input range of the ADC is ±10V, so the amplifiers are linear well beyond the required range. See *Determining a SAR ADC's Linear Range when using Instrumentation Amplifiers* for detailed theory on this subject. The full-scale range (FSR) of the ADC falls within the linear range of the instrumentation amplifier.



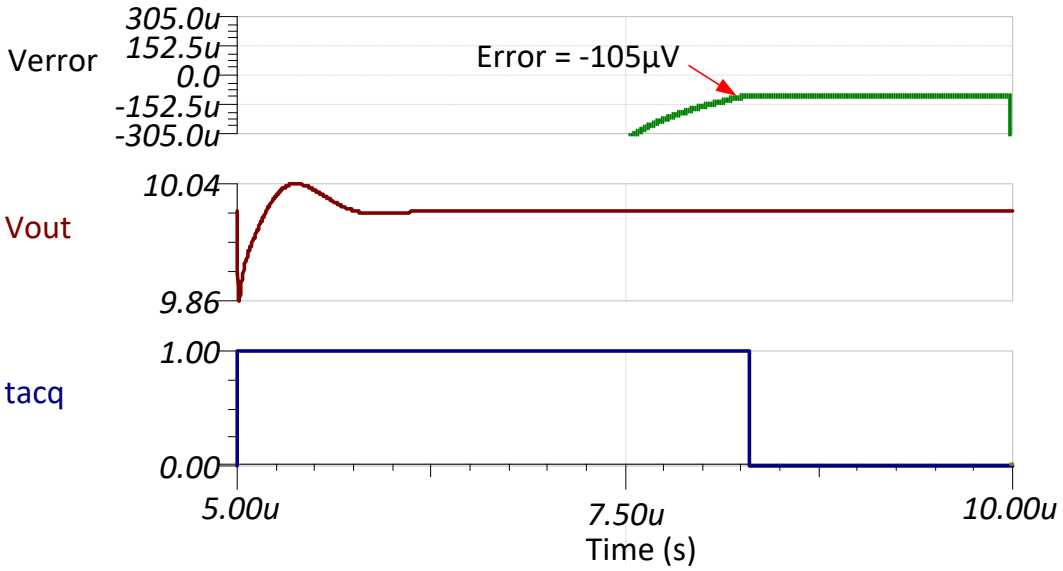
AC Transfer Characteristics

The bandwidth for this circuit is simulated to be 446.75kHz and the gain is 0dB.



Transient ADC Input Settling Simulation (200kSPS)

The following simulation shows settling to a 10-V DC input signal with INA828 and ADS8568. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (152µV) at 200kSPS sampling rate on ADS8568. See the *ADC Front End Component Selection* video series for detailed theory on this subject.



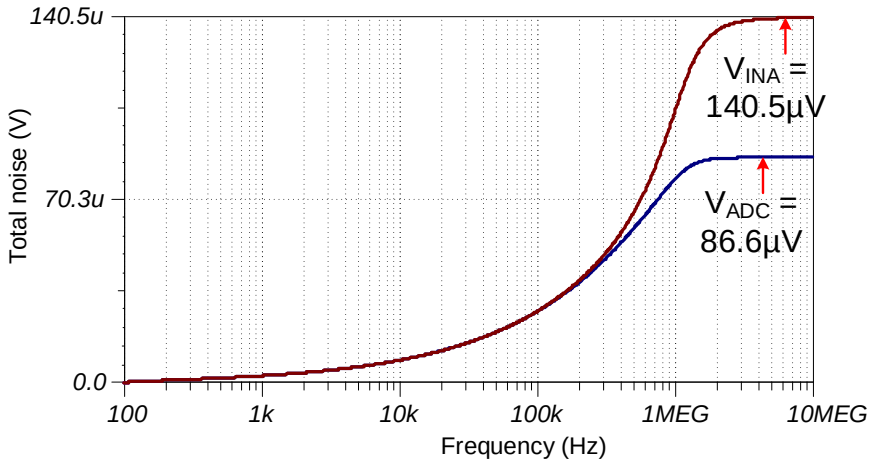
Noise

This section shows a simplified noise calculation for a rough estimate. The bandwidth estimate was taken from the TINA simulation, and the noise density values are from the *INA828 50-µV Offset, 7-nV/√Hz Noise, Low-Power, Precision Instrumentation Amplifier* data sheet. The Kn factor of 1.22 is used because the filter is second order (the INA and output filter both have a pole).

$$E_{n-ADC} = Gain \cdot \sqrt{e_{ni}^{\,2} + \left(\frac{e_{no}}{Gain}\right)^2} \cdot \sqrt{K_n \cdot f_c}$$

$$E_{n-ADC} = 1 \cdot \sqrt{\left(7nV/\sqrt{Hz}\right)^2 + \left(\frac{90nV/\sqrt{Hz}}{1}\right)^2} \cdot \sqrt{1.22 \cdot 1.08MHz} = 103\mu Vrms$$

Note that simulated and calculated are close but not exact (simulated = 86.6µV, calculated = 103µV). The difference is because the INA has gain peaking and the filter order is approximated as two but in reality the INA and filter poles are not exactly aligned.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8860	16-bit resolution, SPI, 1MSPS sample rate, single-ended input, Vref input range 2.5 V to 5.0 V	http://www.ti.com/product/ADS8860	http://www.ti.com/adcs
INA826	Bandwidth 1MHz (G=1), low noise 18nV/√Hz, low offset ±40µV, low offset drift ±0.4µV/ºC, low gain drift 0.1ppm/ºC. (Typical values)	http://www.ti.com/product/INA826	http://www.ti.com/inas

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

Source files for this circuit - http://www.ti.com/lit/zip/SBAC217.

Circuit for driving high-voltage SAR ADC with a buffered instrumentation amplifier

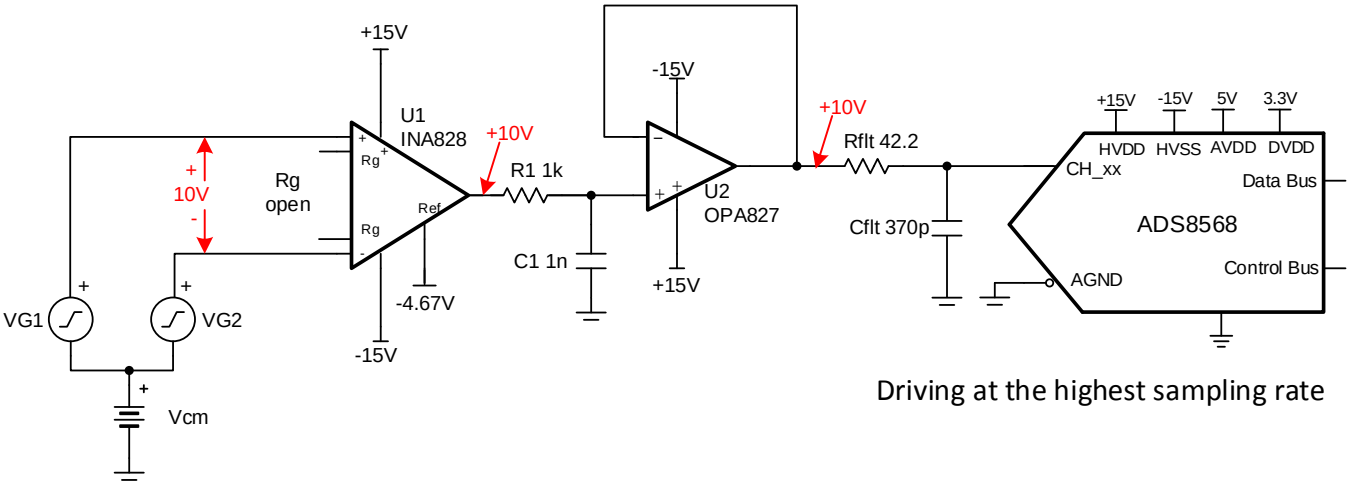
Dale Li

Input	ADC Input	Digital Output ADS7042
VinDiffMin = –10V	CH_x = –10V	8000H
VinDiffMax = +10V	CH_x = +10V	7FFFH

Power Supplies			
AVDD	**DVDD**	**HVDD (V_{CC})**	**HVSS(V_{EE})**
5.0V	3.3V	+15V	–15V

Design Description

Instrumentation amplifiers are optimized for low noise, low offset, low drift, high CMRR and high accuracy but these instrument amplifiers may not be able to drive a precision ADC to settle the signal properly during the acquisition time of ADC. This design will show how a wide bandwidth buffer (OPA827) can be used with an instrumentation amplifier to achieve good settling at higher sampling rate. This INA828 instrumentation amplifier with the buffer drives the ADS8568 SAR ADC to implement data capture for a high voltage fully differential signal which may have a wide common-mode voltage range or a bipolar single-ended signal up to ±10V. A related cookbook circuit shows a simplified approach that does not include the wide bandwidth buffer (*Driving High Voltage SAR ADC with an Instrumentation Amplifier*), this simplified approach has limited sampling rate as compared to the buffered design in this document. This circuit implementation is applicable to *Industrial Transportation* and *Analog Input Modules* that require Precision Signal-Processing and Data-Conversion.



Driving at the highest sampling rate

Specifications

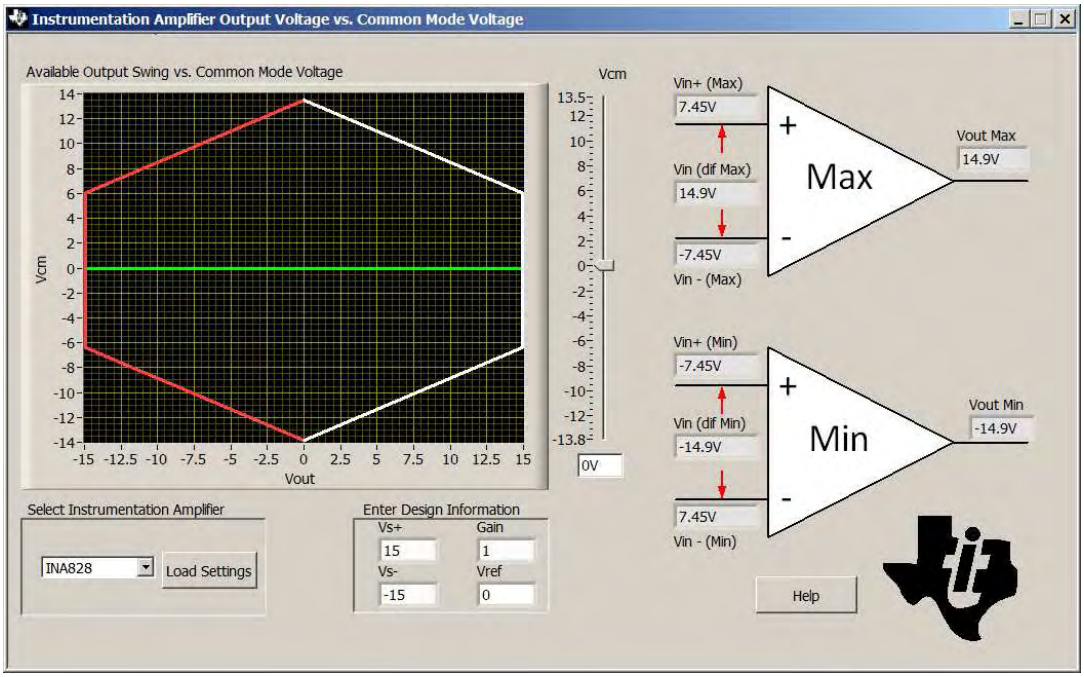
Specification	Goal	Calculated	Simulated
Transient Settling Error	< 1/2LSB (< 152µV)	NA	–346nV
Noise (at ADC Input)	<20µV_{RMS}	47.2µV_{RMS}	46µV_{RMS}

Design Notes

1. The bandwidth of instrumentation amplifiers is typically not enough to drive SAR data converters at higher data rate, so a wide bandwidth driver is needed because the SAR ADC with switched-capacitor input structure has an input capacitor that needs to be fully charged during each acquisition time. The OPA827 buffer is added to allow the ADC to run at full sampling rate (ADS8568 510kSPS for parallel interface).
2. The ADS8568 can accept a ±10-V single-ended input signal. The INA828 is used to translate a ±10-V differential signal to a ±10-V single-ended signal. So the INA282 is in unity gain for this example, and no external gain set resistor Rg is needed. Refer to *Circuit for Driving an ADC with an Instrumentation Amplifier in High Gain* in cases where the input signal range is small and gain is required.
3. Check the common mode range of the amplifier using the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* software tool.
4. Select COG capacitors for C_1 and C_{filt} to minimize distortion.
5. Precision labs video series covers the method for selecting driver amplifier and the charge bucket circuit R_{filt} and C_{filt}. For details, see the *Selecting and Verifying the Driver Amplifier* and *Introduction of SAR ADC Front-End Component Selection* videos.
6. Set the cutoff of the filter between the op amp and instrumentation amplifier for anti aliasing and to minimize noise. See *Aliasing and Anti-aliasing Filters* for more details on aliasing and anti-aliasing filters.

Component Selection

1. Find the gain based on differential input signal and ADC full-scale input range. The input signal in this design is ±10-V high voltage signal, so the Gain of INA828 should be set to 1 and no gain resistor (Rg) is needed.
2. Use the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* to determine if the INA828 is violating the common mode range. The common mode calculator in the following figure indicates that the output swing is ±14.9V for a 0-V common-mode input.

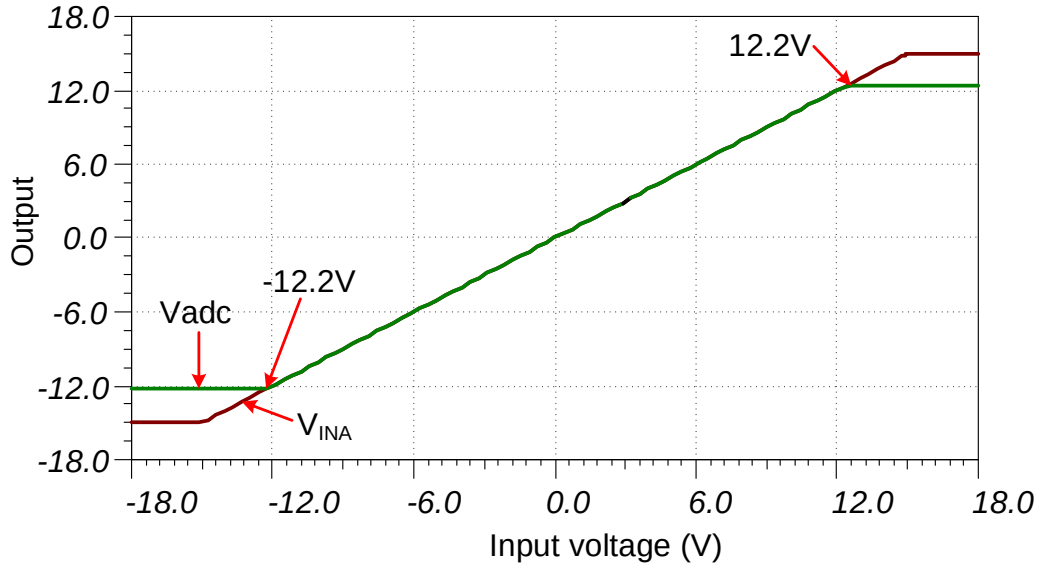


3. Find the value for C_{filt}, and R_{filt} using TINA SPICE and the methods described in *SAR ADC Front-End Component Selection*. The value of R_{filt} and C_{filt} shown in this document will work for these circuits; however, if you use different amplifiers you will have to use TINA SPICE to find new values.
4. Select the RC filter between the INA828 and OPA827 based on your system requirements (f_{cRC} = 15.9kHz in this example). Set the cutoff of this filter for anti aliasing and to minimize noise.

$$f_{cRC} = \frac{1}{2\pi \cdot R_1 \cdot C_1} = \frac{1}{2\pi \cdot (1k\Omega) \cdot (1pF)} = 159\,kHz$$

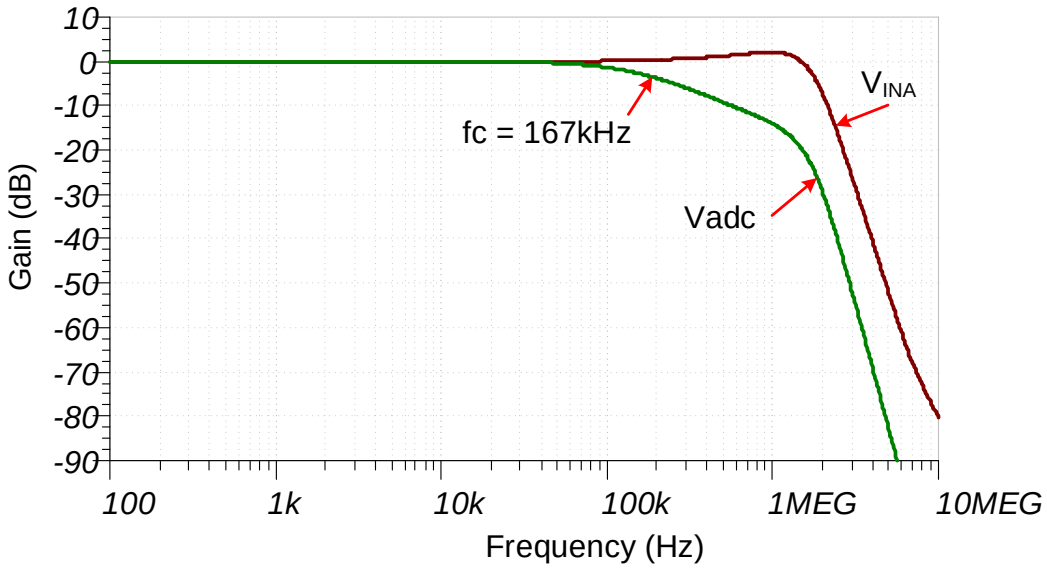
DC Transfer Characteristics

The following graph shows a linear output response for inputs from differential –12.2V to +12.2V. The input range of the ADC is ±10V, so the amplifiers are linear well beyond the required range. Refer to *Determining a SAR ADC's Linear Range when using Instrumentation Amplifiers* for detailed theory on this subject. The full-scale range (FSR) of the ADC falls within the linear range of the Instrumentation Amplifier.



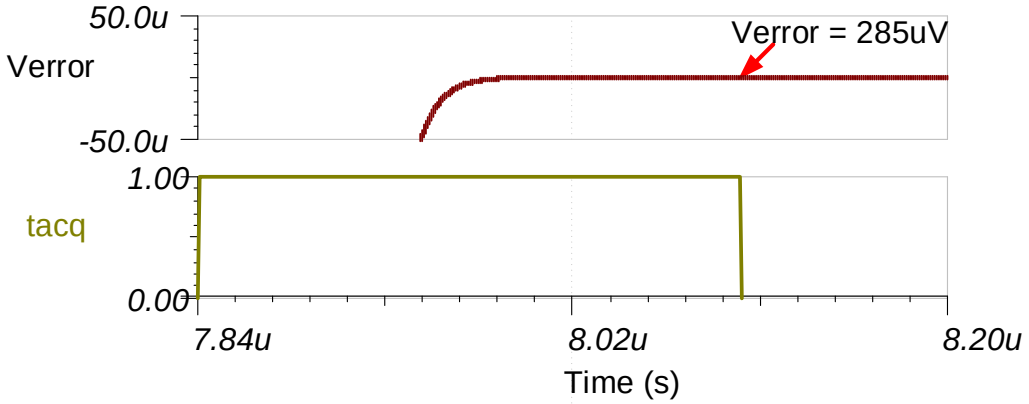
AC Transfer Characteristics

The bandwidth for this system is simulated to be 167kHz and the gain is 0dB. The filter between the OPA827 and INA828 limits the bandwidth to about 167kHz.



Transient ADC Input Settling Simulation (510kSPS)

The OPA827 buffer (22MHz GBW) is used because it is capable of responding to the rapid transients from the ADS8568's charge kickback. The op amp buffer allows the system to achieve the ADS8568 maximum sampling rate of 510kSPS. The following simulation shows settling to a full scale DC input signal with INA828 and OPA827 buffer, and ADS8568. This type of simulation shows that the sample and hold kickback circuit is properly selected to meet desired ½ of a LSB (152µV). Refer to the *Introduction to SAR ADC Front-End Component Selection* training video series for detailed theory on this subject.



Noise Simulation

The section walks through a simplified noise calculation for a rough estimate. We include both the INA828, and OPA827 noise. Note that the RC filter between the instrumentation amplifier and op amp significantly reduces the total noise. The output filter pole is estimated as a second order filter because the OPA827 (22MHz) bandwidth limit and charge bucket filter cutoff frequency (10.2MHz) is close.

$$E_{n-INA} = G\sqrt{e_{n-in}{}^2 + \left(\frac{e_{n-out}}{G}\right)^2} \cdot \sqrt{K_n \cdot f_{cRC}}$$

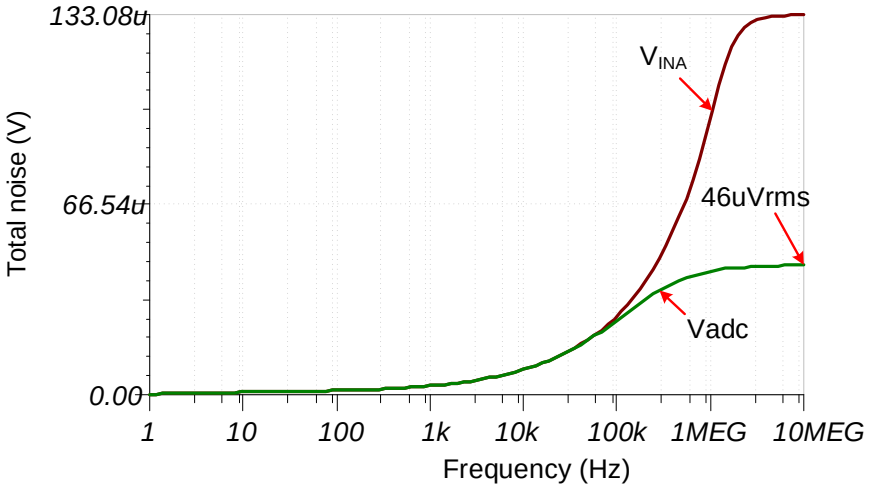
$$E_{n-INA} = 1\sqrt{\left(4nV/\sqrt{Hz}\right)^2 + \left(\frac{90nV/\sqrt{Hz}}{1}\right)^2} \cdot \sqrt{(1.57)\cdot(159kHz)} = 45.1\mu V_{RMS}$$

$$f_{c-adcFilter} = \frac{1}{2\pi \cdot R_{filt} \cdot C_{filt}} = \frac{1}{2\pi \cdot (42.2\Omega)\cdot(370pF)} = 10.2MHz$$

$$E_{opa} = e_{n-opa}\sqrt{K_n \cdot f_c} = \left(4nV/\sqrt{Hz}\right)\sqrt{(1.22)\cdot(10.2MHz)} = 14.1\mu V_{RMS}$$

$$E_{n-total} = \sqrt{E_{n-INA}{}^2 + E_{opa}{}^2} = \sqrt{(45.1\mu V)^2 + (14.1\mu V)^2} = 47.2\mu V_{RMS}$$

Note that calculated and simulated match well- (calculated = 47.2µV, Simulated = 46µV). See *TI Precision Labs - Noise 4* for detailed theory on amplifier noise calculations, and *Calculating Total Noise for ADC Systems* for data converter noise.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8568	16-bit, 8 Channel Simultaneous-Sampling, Bipolar-Input SAR ADC	http://www.ti.com/product/ADS8568	www/ti.com/adcs
INA828	Bandwidth 1MHz (G=1), low noise 18nV/rtHz, low offset ±40μV, low offset drift ±0.4μV/ºC, low gain drift 0.1ppm/ºC. (Typical values)	http://www.ti.com/product/INA828	www.ti.com/inas
OPA827	Gain bandwidth 22MHz, low noise 4nV/rtHz, low offset ±75μV, low offset drift ±0.1μV/ºC (Typical values)	http://www.ti.com/product/OPA827	www.ti.com/opamp

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Links to Key Files

Source files for this circuit - http://www.ti.com/lit/zip/SBAC216.

Circuit for driving high-voltage SAR ADCs for high-voltage, true differential signal acquisition

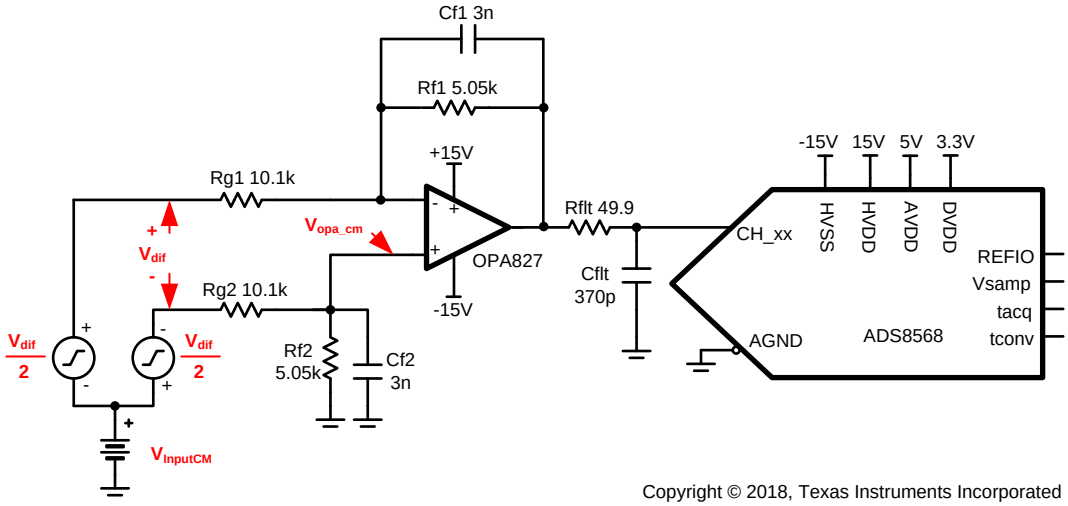
Dale Li

Input	ADC Input	Digital Output ADS7042
VinDiffMin = –20V	CH_x = +10V	7FFF $_{H}$, or 32767 $_{10}$
VinDiffMax = +20V	CH_x = –10V	8000 $_{H}$, or 32768 $_{10}$

Power Supplies			
AVDD	**DVDD**	**V_{CC} (HVDD)**	**V_{SS} (HVSS)**
5.0V	3.3V	+15V	–15V

Design Description

This design shows a solution to drive high-voltage SAR ADC to implement data capture for high-voltage fully differential signal which may have a wide common-mode voltage range depended on amplifier's power supply and input signal's amplitude. A general high-voltage precision amplifier performs the differential to single-ended conversion and drives high-voltage SAR ADC single-ended input scale of ±10V at highest throughput. This type of application is popular in end equipment such as: *Multi-Function Relays*, *AC Analog Input Modules*, and *Control Units for Rail Transport*. The values in the *component selection* section can be adjusted to allow for different level differential input signal, different ADC data throughput rates, and different bandwidth amplifiers.



Specifications

Specification	OPA827 Calculated	OPA827 Simulated	OPA192 Calculated	OPA192 Simulated
Common Mode Input Range (with Vdif = ±20V)	±26V	±26V	±35V	±35V
Transient ADC Input Settling Error	< 1/2LSB (< 152µV)	0.002 LSB (0.568µV)	< 1/2LSB (< 152µV)	0.006 LSB (1.86µV)
Phase Margin of driver	> 45°	67.1°	> 45°	68.6°
Noise (at ADC Input)	14.128µVrms	15.88µVrms	5.699µVrms	6.44µVrms

Design Notes

1. Determine the amplifier gain based on the differential input signal level, the ADC's configuration for input range. This is covered in the *component selection* section.
2. Determine amplifier's linear range based on common mode voltage, input swing, and power supplies. This is covered in the *component selection* section.
3. In this design circuit, the common-mode voltage of the input signal can be any value in the range of $V_{InputCM}$. The derivation of this range is provided in the *component selection* section for the OPA827 and OPA192.
4. Select COG capacitors to minimize distortion.
5. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift, and to minimize distortion. Review *Statistics Behind Error Analysis* for methods to minimize gain, offset, drift, and noise errors.
6. Refer to *Introduction to SAR ADC Front-End Component Selection* for an explanation of how to select Rfilt and Cfilt for best settling and AC performance. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here provide good settling and AC performance for the amplifier and data converter in this example. If the design is modified, select a different RC filter.

Component Selection

1. Find the gain based on differential input signal and ADC full-scale input range.

$$Gain_{OPA} = \frac{\pm V_{ADC(range)}}{\pm V_{DifIn(range)}} = \frac{\pm 10V}{\pm 20V} = 0.5V / V$$

2. Find standard resistor values for differential gain. Use the *Analog Engineer's Calculator* ("Amplifier and Comparator\Find Amplifier Gain" section) to find standard values for Rf/Rg ratio.

$$Gain_{OPA} = \frac{R_f}{R_g} = \frac{5.05k\Omega}{10.1k\Omega} = 0.5$$

3. Find the amplifier's maximum and minimum input for linear operation (that is, the common mode range of the amplifier, V_{cm_amp}). For this example, the OPA827 is used.

$V_- + 3V < V_{cm\_opa} < V_+ - 3V$ from the OPA827 common mode specification

$-12V < V_{cm\_opa} < 12V \quad for \quad \pm 15V \quad supplies$

4. Calculate the maximum common-mode voltage range based on amplifier's input range and previously shown configuration. Refer to the schematic diagram on the first page for better understanding of how V_{cm_opa}, $V_{InputCM}$, and V_{dif} relate to the circuit.

$$V_{cm\_opa} = \left(V_{InputCM} \pm \frac{V_{dif}}{2}\right) \cdot \left(\frac{R_f}{R_f + R_g}\right)$$

$$V_{cm\_opaMin} \cdot \left(\frac{R_f + R_g}{R_f}\right) + \frac{V_{dif}}{2} < V_{InputCM} < V_{cm\_opaMax} \cdot \left(\frac{R_f + R_g}{R_f}\right) - \frac{V_{dif}}{2}$$

5. Solve the equation for the input common-mode range $V_{InputCM}$ for the amplifier. For this example (OPA827), the common mode input can be ±26V with a ±20-V differential input. Using the same method on OPA192 shows a common mode range of ±35V with a ±20-V differential input. Exceeding this common-mode range will distort the signal. Note that this common-mode range was calculated using ±15-V power supplies. The common mode range could be extended by increasing the supply (maximum ±18V).

$$V_{cm\_opaMin} \cdot \left(\frac{R_f + R_g}{R_f}\right) + \frac{V_{dif}}{2} < V_{InputCM} < V_{cm\_opaMax} \cdot \left(\frac{R_f + R_g}{R_f}\right) - \frac{V_{dif}}{2}$$

$$(-12V) \cdot \left(\frac{5.05k\Omega + 10.1k\Omega}{5.05k\Omega}\right) + \frac{20V}{2} < V_{InputCM} < (12V) \cdot \left(\frac{5.05k\Omega + 10.1k\Omega}{5.05k\Omega}\right) - \frac{20V}{2}$$

$$-26V < V_{InputCM} < 26V$$

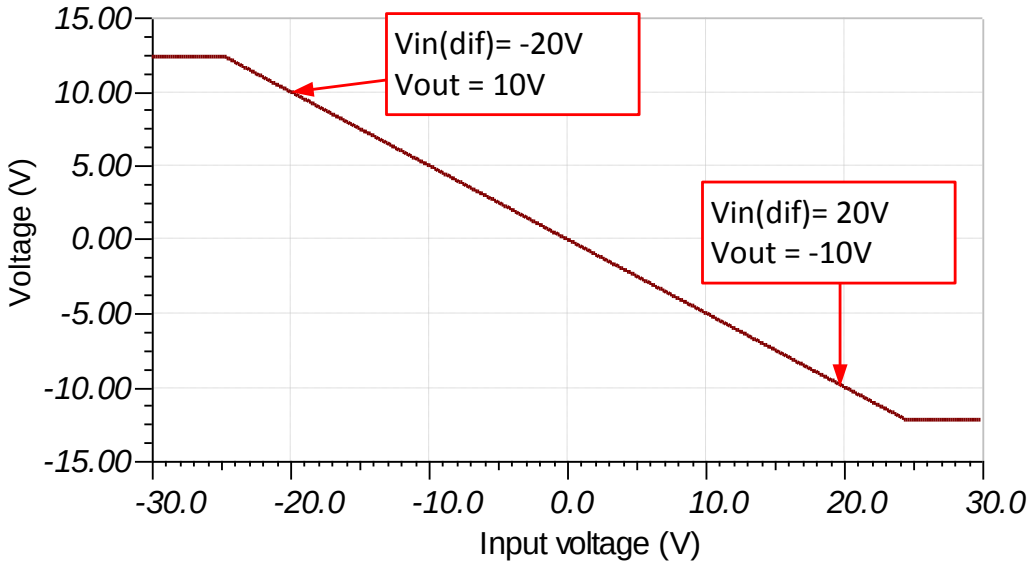
6. Find the value for Cf that will achieve the desired closed-loop bandwidth. In this example we want approximately 10-kHz bandwidth. Note: if you adjust the bandwidth you will need to verify the charge bucket filter settling (C_{filt} and R_{filt}) as the closed-loop bandwidth effects settling.

$$C_f = \frac{1}{2 \cdot \pi \cdot R_f \cdot f_c} = \frac{1}{2 \cdot \pi \cdot (5.05k\Omega) \cdot (10kHz)} = 3.1nF \quad or \quad 3nF \quad standard \quad value$$

7. Find the value for Cfilt and Rfilt using *TINA SPICE* and the methods described in *Introduction to SAR ADC Front-End Component Selection*. The value of Rfilt and Cfilt shown in this document will work for these circuits; however, if you use different amplifiers or different gain settings you must use TINA SPICE to find new values.

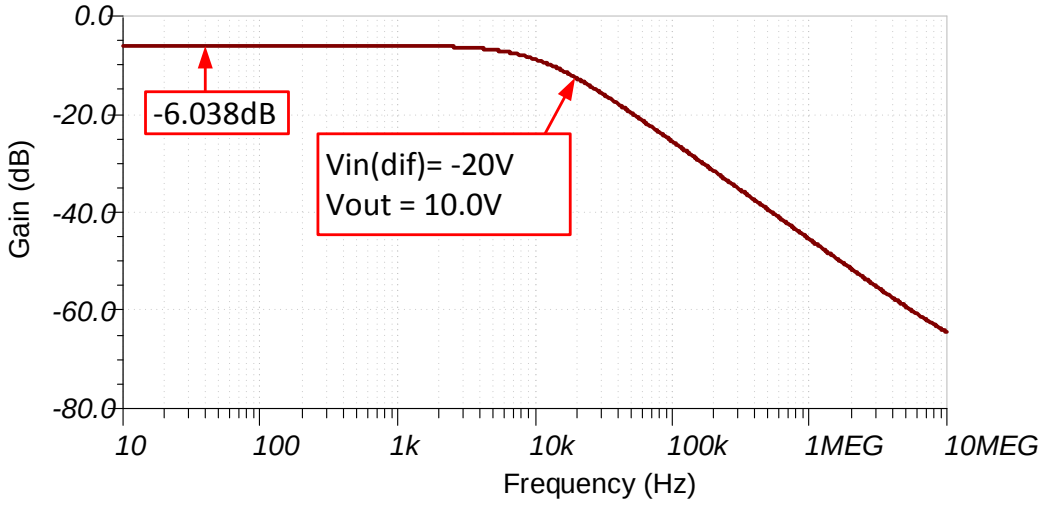
DC Transfer Characteristics

The following graph shows a linear output response for inputs from differential –20V to +20V. The full-scale range (FSR) of the ADC falls within the linear range of the op amp. Refer to *Determining a SAR ADC's Linear Range when using Operational Amplifiers* for detailed theory on this subject.



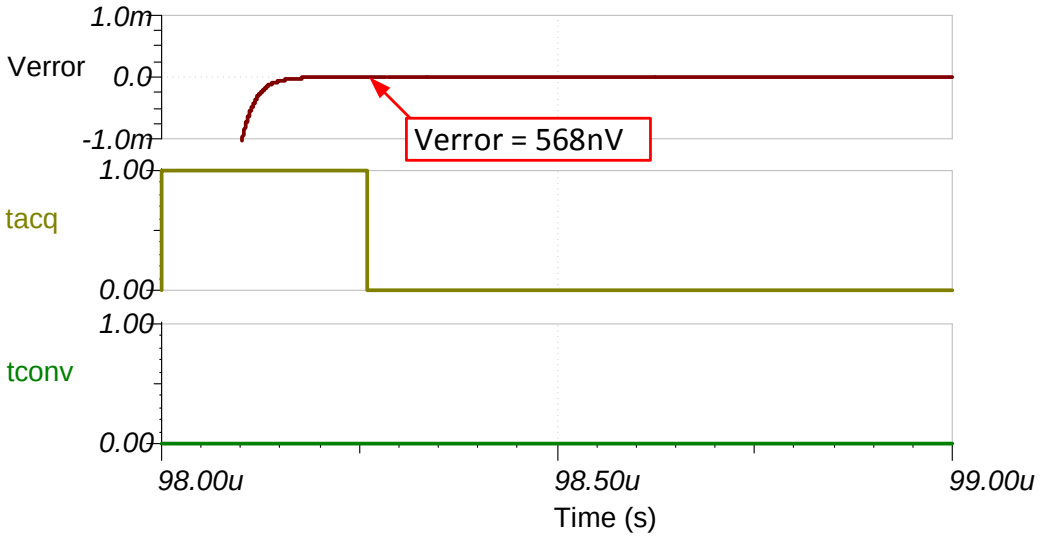
AC Transfer Characteristics

The bandwidth is simulated to be 10.58kHz and the gain is –6.038dB which is a linear gain of 0.5V/V. See the *Op Amps: Bandwidth 1* video for more details on this subject.



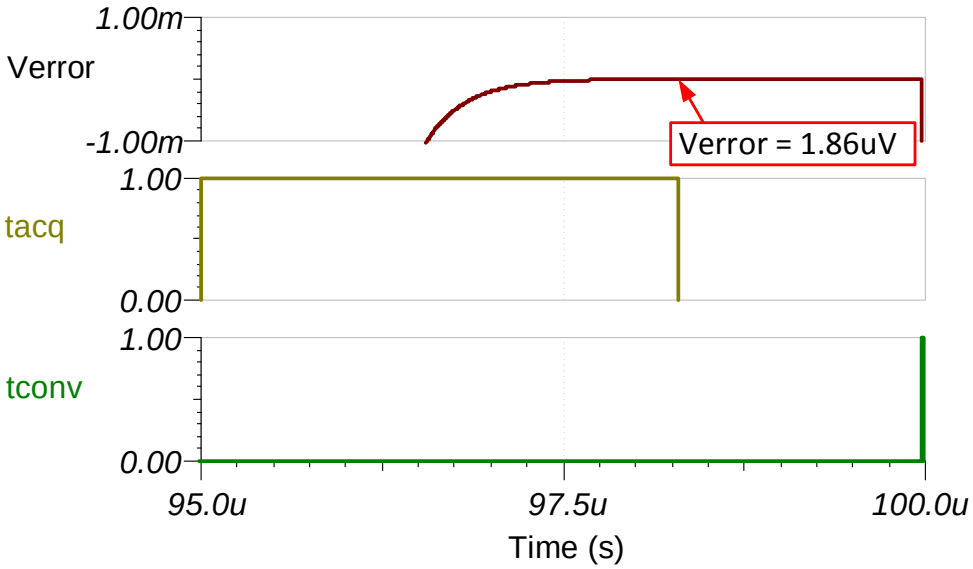
Transient ADC Input Settling Simulation Highest Sampling rate – 510ksps on ADS8568+OPA827

The following simulation shows settling to a 20-V DC input signal with OPA827. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (152µV). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



Transient ADC Input Settling Simulation Lower Sampling rate – 200ksps on ADS8568+OPA192

The following simulation shows settling to a 20-V DC input signal with OPA192. This type of simulation shows that the sample and hold kickback circuit is properly selected to within ½ of a LSB (152µV).



Noise Calculation

This section demonstrates a full-noise analysis including resistor noise. Also, we look at the noise below f_c (Noise Gain = 1.5), and the noise above f_c (noise Gain = 1). In this example, the noise is dominated by wide band amplifier noise so the resistors do not contribute significantly. However, in many cases the resistor noise may be important, so the full noise calculation is provided. Refer to *Calculating the Total Noise for ADC Systems* and *Op Amps: Noise 1* for more detailed theory on this subject.

Bandwidth for feedback loop:

$$f_c = \frac{1}{2 \cdot \pi \cdot R_f \cdot C_f} = \frac{1}{2 \cdot \pi \cdot (5.05k\Omega) \cdot (3nF)} = 10.6kHz$$

Noise from OPA827: 3.8nV/rtHz

$$E_{n\_amp1} = e_{n\_827} \cdot \sqrt{K_n \cdot f_c} = (3.8nV / \sqrt{Hz}) \cdot \sqrt{(1.57) \cdot (10.6kHz)} = 490nVrms$$

Thermal noise density from feedback loop (R_{f1} and R_{g1}) and RC non-inverting input (R_{f2} and R_{g2}):

$$R_{eq} = R_f || R_g = \frac{R_f \cdot R_g}{R_f + R_g} = \frac{(5.05k\Omega) \cdot (10.1k\Omega)}{5.05k\Omega + 10.1k\Omega} = 3.37k\Omega$$

$$e_{n\_feedback} = \sqrt{4 \cdot K_n \cdot T_K \cdot R_{eq}} = \sqrt{4 \cdot \left(1.38 \cdot 10^{-23}\right) \cdot \left(298\right) \cdot \left(3.37k\Omega\right)} = 7.4nV / \sqrt{Hz}$$

$$E_{n\_feedback} = e_{n\_feedback} \cdot \sqrt{K_n \cdot f_c} = (7.4nV / \sqrt{Hz}) \cdot \sqrt{(1.57) \cdot (10.6kHz)} = 0.955\mu Vrms$$

Noise from resistors on the non-inverting input is the same as noise from the feedback resistors.

$$E_{n\_input} = E_{n\_feedback} = 0.955\mu Vrms$$

Total noise (in gain) referred to output of amplifier:

$$E_{n\_below\_fc} = (G_n) \sqrt{{E_{n\_amp1}}^2 + {E_{n\_feedback}}^2 + {E_{n\_input}}^2}$$

$$E_{n\_below\_fc} = (1.5) \sqrt{(0.49\mu V)^2 + (0.995\mu V)^2 + (0.995\mu V)^2} = 2.155\mu Vrms$$

Noise above fc is limited by the output filter (cutoff given below):

$$f_{output} = \frac{1}{2 \cdot \pi \cdot R_{filt} \cdot C_{filt}} = \frac{1}{2 \cdot \pi \cdot (49.9\Omega) \cdot (370pF)} = 8.6MHz$$

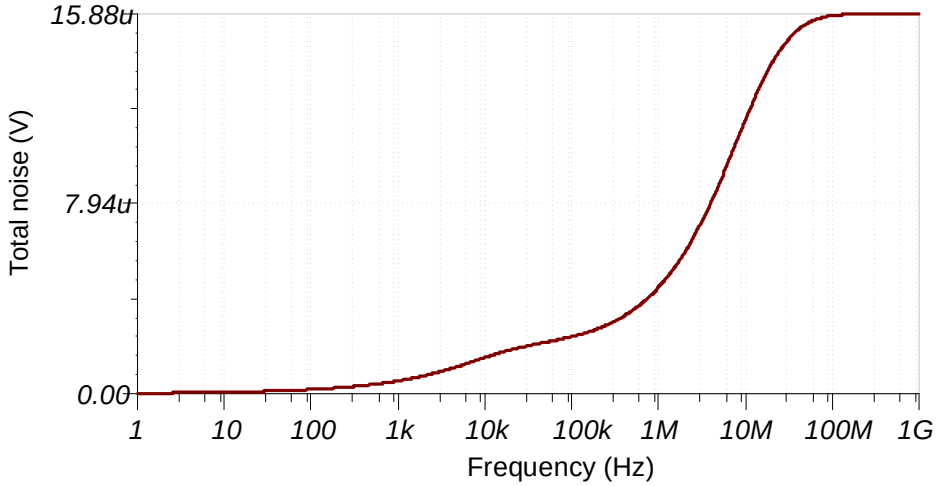
$$E_{n\_above\_fc} = e_{n\_827} \cdot \sqrt{K_n \cdot f_{output}} = (2.8nV / \sqrt{Hz}) \cdot \sqrt{(1.57) \cdot (8.6MHz)} = 13.963\mu V$$

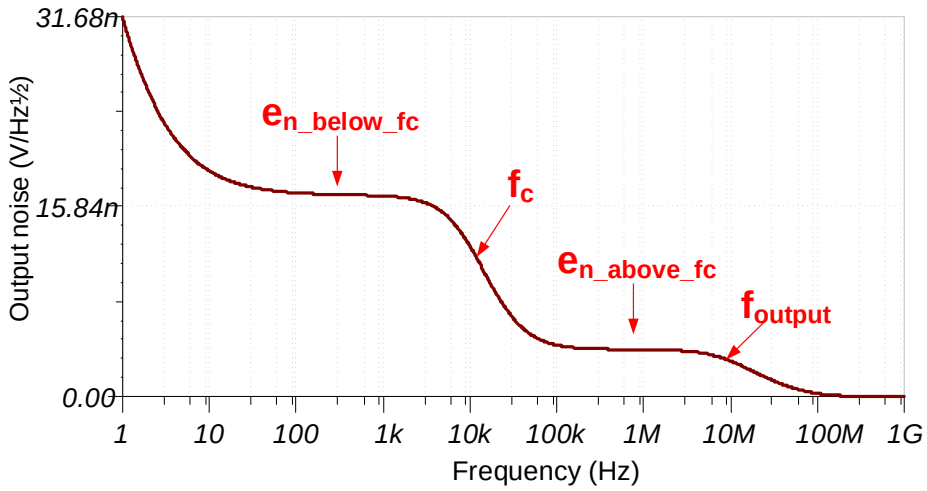
Total noise applied to input of the ADC:

$$E_{n\_total} = \sqrt{{E_{n\_below\_fc}}^2 + {E_{n\_above\_fc}}^2} = \sqrt{(2.155\mu V)^2 + (13.963\mu V)^2} = 14.128\mu Vrms$$

Noise Simulation

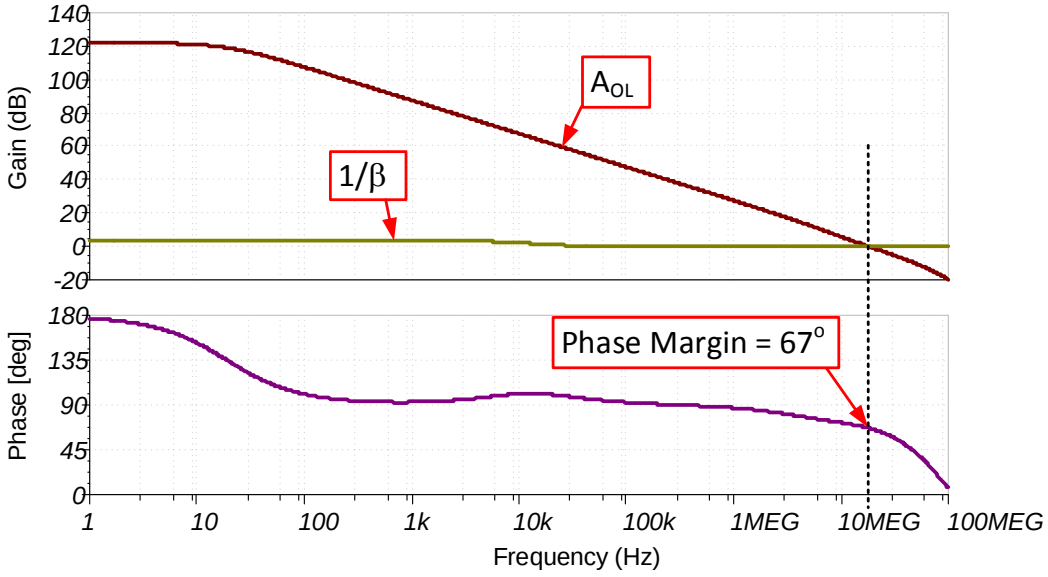
The simulated results compare well with the calculated results (that is, simulated = 15.88µVrms, calculated = 14.128µVrms).

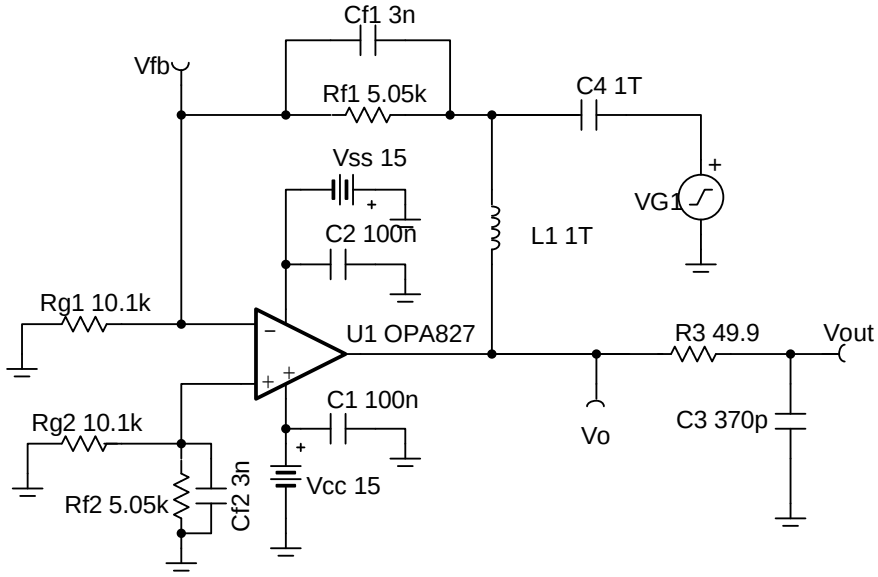




Stability Test

The phase margin for this OPA827 driving circuit is 67.1°, which meets the >45° requirement and is stable. Refer to *Op Amps: Stability 1* for detailed theory explaining stability analysis.





Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8568 (1)	16-bit, 8 Channel Simultaneous-Sampling, Bipolar-Input SAR ADC	www.ti.com/product/ADS8568	www.ti.com/adcs
OPA827	Low-Noise, High-Precision, JFET-Input Operational Amplifier	www.ti.com/product/OPA827	www.ti.com/opamp
OPA192	High-Voltage, Rail-to-Rail Input/Output, 5µV, 0.2µV/°C, Precision operational amplifier	www.ti.com/product/OPA192	www.ti.com/opamp

(1) The ADS8568 has integrated a precision voltage reference which can meet most design requirements, but an external REF5050 can be directly connected to the ADS8568 without any additional buffer because the ADS8568 has a built in internal reference buffer for every ADC channel pair. Also, REF5050 has the required low noise and drift for precision SAR applications. C1 is added to balance CMRR (common-mode rejection ratio). Clean analog power supplies are required to achieve best performance specified in the data sheet of the ADC.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files (TINA)

Design files for this circuit – http://www.ti.com/lit/zip/sbac180.

Revision History

Revision	Date	Change
A	March 2019	Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page.

Circuit to increase input range on an integrated analog front end (AFE) SAR ADC

Cynthia Sosa

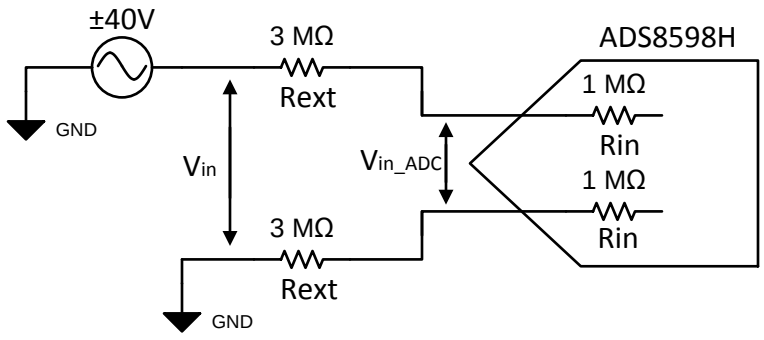
Input	ADC Input	Digital Output
VinMin = –40V	AIN-xP = –10V, AIN-xGND = 0V	-131072_{10} or 20000_{H}
VinMax = 40V	AIN-xP = 10V, AIN-xGND = 0V	131071_{10} or $1FFFF_{H}$

Power Supplies	
AVDD	**DVDD**
5V	3.3V

Design Description

This cookbook design describes how to expand the input range of a SAR ADC with an integrated analog front end (AFE) and decrease the loss of accuracy by implementing a two-point calibration method. This design uses the ADS8598H at the full scale range of ±10V and expands the accessible input range to ±40V. This allows for a wider input range to be used without extra analog circuitry to step down the voltage; instead a simple voltage divider is used to interact with the AFE of the device to step down the voltage near the device input. A calibration method can be implemented to eliminate any error that could occur.

A similar cookbook design, *Reducing Effects of External RC Filter on Gain and Drift Error for Integrated AFE: ±10 V, up to 200kHz, 16 bit*, explaining how to measure introduced drift from external components can prove to also be helpful in this application. Increasing the input range that the ADC can measure proves useful in end equipment such as: *Data Acquisition Modules*, *Multi Function Relays*, *AC Analog Input Modules*, and *Control Units for Rail Transport*.



Specifications

Specification	Measured Accuracy Without Calibration	Measured Accuracy With Calibration
±40V	0.726318%	0. 008237%

Design Notes

1. Use low-drift resistors to decrease any error introduced due to temperature drift, such as 50 ppm/°C with 1% tolerance or better. Note that as resistor values increase to 1MΩ and beyond, low-drift precision resistors can become more expensive.
2. An input filter is frequently required for this configuration. Placing it directly after the large input impedance can cause errors because of the capacitor leakage. If an input filtering capacitor is needed, an alternate schematic is shown in this design.

Component Selection

The internal impedance of the device is 1MΩ, the external resistor is selected based on the desired extended input range (Vin), in this case ±40V. This external resistor forms a voltage divider with the internal impedance of the device, stepping down the input voltage at the ADC input pins (Vin_{ADC}) within the device input range of ±10V.

1. Rearrange the voltage divider equation to solve for the external resistor value. This same equation can later be used to calculate the expected Vin_{ADC} value from the input voltage.

$$V_{in_{ADC}} = V_{in} \cdot \frac{R_{in}}{R_{in} + R_{ext}}$$

$$R_{ext} = \frac{V_{in} \cdot R_{in}}{V_{in_{ADC}}} - R_{in}$$

2. Solve for the external resistor value for the desired extended input voltage. Vin = ±40V, Rin = 1M Ω

$$R_{ext} = \frac{40V \cdot 1M\Omega}{10V} - 1M\Omega$$

The input can be extended to a variety of ranges, depending on what external resistor value is used.

Vin	Rext
±40	3MΩ
±30	2MΩ
±20	1MΩ
±12	200kΩ

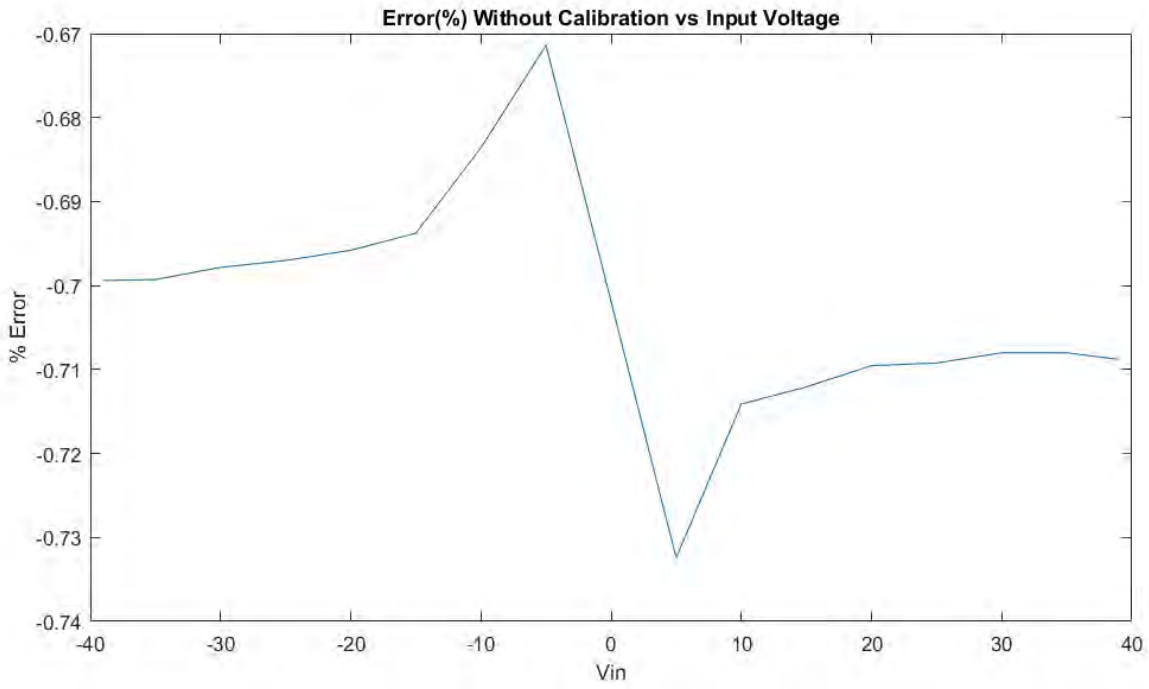
Non-Calibrated Measurements

Different DC input values ranging through the full ±40-V scale were used to measure the ADC voltage input and the accuracy of the measurement. The following equation shows how to calculate the analog voltage read by the ADC. Here the FSR is the system full scale range which is 40V in this case. The factor of 2 is included because this is a bipolar input where the input range is actually ±40V which is a range of 80V. $Vout_{ADC}$ for this equation will range ±40V, which corresponds to the system input.

$$V_{out\,ADC} = Code_{out} \frac{2 \cdot FSR}{2^N}$$

The percent error of the value is calculated using the next equation:

$$Error(\%) = \frac{V_{in\,ADC} - V_{out\,ADC}}{V_{in\,ADC}} \cdot 100$$



Two-Point Calibration

Calibration can be applied in order to eliminate the reading error introduced by the external resistor. The two-point calibration applies and samples two test signals at 0.25V from the full scale input range within the linear range of the ADC. These sample measurements are then used to calculate the slope and offset of the linear transfer function. Calibration will eliminate both the gain error introduced by the external resistor and the internal device gain error.

1. Apply test signal at –39 V:

Vmin	Measured Code
–39 V	–128689

2. Apply test signal at 39 V:

Vmax	Measured Code
39 V	128701

3. Calculate slope and offset calibration coefficients:

$$\text{Error}(\%) = \frac{V_{in_{ADC}} - V_{out_{ADC}}}{V_{in_{ADC}}} \cdot 100$$

$$m = \frac{Code_{max} - Code_{min}}{V_{max} - V_{min}} = \frac{128701 - (-128689)}{39V - (-39V)} = 3299.872$$

$$b = Code_{min} - m \cdot V_{min} = -128689 - 3299.872 \cdot (-39V) = 6.008$$

4. Apply calibration coefficients to all subsequent measurements:

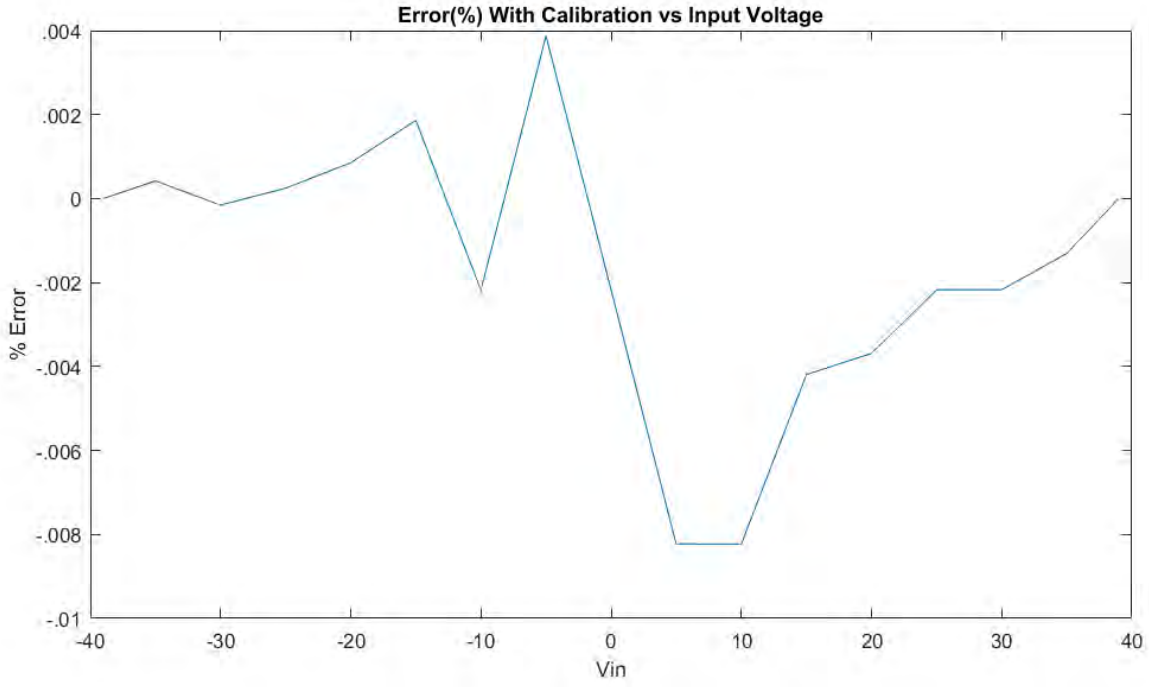
$$V_{in_{Calibrate}} = \frac{Code - b}{m} = \frac{128701 - 6.008}{3299.872} = 38.999$$

Two-Point Calibration Measurements

Calibration Coefficients

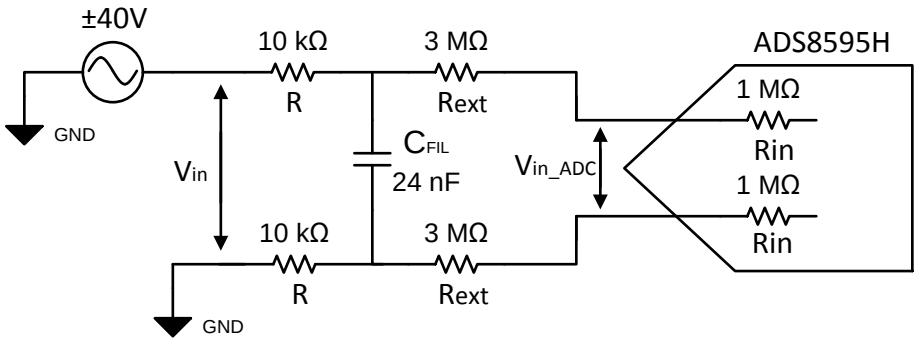
m = 3299.872; *b* = 6.008

When calibration is applied the readings error is dramatically reduced.



Alternate Schematic With Filter Capacitor

Due to the high-value resistors used, introducing a capacitor would lead to significant impact in readings, such as increase drift experienced. This is because of the capacitor leakage. This leakage will vary over time and temperature and will generate errors that are difficult to calibrate out. If an input filter is needed, the alternate schematic can be used to implement it. The capacitor is placed with a balanced resistor-capacitor filter before the external resistors in relation to the input signal.



Alternate Schematic With Filter Capacitor - Component Selection

External anti-aliasing RC filters reduce noise and protect from electrical overstress. A balanced RC filter configuration is required for better common-mode noise rejection; matching external resistors are added to both the negative and positive input paths. These external resistors should also be low-drift resistors as stated in the *Design Notes*.

1. Choose a value of R based on the desired cutoff frequency. This example uses a cutoff frequency of 320Hz, and a resistor value of 10kΩ.

   R = 10kΩ

2. Select C_{FIL}

   $$C_{FIL} = \frac{1}{2 \cdot \pi \cdot f_c \cdot 2 \cdot R} = \frac{1}{2 \cdot \pi \cdot 320\text{Hz} \cdot 2 \cdot 10\,\text{k}\Omega} = 24.8\text{nF}$$

   Nearest standard capacitor value available, C_{FIL}= 24 nF

Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8598H	18-bit high-speed 8-channel simultaneous-sampling ADC With bipolar inputs on a single supply	www.ti.com/product/ADS8598H	www.ti.com/adcs

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Revision History

Revision	Date	Change
A	March 2019	Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page.

High common-mode differential input voltage to ±10-V ADC input circuit

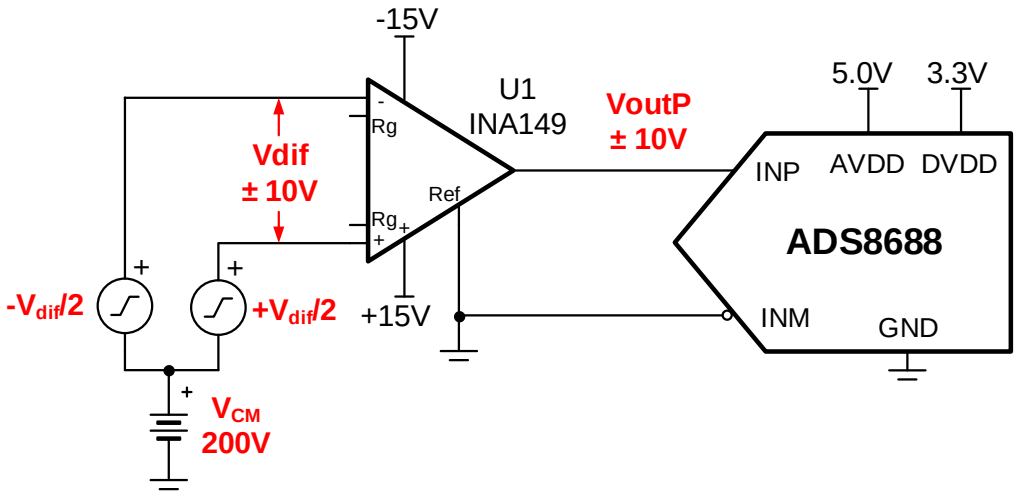
Aaron Estrada

Input	ADC Input	Digital Output ADS8688
VinDiffMin = –10.24V	CH_x = –10.24V	0000_H
VinDiffMax = +10.24V	CH_x = +10.24V	$FFFF_H$

Power Supplies			
AVDD	**DVDD**	**AGND**	**DGND**
5.0V	3.3V	GND	GND

Design Description

The purpose of this cookbook is to demonstrate the advantages and disadvantages of using difference amplifiers or instrumentation amplifiers to translate a signal with a high common mode voltage (Vcm) to a level that the ADS86XX family can accept. The ADS86XX family **cannot** support a high Vcm so using a difference or instrumentation amplifier to drive the ADC solves this issue. The INA828 device is an instrumentation amplifier with very high input impedance (100GΩ), excellent DC precision, and low noise. The INA828 can accept common-mode signals in the range of its supply voltage (±15V). The INA149 device is a unity-gain difference amplifier with a high input common-mode voltage range of up to ±275V, but the input impedance is lower than the INA828 device (differential = 800kΩ, common mode = 200kΩ). The ADS86XX family of ADCs has an integrated analog front end (AFE) and multiplexer which makes it an ideal candidate for a PLC (analog input module), protection relay, grid automation, and other various industrial applications.



Specifications

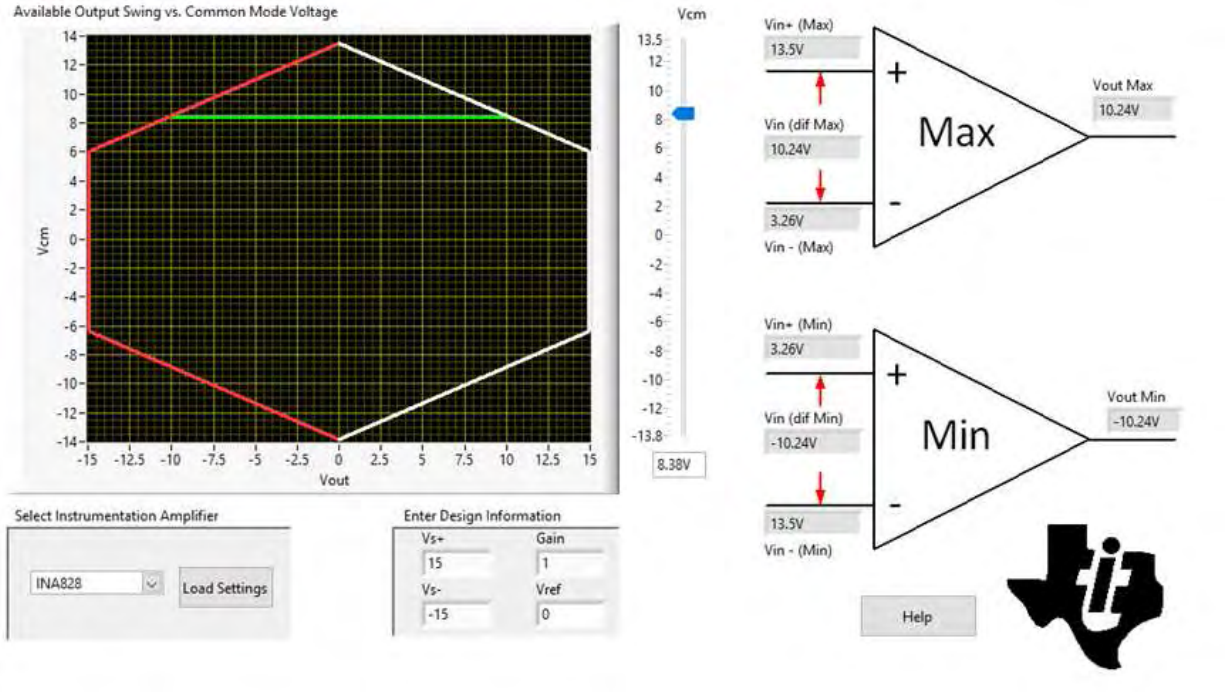
Specification	Calculated	Simulated	Measured
INA149 Common-Mode Voltage (VCM)	275V	275V	275V
INA828 Common-Mode Voltage (VCM)	8.38V	8.38V	7.5V
INA149 Integrated Noise	487µV	487.3µV	488µV
INA828 Integrated Noise	150µV	150µV	154µV

Design Notes

1. The ADS86XX family of HV SAR ADCs was selected because of the integrated analog front end and multiplexer. The integrated AFE eliminates the use of extra components to drive the ADC.
2. The INA149 device was selected to provide a very high common-mode voltage (Vcm = ±275V).
3. Comparing the INA828 device to the INA149 shows that the INA828 device has high input impedance (100GΩ), and the INA149 device has lower input impedance (differential = 800kΩ, common mode = 200kΩ). Also, the INA149 device has very wide common mode (Vcm = ±275V) but the INA828 common mode range is limited to the supply range (for example, ±15V). In cases where high input impedance is required, the INA828 device can be used, but be careful to not violate common-mode range. Note that high input impedance is important when the sensor output impedance is high as this will create a voltage divider effect and introduce error.
4. In this example, the input signal is ±10.24V. Therefore, resistor Rg is not needed in order to set the Gain = 1 for the INA828 device. If the input signal is smaller, use the appropriate resistor value to set the gain with a proper reference voltage on reference pin to achieve an input swing that matches the input range of the ADC.
5. Check the common mode range of the instrumentation amplifier using the Common-Mode Input Range Calculator for Instrumentation Amplifiers software tool.
6. If gain is required, use 0.1% 20ppm/°C film resistors or better for the gain setting resistor (Rg) to achieve best gain accuracy and low gain drift.

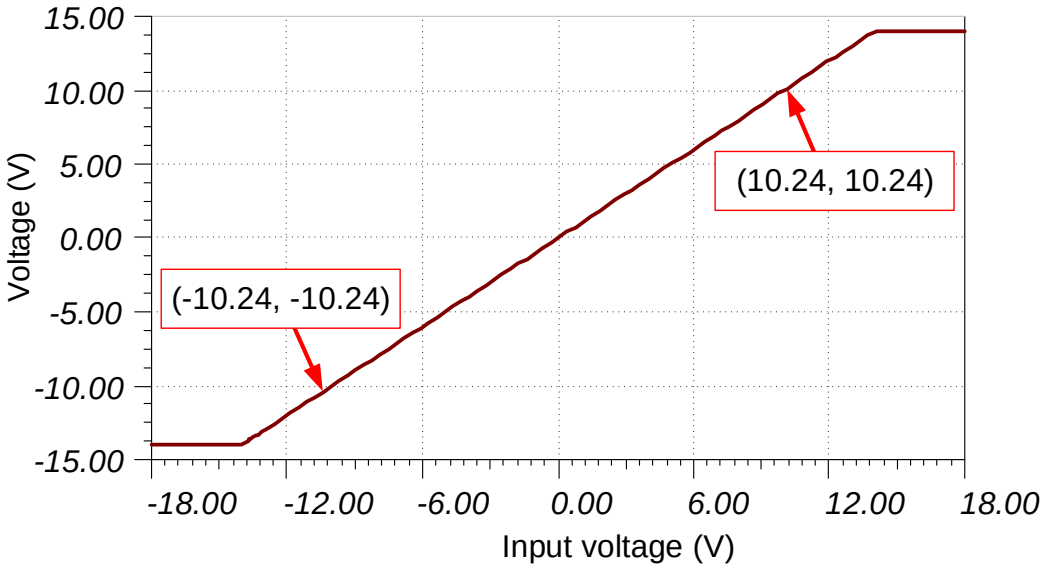
Component Selection

1. The ADS86XX can accept a single-ended input signal of ±10.24V. In this example, the input signal is ±10.24V so no external gain set resistor is required for the INA828 device. The INA149 device is a unity gain difference amplifier so no extra components are necessary.
2. The INA828 reference voltage input is used to shift inputs to match the input range of the ADC. In this example, the ADC input range is symmetrical so the reference pin is grounded.
3. Determine if the INA828 device is violating the common-mode range by using the Common-Mode Input Range Calculator for Instrumentation amplifiers. In this example, the INA828 device shows that you can achieve a maximum VCM of 8.38V with ±15V supplies, Gain = 1, and Vref = 0V.



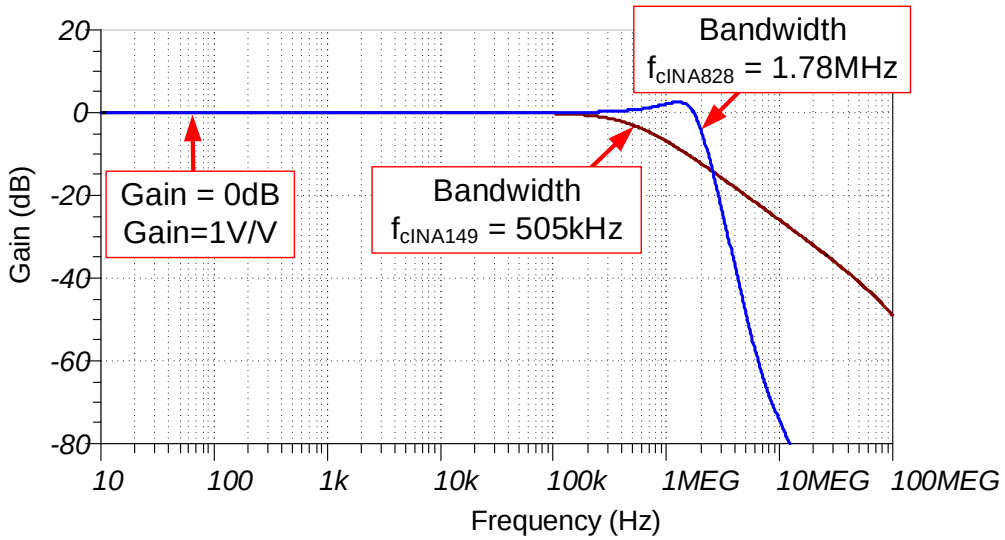
DC Transfer Characteristics

The following graphs show a linear output response for the INA149 device. The input range of the ADC is ±10.24V so the amplifier is linear well beyond the range the ADC requires. Refer to Determining a SAR ADC's Linear Range when using instrumentation amplifiers for detailed theory on this subject.



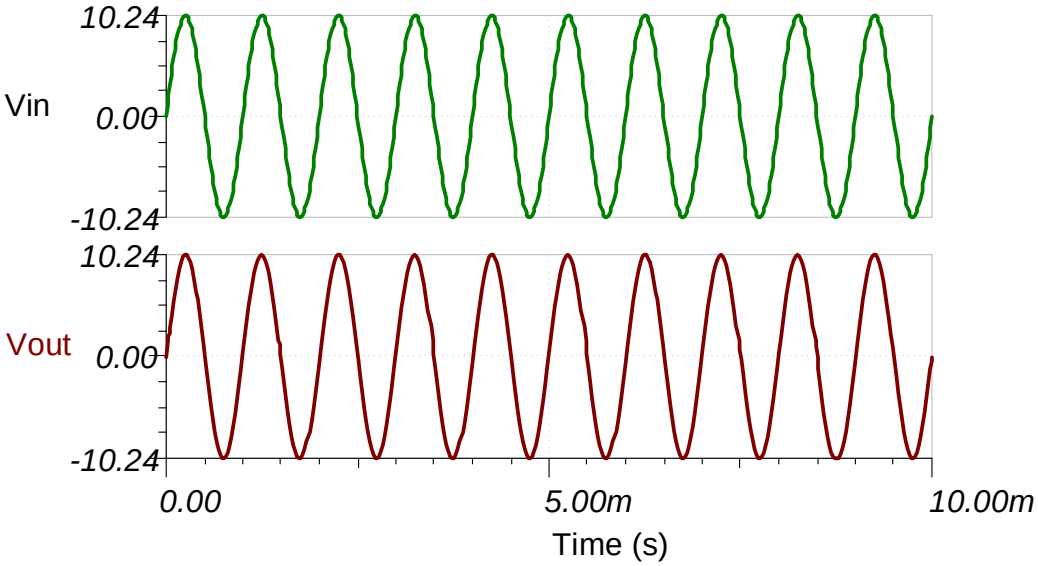
AC Transfer Characteristics

The simulated bandwidth for the INA149 device is 505kHz at gain = 1V/V, or 0dB. The simulated bandwidth for the INA828 device is 1.78MHz at a gain of 0dB. Both of the simulated bandwidths closely match their respective data sheets. See *Amplifier Bandwidth Video Series* for more details on this subject.

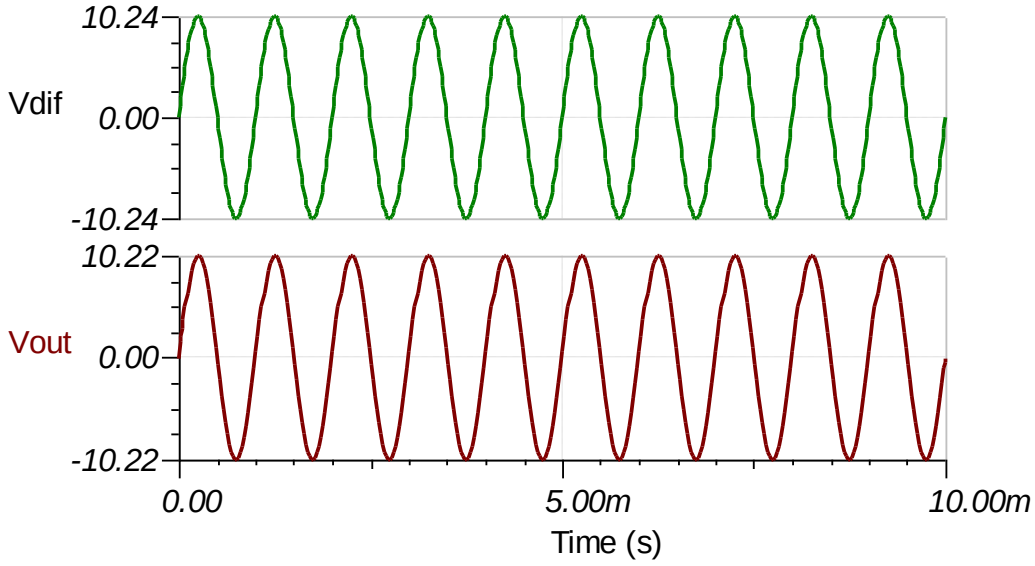


Transient ADC Input Settling Simulation

The INA149 device was simulated with a ±10.24-V differential input and a 275-V common-mode voltage. The following TINA simulation shows the differential input as well as the single-ended output for the INA149 device. The device has no issue with a common-mode voltage of 200V.



The INA828 device was simulated with a ±10.24-V differential input and a 7.75-V common-mode voltage. The following TINA simulation shows the differential input as well as the single-ended output for the INA828 device.



Noise Simulation

The section provides simplified noise calculations for the INA149 and INA828 devices. The simulated results closely match the calculated results. Refer to Op Amps: Noise 4 for detailed theory on amplifier noise calculations, and Calculating Total Noise for ADC Systems for data converter noise.

INA149 integrated noise :

$$E_{nINA149} = e_{ni}\sqrt{f_c \cdot K_n} = \left(550nV / \sqrt{Hz}\right)\sqrt{505kHz \cdot 1.57} = 489\,\mu V_{RMS}$$

INA828 integrated noise :

$$E_{nINA828} = Gain\sqrt{e_{ni}^2 + e_{no}^2}\sqrt{f_c \cdot K_n} = (1)\sqrt{\left(7nV / \sqrt{Hz}\right)^2 + \left(90nV / \sqrt{Hz}\right)^2}\sqrt{1.78MHz \cdot 1.57} = 151\mu V_{RMS}$$

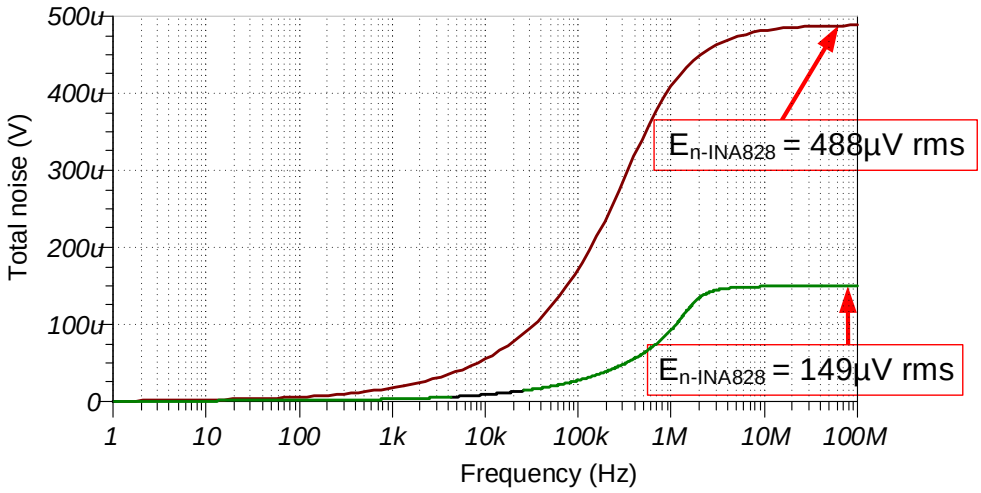
The ADS8688 device has an internal second-order 15-kHz LPF. This filter will reduce the noise from the instrumentation amplifiers significantly.

INA149 integrated noise :

$$E_{nINA149} = e_{ni}\sqrt{f_c \cdot K_n} = \left(550nV / \sqrt{Hz}\right)\sqrt{15kHz \cdot 1.22} = 74.4\,\mu V_{RMS}$$

INA828 integrated noise :

$$E_{nINA828} = Gain\sqrt{e_{ni}^2 + e_{no}^2}\sqrt{f_c \cdot K_n} = (1)\sqrt{\left(7nV / \sqrt{Hz}\right)^2 + \left(90nV / \sqrt{Hz}\right)^2}\sqrt{15kHz \cdot 1.22} = 12.2\,\mu V_{RMS}$$



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS86XX	16-Bit Resolution, 4-,8-Channel MUX, SPI, 500ksps sample rate, on-chip 4.096V Reference	http://www.ti.com/product/ADS8688	http://www.ti.com/adcs
INA149	500kHz BW, Very High VCM, excellent nonlinearity	http://www.ti.com/product/INA149	http://www.ti.com/amplifier-circuit/op-amps/fully-differential/overview.html
INA828	2MHz BW, Low Power12nV/√Hz noise	http://www.ti.com/product/INA828	http://www.ti.com/inas

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

TINA source files – http://www.ti.com/lit/zip/sbac224.

High-current battery monitor circuit: 0–10 A, 0–10 kHz, 18 bit

Luis Chioye

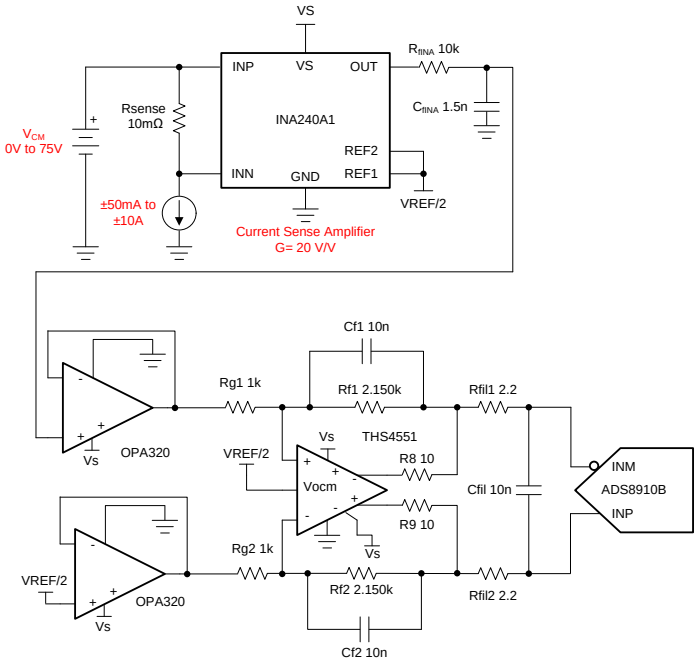
Sense Resistor Current	INA Out, Amplifier Input	ADC Input	Digital Output ADS8910B
MinCurrent = ±50mA	Out = ±10mV	VoutDif = ±21.3mV	233_H 563_{10}, $3FDCB_H$ -564_0
MaxCurrent = +10A	Out = ±2V	VoutDif = ± 4.3V	$1B851^H$ 112722_{10} $247AE_H$ -112722_{10}

Supply and Reference			
Vs	**Vee**	**Vref**	**Vcm**
5.3 V <Vs <5.5V	0V	5V	2.5V

Design Description

This single-supply current sensing solution can measure a current signal in the range of ±50 mA to ±10 A across a shunt resistor. The current sense amplifier can measure shunt resistors over a wide common-mode voltage range from 0V to 75V. A fully differential amplifier (FDA) performs the single-ended to differential conversion and drives the SAR ADC differential input scale of ±5V at full data rate of 1MSPS. The values in the *component selection* section can be adjusted to allow for different current levels.

This circuit implementation is applicable in accurate voltage measurement applications such as Battery Maintenance Systems, Battery Analyzers, *Battery Testing Equipment*, *ATE*, and Remote Radio Units (RRU) in wireless base stations.



Specifications:

Error Analysis	Calculated	Simulated	Measured
Transient ADC Input Settling	> 1LSB > 38µV	6.6µV	N/A
Noise (at ADC Input)	221.8µV rms	207.3µV rms	227µV rms
Bandwidth	10.6kHz	10.71kHz	10.71kHz

Design Notes

1. Determine the shunt sense resistor value and select the current sense amplifier based on the input current range and input common mode voltage requirements. This is covered in the *component selection* section.
2. Determine the fully differential amplifier gain based on the current sense amplifier output, the ADC full-scale range input and the output swing specifications of the fully differential amplifier. This is covered in the *component selection* section.
3. Select COG capacitors to minimize distortion.
4. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift, and to minimize distortion.
5. The TI Precision Labs training video series covers methods for error analysis. Review the following links for methods to minimize gain, offset, drift, and noise errors: *Error and Noise*.
6. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit R_{filt} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and ac performance for the amplifier, gain settings, and data converter in this example. If the design is modified, select a different RC filter. Refer to *Introduction to SAR ADC Front-End Component Selection* for an explanation of how to select the RC filter for best settling and ac performance.

Component Selection for Current Sense Circuit

1. Choose the Rsense resistor and find the gain for the current sense amplifier (bidirectional current).

$$R_{sh} = \frac{V_{sh(max)}}{I_{load(max)}} = \frac{100mV}{10A} = 0.01\Omega$$

$$\pm V_{out(range)} = \pm \frac{V_{REF}}{2} = \pm \frac{5V}{2} = \pm 2.5V$$

$$G_{INA} = \frac{\pm V_{out(range)}}{I_{load(max)} \cdot R_{sh}} = \frac{\pm 2.5V}{10A \cdot 0.01\Omega} = 25V / V$$

2. Calculate the current sense amplifier output range.

$$V_{ina\_outmax} = G_{INA} \cdot (I_{load(max)} \cdot R_{sh}) + \frac{V_{ref}}{2} = (20V / V) \cdot (10A \times 0.01\Omega) + \frac{5V}{2} = 4.5V$$

$$V_{ina\_outmax} = G_{INA} \cdot (I_{load(max)} \cdot R_{sh}) + \frac{V_{ref}}{2} = (20V / V) \cdot (-10A \cdot 0.01\Omega) + \frac{5V}{2} = 0.5V$$

3. Find ADC full-scale input range and results from step 3.

$$ADC_{Full-Scale\ Range} = \pm V_{REF} = \pm 5V$$

4. Find FDA maximum and minimum output for linear operation.

$0.23V < V_{out} < 4.77V$ from THS4551 output low / high specification for linear operation

$V_{out\_FDA\_max} = 4.77V - 0.23V = 4.54V$ Differential max output

$V_{out\_FDA\_min} = -V_{out\_FDA\_max} = -4.54V$ Differential min output

5. Find differential gain based on ADC full-scale input range, FDA output range and results from step 3.

$$Gain = \frac{V_{out\_FDA\_max} - V_{out\_FDA\_min}}{V_{INA\_outmax} - V_{INA\_outmin}} = \frac{4.54V - (-4.54V)}{4.5V - 0.5V} = 2.77V / V$$

$Gain \approx 2.15V / V$ for margin

6. Find standard resistor values for differential gain.

$$Gain_{FDA} = \frac{R_f}{R_g} = 2.15V / V$$

$$\frac{R_f}{R_g} = 2.15V / V = \frac{2.15k\Omega}{1.00k\Omega} = 2.15V / V$$

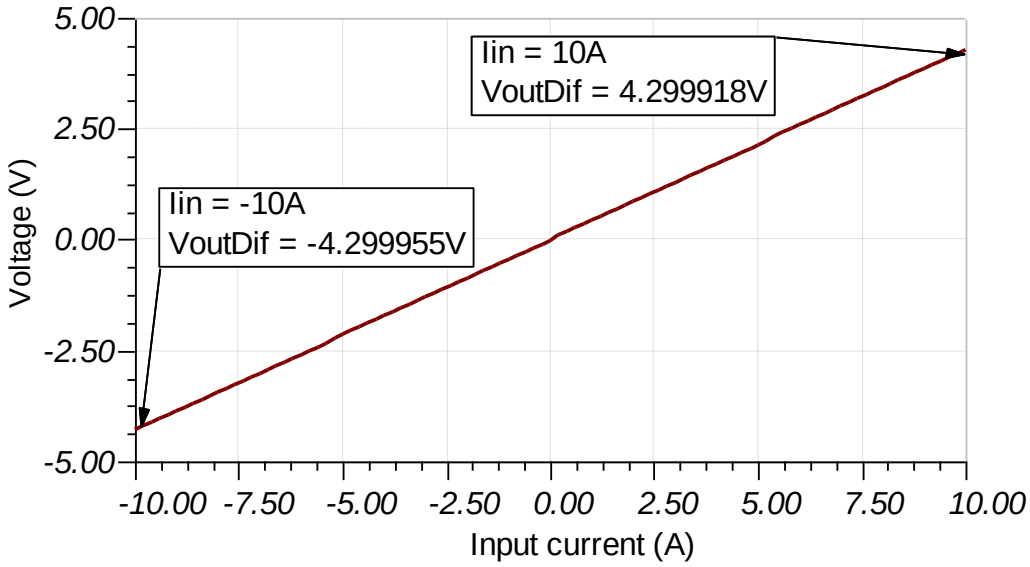
7. Find R_{flNA}, C_{flNA} for cutoff frequency.

$$C_{flNA} = \frac{1}{2 \cdot \pi \cdot f_c \cdot R_{flNA}} = \frac{1}{2 \cdot \pi \cdot 10kHz \cdot 10k\Omega} = 1.591nF \text{ or } 1.5nF \text{ for standard value}$$

$$f_{fina} = \frac{1}{2 \cdot \pi \cdot C_{flNA} \cdot R_f} = \frac{1}{2 \cdot \pi \cdot 1.5nF \cdot 10k\Omega} = 10.6kHz$$

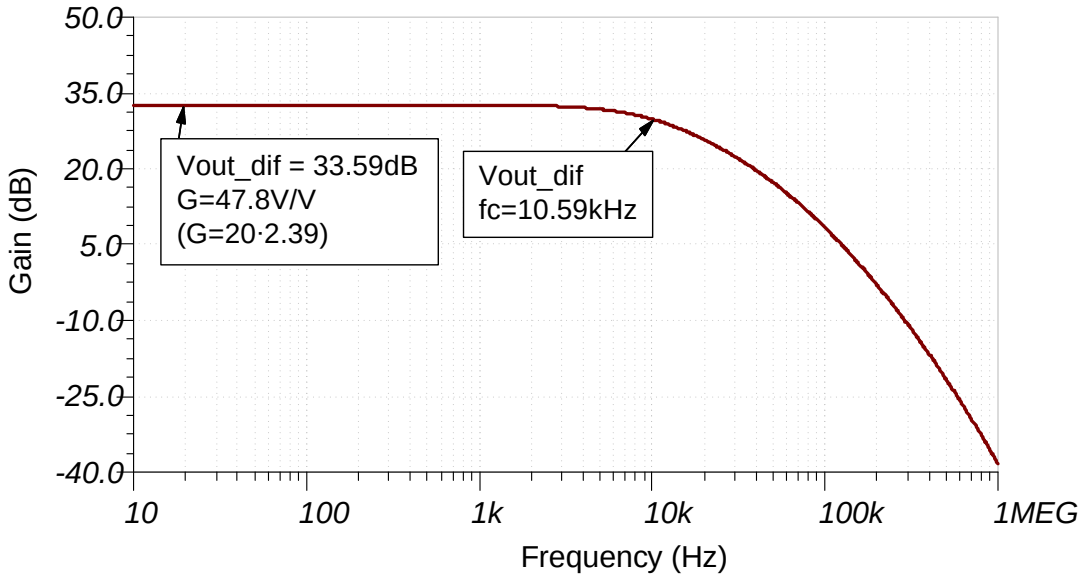
Fully Differential DC Transfer Characteristics

The following graph shows a linear output response for inputs from –10A to +10A.



AC Transfer Characteristics

The bandwidth is simulated to be 10.5kHz and the gain is 32.66dB which is a linear gain of 43V/V (G = 20·2.15V/V).



Noise Simulation

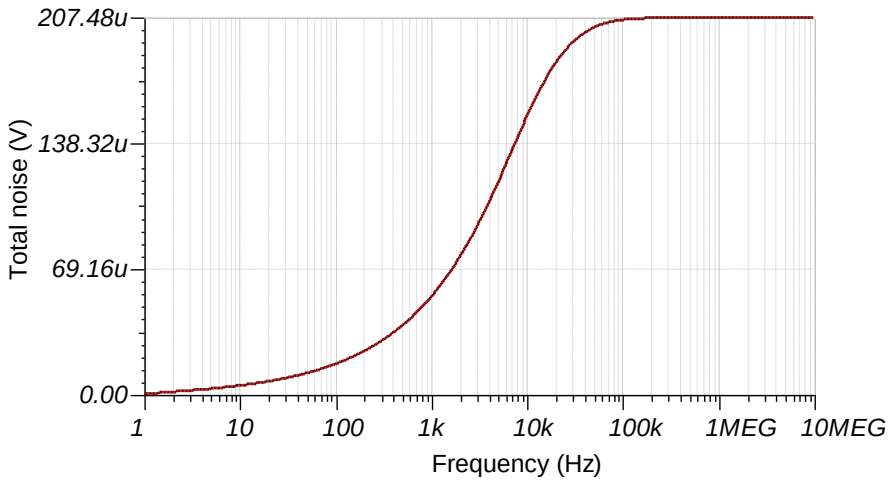
The following simplified noise calculation is provided for a rough estimate. Since the current sense amplifier INA240 is the dominant source of noise, the noise contribution of the OPA320 buffers and THS4521 is omitted in the noise estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10.6kHz.

$$f_c = \frac{1}{2\pi \cdot R_{flNA} \cdot C_{flNA}} = \frac{1}{2\pi \cdot 10k\Omega \cdot 1.5nF} = 10.6kHz$$

$$E_{nINA240} = e_{nINA240} \cdot G_{INA} \cdot \sqrt{K_n \cdot f_c} = (40nV / \sqrt{Hz}) \cdot (20V / V) \cdot \sqrt{1.57 \cdot 10.6kHz} = 103.2\mu V$$

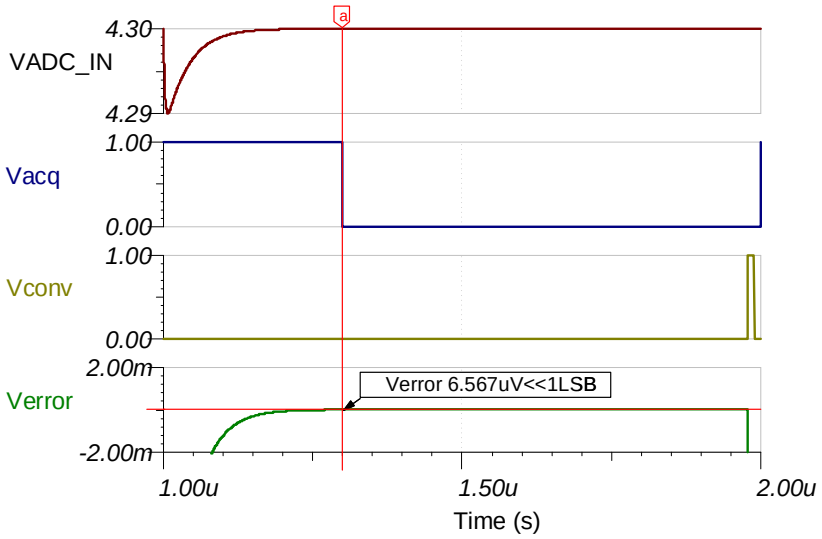
$$E_{nADCIN} = E_{nINA240} \cdot G_{FDA} = (103.2\mu Vrms) \cdot (2.15V / V) = 221.8\mu Vrms$$

Note that calculated and simulated match well. Refer to *Op Amps: Noise 4* for detailed theory on amplifier noise calculations, and *Calculating Total Noise for ADC Systems* for data converter noise.



Transient ADC Input Settling Simulation

The following simulation shows settling to a 10-A DC input signal (ADC differential input signal +4.3V). This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Final SAR ADC Drive Simulations* for detailed theory on this subject.



Design Featured Devices:

Device	Key Features	Link	Similar Devices
ADS8910B(1)	18-bit resolution, 1-Msps sample rate, integrated reference buffer, fully differential input, Vref input range 2.5V to 5V	www.ti.com/product/ADS8910B	www.ti.com/adcs
INA240	High- and low-Side, bi-directional, zero-drift current sense amp, GainError = 0.20%, Gain = 20V/V, wide common-mode = –4V to 80V	www.ti.com/product/INA240	www.ti.com/inas
THS4551	Fully differential amplifier (FDA), 150-MHz bandwidth, Rail-to-Rail output, VosDriftMax = 1.8 µV/°C, e_n = 3.3 nV/rtHz	www.ti.com/product/THS4551	www.ti.com/opamp
OPA320	20-MHz bandwidth, Rail-to-Rail with zero crossover distortion, VosMax = 150 µV, VosDriftMax = 5 µV/C, e_n = 7 nV/rtHz	www.ti.com/product/OPA320	www.ti.com/opamp
REF5050	3 ppm/°C drift, 0.05% initial accuracy, 4 µVpp/V noise	www.ti.com/product/REF5050	www.ti.com/vref

(1) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR applications. The INA240 offers high common-mode range and low gain error in current sensing solutions. The THS4551 is commonly used in high-speed precision fully differential SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling. The OPA320 is required to isolate the INA240 from any residual charge kickback at the inputs of the FDA..

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

ADS8900B Design File – http://www.ti.com/lit/zip/sbam340.

High-input impedance, true differential, analog front end (AFE) attenuator circuit for SAR ADCs

Luis Chioye

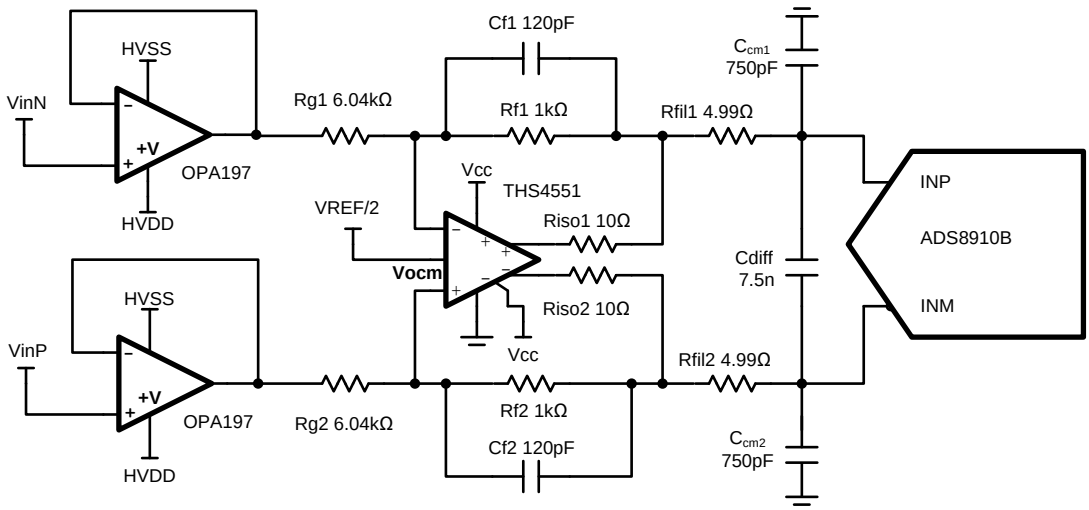
Input Voltage (OPA197 Buffers)	THS4551 Output, ADC Input	ADS8912B Digital Output
VinP = –12V, VinN = +12V, VinMin (Dif) = –24V	VoutDif = –4.00V, VoutP = 0.25V, VoutN = 4.25V	$238E3_H$ -116509_{10}
VinP = +12V, VinN = –12V, VinMax (Dif) = +24V	VoutDif = +4.0V, VoutP = 4.25V, VoutN = 0.25V	$1C71C_H$ +116508_{10}

Supplies and Reference					
HVDD	**HVSS**	**Vcc**	**Vee**	**Vref**	**Vcm**
+15V	–15V	+5.0V	0V	+4.5V	2.5V

Design Description

This analog front end (AFE) and SAR ADC data acquisition solution can measure true differential voltage signals in the range of ±24V (or absolute input range VinP = ±12V, VinN = ±12V) offering high-input impedance supporting data rates up to 500ksps with 18-bit resolution. A precision, 36-V rail-to-rail amplifier with low-input bias current is used to buffer the inputs of a fully-differential amplifier (FDA). The FDA attenuates and shifts the signal to the differential voltage and common-mode voltage range of the SAR ADC. The values in the *component selection* section can be adjusted to allow for different input voltage levels.

This circuit implementation is used in accurate measurement of true differential voltage in *Application-Specific Test Equipment*, *Data Acquisition (DAQ) cards*, and *Analog Input Modules* used in *Programmable Automation Control (PAC)*, *Discrete Control System (DCS)*, and *Programmable Logic Control (PLC)* applications.



Specifications

Specification	Goal	Calculated	Simulated
Transient ADC Input Settling (500ksps)	<< 1 LSB; << 34µV	N/A	0.5µV
Noise (at ADC Input)	$10\mu V_{RMS}$	$9.28\mu V_{RMS}$	$9.76\mu V_{RMS}$
Bandwidth	1.25MHz	1.25MHz	1.1MHz

Design Notes

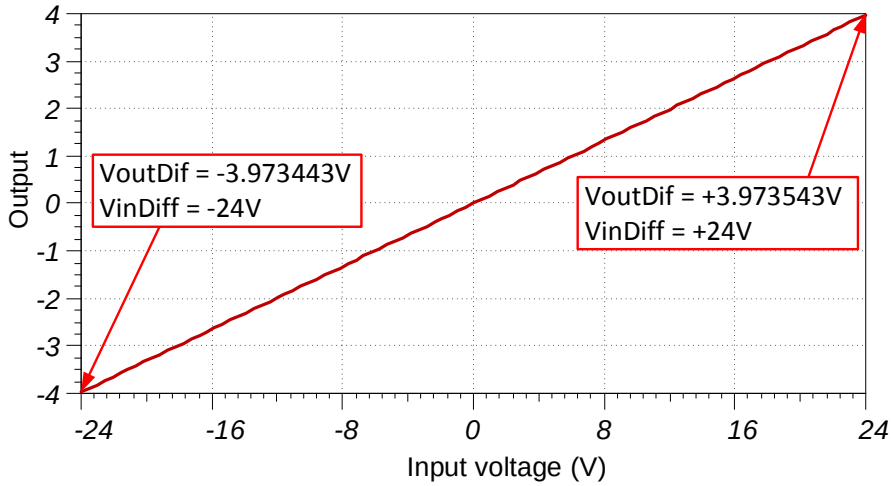
1. Verify the linear range of the op amp (buffer) based on the common mode, output swing specification for linear operation. This is covered in the *component selection* section. Select an amplifier with low input bias current.
2. Find ADC full-scale range and common-mode range specifications. This is covered in the *component selection*.
3. Determine the required attenuation for the FDA based on the input signal amplitude, the ADC full-scale range and the output swing specifications of the FDA. This is covered in the *component selection* section.
4. Select COG capacitors to minimize distortion.
5. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift, and to minimize distortion.
6. *Understanding and Calibrating the Offset and Gain for ADC Systems* covers methods for error analysis. Review the link for methods to minimize gain, offset, drift, and noise errors
7. *Introduction to SAR ADC Front-End Component Selection* covers methods for selecting the charge bucket circuit Rfilt and Cfilt. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier, gain settings, and data converter in this example. If the design is modified, a different RC filter must be selected. Refer to the *Precision Labs* videos for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection and Settings for Buffer Amplifier and FDA

1. Verify the buffer amplifier input range for linear operation:
   Select Supplies $(V-) = -15V$, $(V+) = +15V$ to allow VinP = ±12V VinN = ±12V range
   $(V-) - 0.1V < V_{cm} < (V+) - 3V$ from OPA197 common-mode voltage specification
   $-15.1V < V_{cm} < +12V$ allows required ±12V input voltage range
2. Verify the buffer amplifier output range for linear operation:
   $(V-) + 0.6V < V_{out} < (V+) - 0.6V$ from OPA197 AoI specification for linear operation
   $-14.4V < V_{out} < 14.4V$ allows required ±12V output voltage range
3. Find ADC full-scale input range. In this circuit, $V_{REF} = 4.5V$:
   $ADC_{Full\text{-}Scale\ Range} = \pm V_{REF} = \pm 4.5V$ from ADS8910B data sheet
4. Find the required ADC common-mode voltage:
   $V_{CM} = \frac{+V_{REF}}{2} = +2.25V$ from ADS8910B data sheet, therefore set FDA VCOM = 2.25V
5. Find FDA absolute output voltage range for linear operation:
   $0.23 < V_{out} < 4.77V$ from THS4551 output low / high specification for linear operation
   However, the positive range is limited by $ADC_{Full\text{-}Scale\ Range} = \pm 4.5V$, therefore
   $0.23V < V_{out} < 4.5V$ where $V_{outMin} = 0.23V$, $V_{outMax} = 4.5V$
6. Find FDA differential output voltage range for linear operation. The general output voltage equations for this circuit follow:
   $V_{outMin} = \frac{V_{outDifMin}}{2} + V_{cm}$ and $V_{outMax} = \frac{V_{outDifMax}}{2} + V_{cm}$
   Re-arrange the equations and solve for $V_{outDifMin}$ and $V_{outDifMax}$.
   Find maximum differential output voltage range based on worst case:
   $V_{outDifMax} = 2 \times V_{outMax} - 2 \times V_{cm} = 2 \times (4.5V) - 2 \times (2.25V) = 4.5V$
   $V_{outDifMin} = 2 \times V_{outMin} - 2 \times V_{cm} = 2 \times (0.23V) - 2 \times (2.5V) = -4.04V$
   Based on combined worst case, choose $V_{outDifMin} = -4.04V$ and $V_{outDifMax} = +4.04V$
7. Find the FDA differential input voltage range:
   $V_{inDifMax} = V_{inPmax} - V_{inNmin} = +12V - (-12V) = +24V$
   $V_{inDifMin} = V_{inPmin} - V_{inNmax} = -12V - (+12V) = -24V$
8. Find FDA required attenuation ratio:
   $Gain_{FDA} = \frac{V_{outDifMax} - V_{outDifMin}}{V_{inDifMax} - V_{inDifMin}} = \frac{(+4.04V) - (-4.04V)}{(+24V) - (-24V)} = 0.166 \frac{V}{V} \approx \frac{1}{6} \frac{V}{V}$
9. Find standard resistor values to set the attenuation:
   $Gain_{FDA} = \frac{R_f}{R_g} = \frac{1}{6} V/V \Rightarrow \frac{R_g}{R_f} = \frac{1.00k\Omega}{6.04k\Omega} = \frac{1}{6.04} V/V$
10. Find C_f for cutoff frequency f_c, $R_{fINA} = 1k\Omega$:
    $C_f = \frac{1}{2 \cdot \pi \cdot f_c \cdot R_{fINA}} = \frac{1}{2 \cdot \pi \cdot (1.25MHz) \cdot (1k\Omega)} = 127pF$ or 120pF standard value

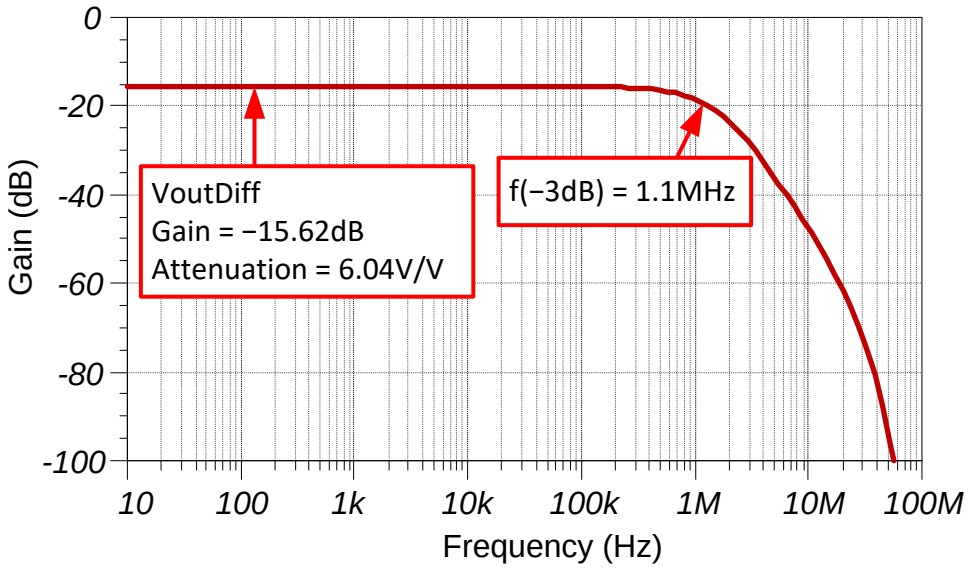
DC Transfer Characteristics

The following graph shows a linear output response for differential inputs from +24V to –24V.



AC Transfer Characteristics

The simulated bandwidth is approximately 1.1MHz and the gain is –15.62dB which is a linear gain of approximately 0.166V/V (attenuation ratio 6.04V/V).



Noise Simulation

Simplified Noise calculation for rough estimate:

$$f_c = \frac{1}{2 \cdot \pi \cdot R_f \cdot C_f} = \frac{1}{2 \cdot \pi \cdot (1k\Omega) \cdot (120pF)} = 1.33MHz$$

Noise contribution of OPA197 buffer referred to ADC input

$$E_{nOPA197} = e_{nOPA197} \cdot \sqrt{K_n \cdot f_c} \cdot Gain_{FDA}$$

$$E_{nOPA197} = \left(5.5nV / \sqrt{Hz}\right) \cdot \sqrt{1.57 \cdot 1.33MHz} \cdot 0.166V / V = 1.319\mu V_{RMS}$$

Noise of THS4551 FDA referred to ADC input

$$\text{Noise gain: } NG = 1 + R_f / R_g = 1 + \frac{1.00k\Omega}{6.04k\Omega} = 1.166V / V$$

$$e_{noFDA} = \sqrt{\left(e_{nFDA} \cdot NG\right)^2 + 2\left(i_{nFDA} \cdot R_f\right)^2 + 2\left(4kTR_f \cdot NG\right)}$$

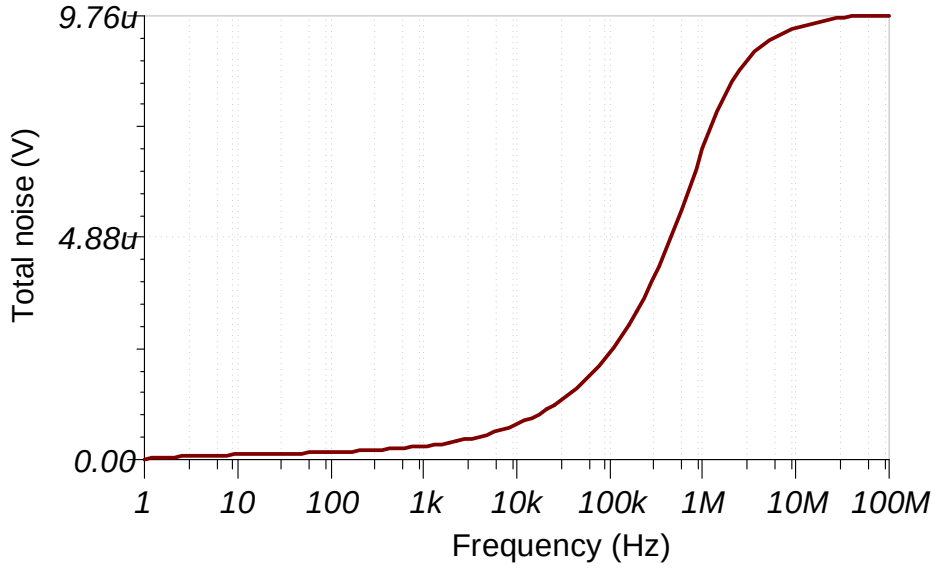
$$e_{noFDA} = \sqrt{\left(3.4nV / \sqrt{Hz} \cdot 1.166V / V\right)^2 + 2\left(0.5pA / \sqrt{Hz} \cdot 1k\Omega\right)^2 + 2\left(16.56 \cdot 10^{-18} \cdot 1.166V / V\right)}$$

$$e_{noFDA} = 7.4nV / \sqrt{Hz}$$

$$E_{nFDA} = e_{noFDA} \cdot \sqrt{K_n \cdot f_c} = \left(7.40nV / \sqrt{Hz}\right) \cdot \sqrt{1.57 \cdot 1.33MHz} = 9.28\mu V_{RMS}$$

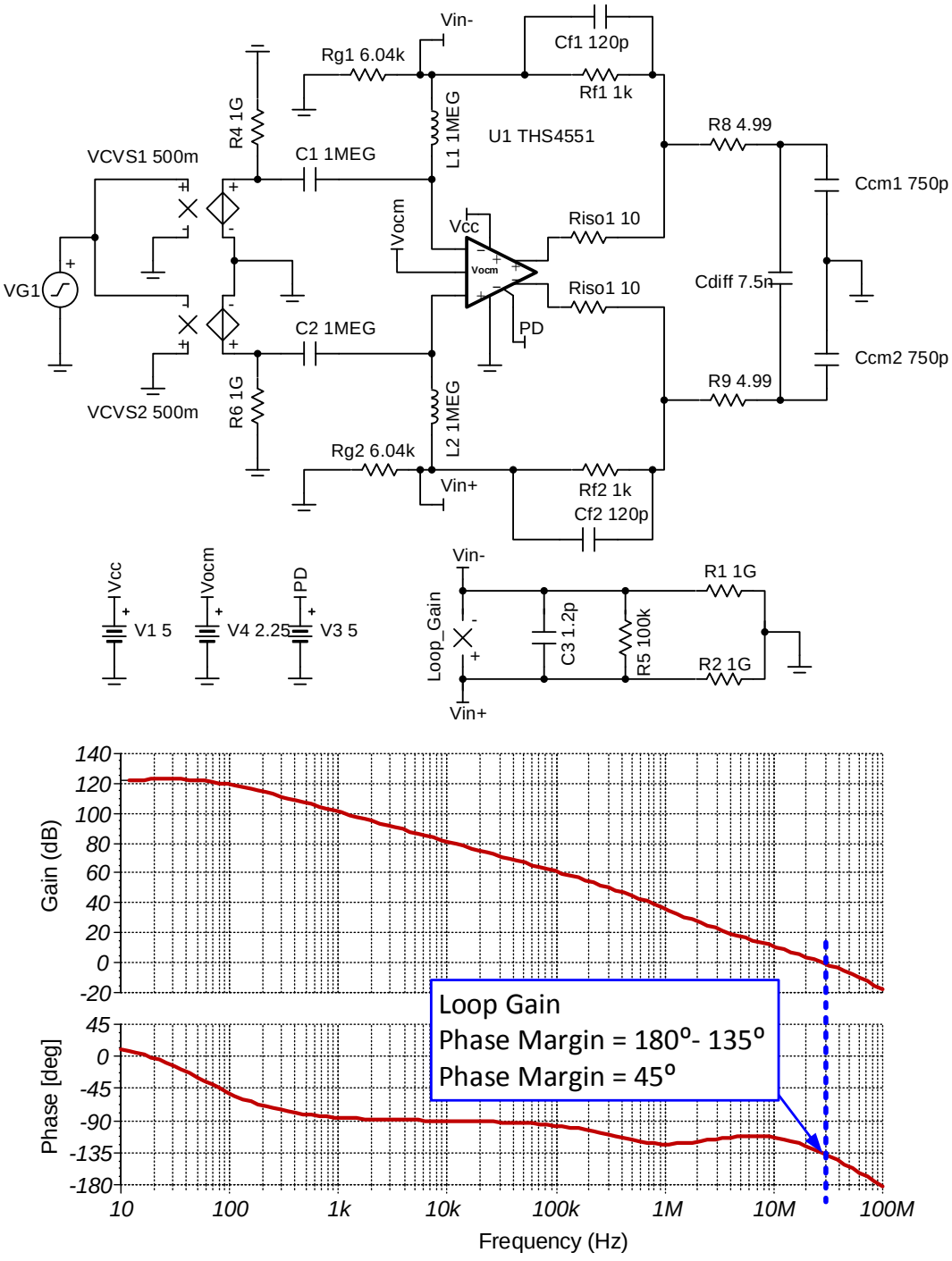
$$\text{Total Noise} = \sqrt{E_{nFDA}{}^2 + E_{nOPA197}{}^2} = \sqrt{\left(9.28\mu V_{RMS}\right)^2 + \left(1.32\mu V_{RMS}\right)^2} = 9.37\mu V_{RMS}$$

Note that calculated and simulated match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



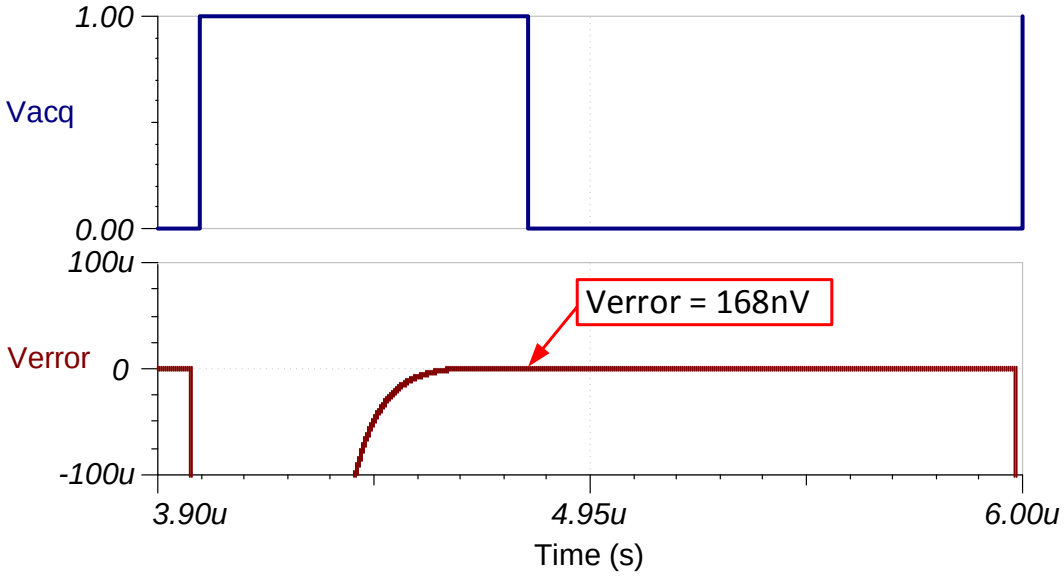
Stability Simulation

The following circuit is used in TINA to measure loop gain and verify phase margin using AC transfer analysis in TINA. Resistors R_{ISO} = 10Ω are used inside the feedback loop to increase phase margin. The circuit has 45 degrees of phase margin. Refer to *TI Precision Labs - Op Amps: Stability 4* for detailed theory on this subject.



Transient ADC Input Settling Simulation

The following simulation shows settling to a 24-V DC differential input signal with the OPA197 buffers inputs set at +12V and –12V. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Refine the Rfilt and Cfilt Values* for detailed theory on this subject.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8912B[1]	18-bit resolution, 500-ksps sample rate, integrated reference buffer, fully-differential input, Vref input range 2.5V to 5V.	www.ti.com/product/ADS8912B	www.ti.com/adcs
THS4551	FDA, 150-MHz bandwidth, Rail-to-Rail Output, VosDriftMax = 1.8µV/°C, e_n = 3.3nV/rtHz	www.ti.com/product/THS4551	www.ti.com/opamp
OPA197	36V, 10-MHz bandwidth, Rail-to-Rail Input/Output, VosMax = ±250µV, VosDriftMax = ±2.5µV/°C, bias current = ±5pA	www.ti.com/product/OPA197	www.ti.com/opamp
REF5045	VREF = 4.5V, 3 ppm/°C drift, 0.05% initial accuracy, 4µVpp/V noise	www.ti.com/product/REF5045	www.ti.com/voltageref

(1) The REF5045 can be directly connected to the ADS8912B without any buffer because the ADS8912B has a built in internal reference buffer. Also, the REF5045 has the required low noise and drift for precision SAR applications. The THS4551 provides the attenuation and common-mode level shifting to the voltage range of the SAR ADC. In addition, this FDA is commonly used in high-speed precision fully-differential SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling. The OPA197 is a 36-V operational amplifier that provides a very high input impedance front end, buffering the FDA inputs

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

Source files for this design – http://www.ti.com/lit/zip/sbac183.

Revision History

Revision	Date	Change
A	March 2019	Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page.

High-voltage battery monitor circuit: ±20V, 0–10kHz, 18-bit fully differential

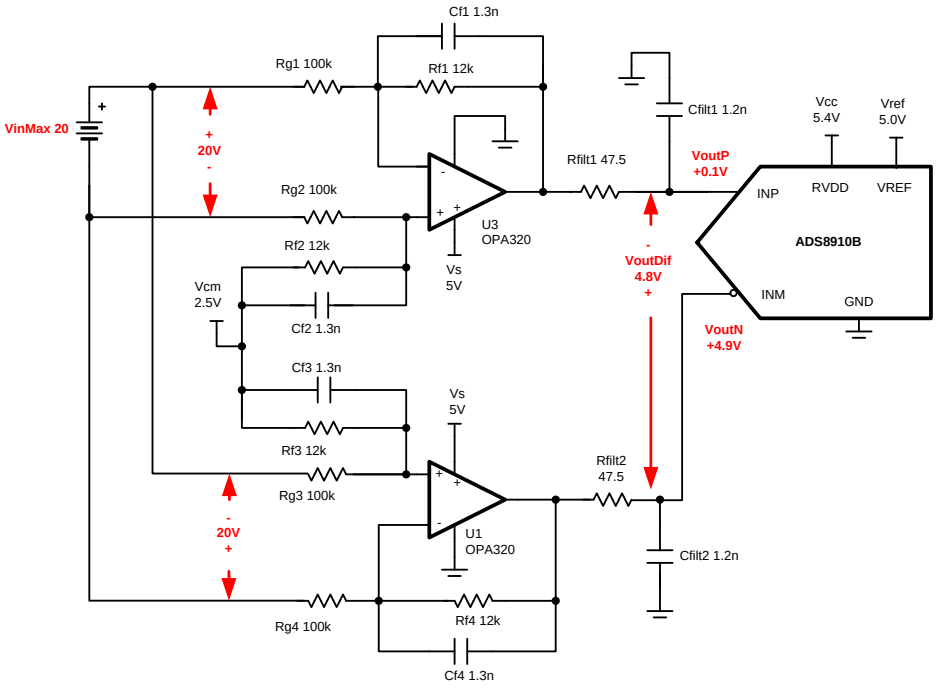
Bryan McKay, Arthur Kay

Input	ADC Input	Digital Output ADS8910
VinMin = –20V	VoutDif = 4.8V, VoutP = 4.9V, VoutN = 0.1V	$1EB85_{H}$ or 125829_{10}
VinMax = 20V	VoutDif = –4.8V, VoutP = 0.1V, VoutN = 4.9V	$2147B_{H}$ or -125829_{10}
Power Supplies		
Vcc	**Vee**	**Vref**	**Vcm**
5.3 V	0 V	5 V	2.5 V

Design Description

This design translates an input bipolar signal of ±20V into a fully differential ADC differential input scale of ±4.8V, which is within the output linear operation of amplifiers. The values in the *component selection* section can be adjusted to allow for different input voltage levels.

This circuit implementation is applicable in accurate voltage measurement applications such as Battery Maintenance Systems, Battery Analyzers, *Battery Testing Equipment*, *ATE*, and Remote Radio Units (RRU) in wireless base stations.



Specifications

Specification	Calculated	Simulated	Measured
Transient ADC Input Settling	< 0.5LSB or 19µV	6.6µV	N/A
Noise	20.7µV rms	20.65µV rms	30.8µV rms
Bandwidth	10.2kHz	10.4kHz	10.4kHz

Design Notes

1. Determine the linear range of the op amp based on common mode, output swing, and linear open-loop gain specification. This is covered in the *component selection* section.
2. For capacitors in the signal path, select COG type to minimize distortion. In this circuit Cf1, Cf2, Cf3, Cf4, Cfilt1, and Cfilt2 need to be COG type.
3. Use 0.1% 20ppm/°C film resistors or better for good gain drift and to minimize distortion.
4. Precision labs video series covers methods for error analysis. Review the *Statistics Behind Error Analysis* for methods to minimize gain, offset, drift, and noise errors.
5. The *TI Precision Labs – ADCs* training video series covers methods for selecting the charge bucket circuit R_{filt} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier, gain settings, and data converter in this example. If the design is modified, select a different RC filter. Refer to *Introduction to SAR ADC Front-End Component Selection* for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. The general equation for this circuit.

$$V_{outMinOpa} = \frac{V_{outDifMin}}{2} + V_{cm}$$

$$V_{outMaxOpa} = \frac{V_{outDifMax}}{2} + V_{cm}$$

$$V_{outDif} = V_{inDif} \times Gain_{dif}$$

$$Gain_{dif} = 2 \times \frac{R_f}{R_g}$$

2. Find op amp maximum and minimum output for linear operation.

$-0.1\,V < V_{cm} < 5.1V$ from OPA320 Vcm specification

$0.035\,V < V_{out} < 4.965\,V$ from OPA320 Vout swing specification

$0.1\,V < V_{out} < 4.9\,V$ from OPA320 Aol specification for linear operation

$0.1\,V < V_{out} < 4.9\,V$ Combined worst case

3. Rearrange the equation from part 1 and solve for VoutDifMin and VoutDifMax. Find maximum and minimum differential output voltage based on combined worst case from step 2.

$$V_{outDifMax} = 2 \cdot V_{outMaxOpa} - 2 \cdot V_{cm} = 2 \cdot (4.9\,V) - 2 \cdot (2.5\,V) = 4.8\,V$$

$$V_{outDifMax} = 2 \cdot V_{outMinOpa} - 2 \cdot V_{cm} = 2 \cdot (0.1\,V) - 2 \cdot (2.5\,V) = -4.8\,V$$

4. Find differential gain based on results from step 3.

$$Gain = \frac{V_{outDifMax} - V_{outDifMin}}{V_{inDifMax} - V_{inDifMin}} = \frac{(4.8\ V) - (-4.8\ V)}{(20\ V) - (-20\ V)} = 0.24$$

5. Find standard resistor values for differential gain. Use *Analog Engineer's Calculator* ("Amplifier and Comparator\Find Amplifier Gain" section) to find standard values for Rf/Rg ratio.

$$\frac{Gain_{dif}}{2} = \frac{R_f}{R_g} = \frac{0.24}{2} = 0.12$$

$$\frac{R_f}{R_g} = 0.12 = \frac{12\ k\Omega}{100\ k\Omega} = 0.12$$

6. Find Cf for cutoff frequency.

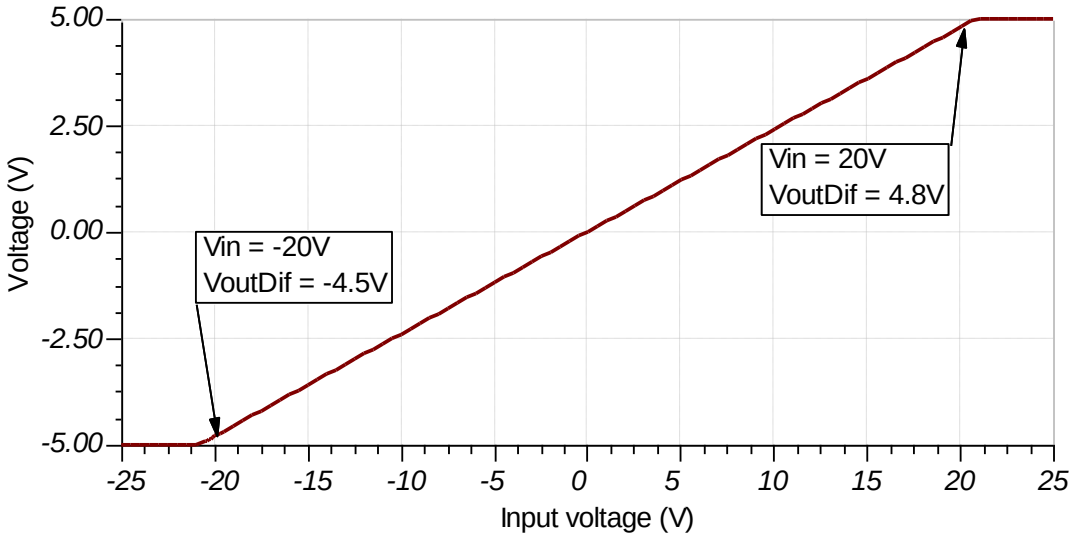
$$f = \frac{1}{2 \cdot \pi \cdot C_f \cdot R_f} = \frac{1}{2 \cdot \pi \cdot (1.3nF) \cdot (12k\Omega)} = 10.2\,kHz$$

$$C_f = \frac{1}{2 \cdot \pi \cdot f_c \cdot R_f} = \frac{1}{2 \cdot \pi \cdot (10\ kHz) \cdot (12\ k\Omega)} = 1.326 \quad nF \text{ or } 1.3\ nF \text{ for standard value}$$

$$f = \frac{1}{2 \cdot \pi \cdot C_f \cdot R_f} = \frac{1}{2 \cdot \pi \cdot (1.3nF) \cdot (12k\Omega)} = 10.2kHz$$

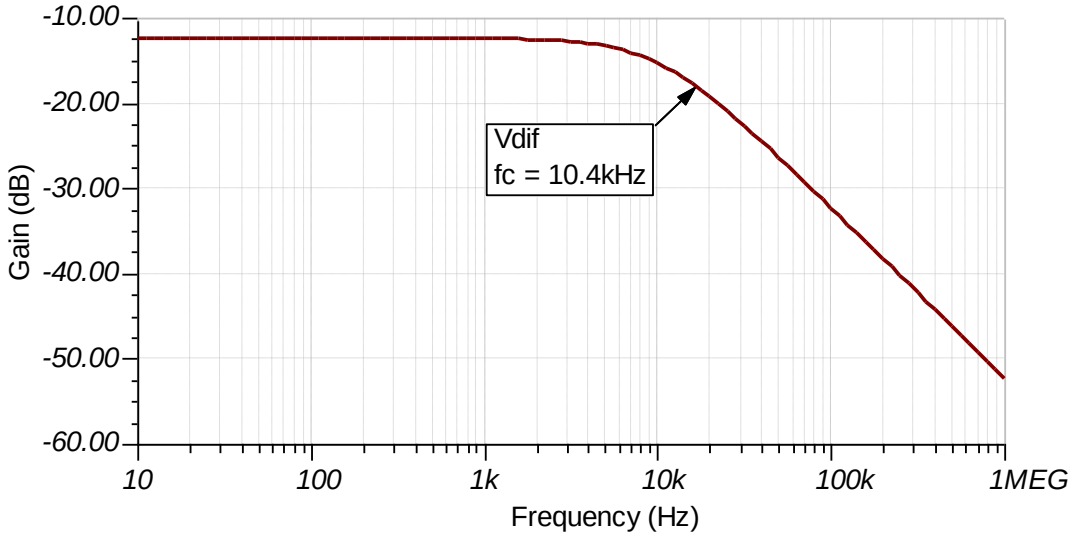
DC Transfer Characteristics

The following graph shows a linear output response for inputs from –20V to +20V. Refer to *Determining a SAR ADC's Linear Range when using Operational Amplifiers* for detailed theory on this subject.



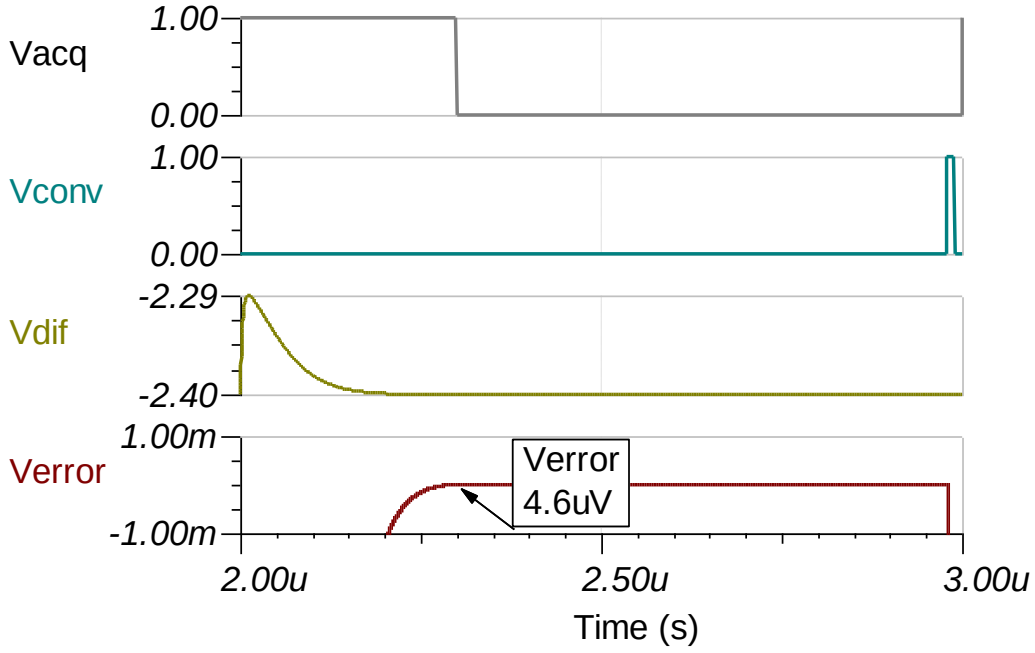
AC Transfer Characteristics

The bandwidth is simulated to be 10.4 kHz, and the gain is –12.4dB which is a linear gain of 0.12. See *Op Amps: Bandwidth 1* for more details on this subject.



Transient ADC Input Settling Simulation

The following simulation shows settling to a –20V dc input signal. This type of simulation shows that the sample and hold kickback circuit is properly selected. Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



Noise Simulation

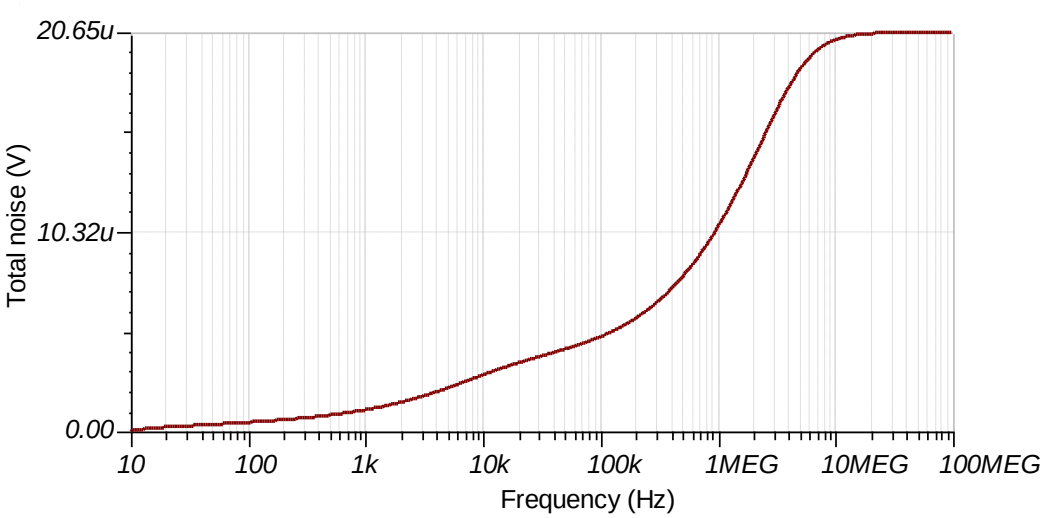
The following simplified noise calculation is provided for a rough estimate. We neglect resistor noise in this calculation as it is attenuated for frequencies greater than 10kHz.

$$f_c = \frac{1}{2 \cdot \pi \cdot R_{filt} \cdot C_{filt}} = \frac{1}{2 \cdot \pi \cdot (47.5\Omega) \cdot (1.2nF)} = 2.8MHz$$

$$E_{n\_se} = e_{n320} \cdot \sqrt{K_n \cdot f_c} = (7nV / \sqrt{Hz}) \cdot \sqrt{(1.57) \cdot (2.8MHz)} = 14.7\mu Vrms \quad \text{for a single ended input}$$

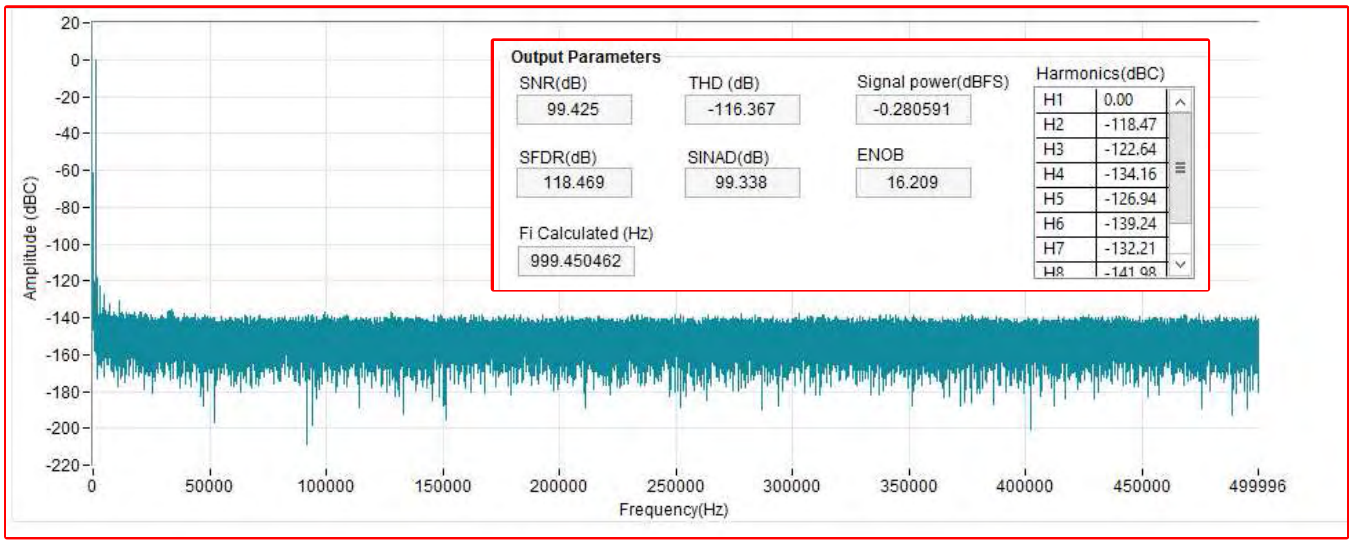
$$E_{n\_tot} = \sqrt{E_{n\_se}{}^2 + E_{n\_se}{}^2} = \sqrt{(14.7\mu V)^2 + (14.7\mu V)^2} = 20.7\mu V \quad \text{rms} \quad \text{Total noise for differential amplifier}$$

Note that calculated and simulated match well. Refer to *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Measure FFT

This performance was measured on a modified version of the ADS8910BEVM. The AC performance indicates SNR = 99.4dB, and THD = –116.4dB. See *Introduction to Frequency Domain* for more details on this subject.

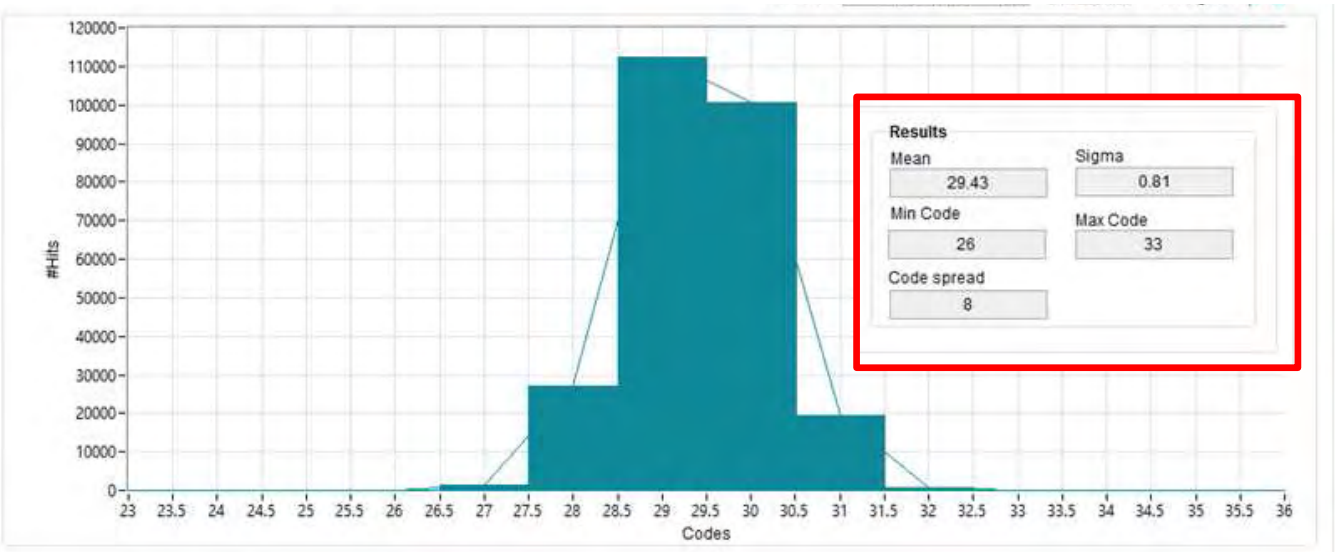


Noise Measurement

The following measured result is for both inputs connected to ground. The histogram shows the system offset and noise. The standard deviation in codes is given by the EVM GUI (0.81), and this can be used to calculate the RMS noise (30.9µV rms) as shown in the following equation.

$$LSB = \frac{FSR}{2^N} = \frac{10\ V}{2^{18}} = 38.14 \mu V$$

$$E_{n\_measured} = E_{nSigma} \cdot LSB = (0.81) \cdot (34.14\ \ \mu V) = 30.9 \mu Vrms$$



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS8900B[1]	18-bit resolution, 1-Msps sample rate, Integrated reference buffer, fully differential input, Vref input range 2.5V to 5V.	www.ti.com/product/ADS8900B	www.ti.com/adcs
OPA320[2]	20-MHz bandwidth, Rail-to-Rail with Zero Crossover Distortion, VosMax = 150 µV, VosDriftMax = 5uV/°C, en = 7nV/rtHz	www.ti.com/product/OPA320	www.ti.com/opamp
REF5050[3]	3 ppm/°C drift, 0.05% initial accuracy, 4µVpp/V noise	www.ti.com/product/REF5050	www.ti.com/vref

(1) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR ADC applications. The OPA320 is also commonly used in 1Msps SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling. Furthermore, the zero crossover distortion rail-to-rail input allows for linear swing across most of the ADC input range.

(2) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR ADC applications. The OPA320 is also commonly used in 1Msps SAR applications as it has sufficient bandwidth.

(3) The REF5050 can be directly connected to the ADS8910B without any buffer because the ADS8910B has a built in internal reference buffer. Also, the REF5050 has the required low noise and drift for precision SAR ADC applications. The OPA320 is also commonly used in 1Msps SAR applications as it has sufficient bandwidth.

Link to Key Files for High Voltage Battery Monitor

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Design files for this circuit – http://www.ti.com/lit/zip/sbac171.

Revision History

Revision	Date	Change
A	January 2019	Downstyle title, update title role content, added link to circuit cookbook library page.

Single-ended to differential signal conversion using an op amp and FDA for unipolar signals

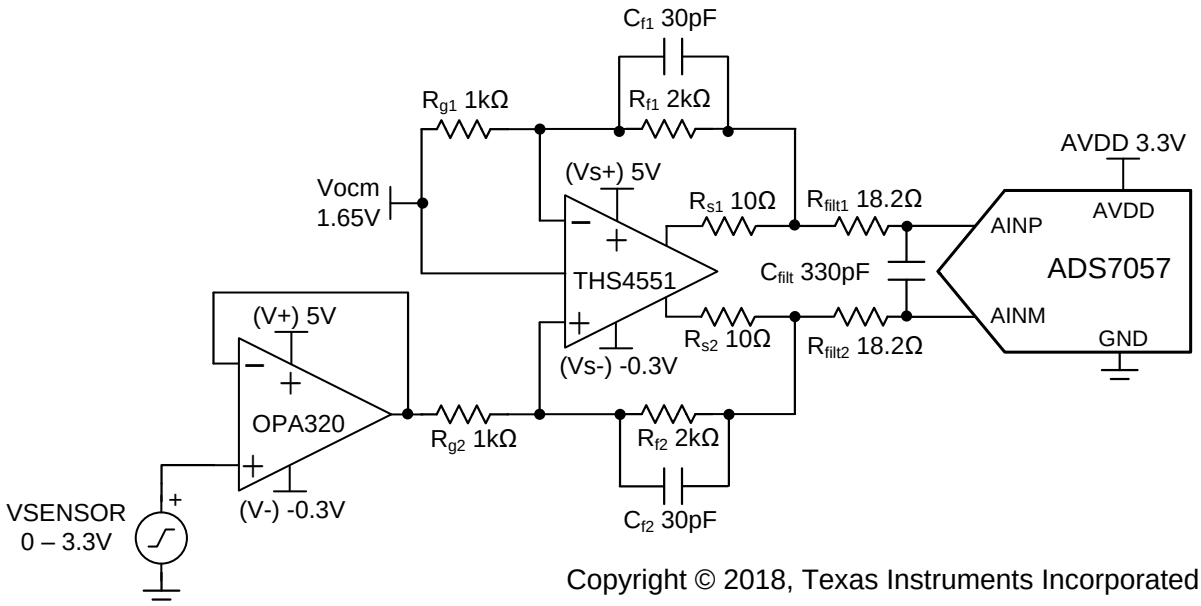
Evan Sawyer

Input	ADC Input	Digital Output ADS7057
V_{in} Min = –3.3V	AINP = 0V AINM = 3.3V	2000_H 8192_{10}
V_{in} Max = 3.3V	AINP = 3.3V AINM = 0V	$1FFF_H$ 8191_{10}

Power Supplies		
AVDD	**GND**	**DVDD**
3.3V	0V	1.8V

Design Description

This design is intended to demonstrate how to convert a unipolar, single-ended signal into a unipolar, fully-differential signal and drive a differential ADC (for more information on these and other signal types, please refer to the *TI Precision Labs* training titled *SAR ADC Input Types*). Compared to a single-ended device, a fully-differential ADC has twice the dynamic range which improves the AC performance of the converter. Many common systems, for example *Sonar Receivers*, *Flow Meters*, and *Motor Controls*, benefit from the higher performance of a differential ADC. The equations and explanation of component selection in this design can be customized based on system specifications and needs. For more information on a similar design using a bipolar input, see the cookbook circuit titled *Single-Ended to Differential Using an Op Amp and FDA for Bipolar Signals*.



Specifications

Specification	Calculated	Simulated
Transient ADC Input Settling (at 250ksps)	< 0.5 · LSB = 201µV	144.8µV
Conditioned Signal Range (at 250ksps)	> 99% ADC FSR = > 6.53V	6.60V
Noise	43.8µV / √Hz	44.3µV / √Hz

Design Notes

1. The ADS7057 was selected because of its throughput (2.5Msps), size (2.25mm²), and low-latency (successive approximation register, or SAR, architecture).
2. Determine the linear range of the fully-differential amplifier (ADC driver) based on common mode, output swing, and linear open-loop gain specification. This is covered in the *component selection* section.
3. Determine the linear range of the op amp (signal conditioning) based on common mode, output swing, and linear open-loop gain specification. This is covered in the *component selection* section.
4. Select COG (NPO) capacitors for C_{filt}, to minimize distortion.
5. For best performance, consider using a 0.1% 20ppm/°C film resistor, or better, to minimize distortion.
6. The *TI Precision Labs - ADCs* training video series covers methods for selecting the charge bucket circuit R_{filtx} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If you modify the design you will need to select a different RC filter. Refer to *Introduction to SAR ADC Front-end Component Selection* (a *TI Precision Labs* training video) for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

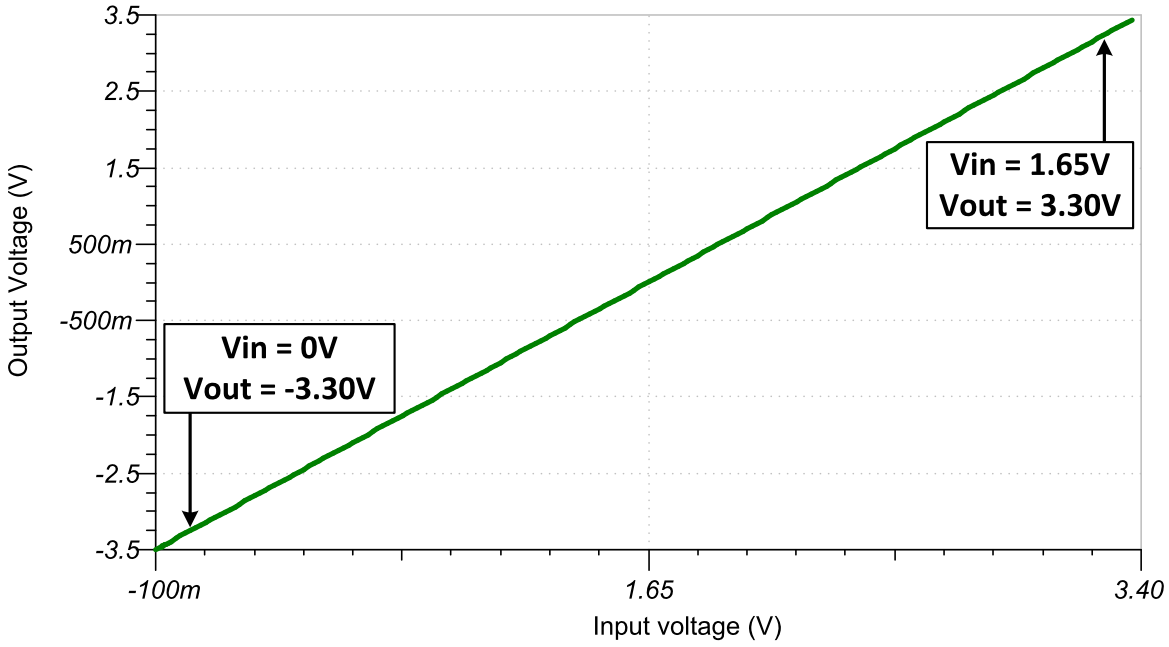
1. Select a fully-differential amplifier capable of driving the ADC:
   THS4551 – Low noise, precision, 150MHz, fully-differential amplifier
   - Wide input common-mode voltage:
     $$V_{s-} - 0.1V < V_{cm} < V_{s+} - 1.3V$$
   - Linear output (requirement: 0V to 3.3V at each output):
     $$V_{s-} + 0.22V < V_{out} < V_{s+} - 0.22V$$
2. Select a wide bandwidth operational amplifier:
   OPA320 – Precision, zero-crossover, 20MHz, RRIO, operational amplifier
   - Gain bandwidth product >12.5MHz (>5 times the sampling rate)
   - Input common-mode voltage (requirement: 0 - 3.3V):
     $$V_{-} - 0.1V < V_{cm} < V_{+} + 0.1V$$
   - Linear output:
     $$V_{-} + 0.03V < V_{out} < V_{+} - 0.03V$$
     $$V_{-} + 0.2V < V_{out} < V_{+} - 0.2V$$
   - Combined worst-case linear range (calculated from supplies used with OPA320):
     $$-0.1V < V_{out} < 4.8V$$

NOTE: The operational amplifier is used to protect the sensor from any charge kickbacks that occur when the ADC connects or disconnects the sampling capacitor. This amplifier may not be needed if the sensor has a high-output impedance. A negative rail is used for both the OPA320 and THS4551 based on the assumption that the sensor is operating with a negative rail. This also ensures the highest performance from the ADC by providing the full scale input range.

3. Select R_{fx} and R_{gx}
   - The combination of R_{fx} and R_{gx} sets the gain of the system. With an input range of 0V - 3.3V and an ADC full scale of ±3.3V, a gain of 2 was selected for this system.
   - The values of R_{fx} = 2k and R_{gx} = 1k were selected to both provide the desired gain as well as limit the current through the feedback network, thus minimizing power consumption of the system.
4. Select R_{sx}
   - It is important to connect small resistors at the output of the amplifier, in this case 10Ω, to flatten the output impedance and improve stability of the system.
5. Select R_{filtx} and C_{filt} values for settling of 250-kHz input signal and sample rate of 2.5Msps:
   - *Refine the R_{filt} and C_{filt} Values* is a Precision Labs Video showing the methodology for selecting R_{filtx} and C_{filt}. The final value of 18.2Ω and 330pF proved to settle to well below ½ of a least significant bit (LSB) within the acquisition window.

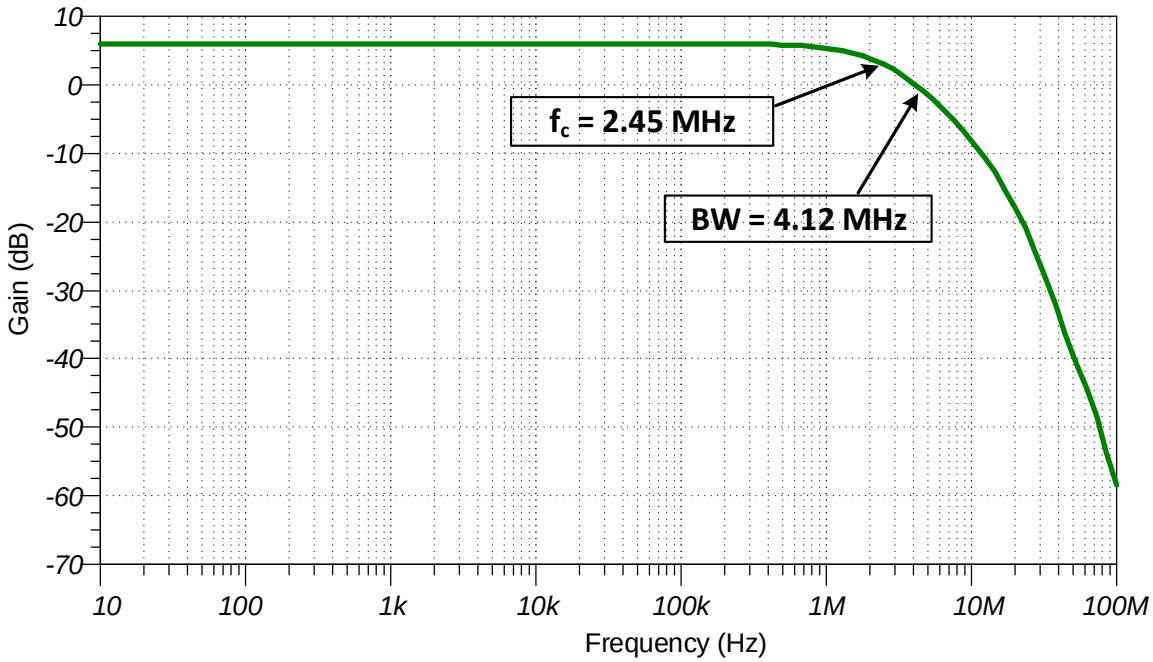
DC Transfer Characteristics

The following graph shows the simulated output for a 0 - 3.3V input. The analog front end has a linear output of ±3.3V which matches the full-scale range (FSR) of the ADC (with AVDD = 3.3V).



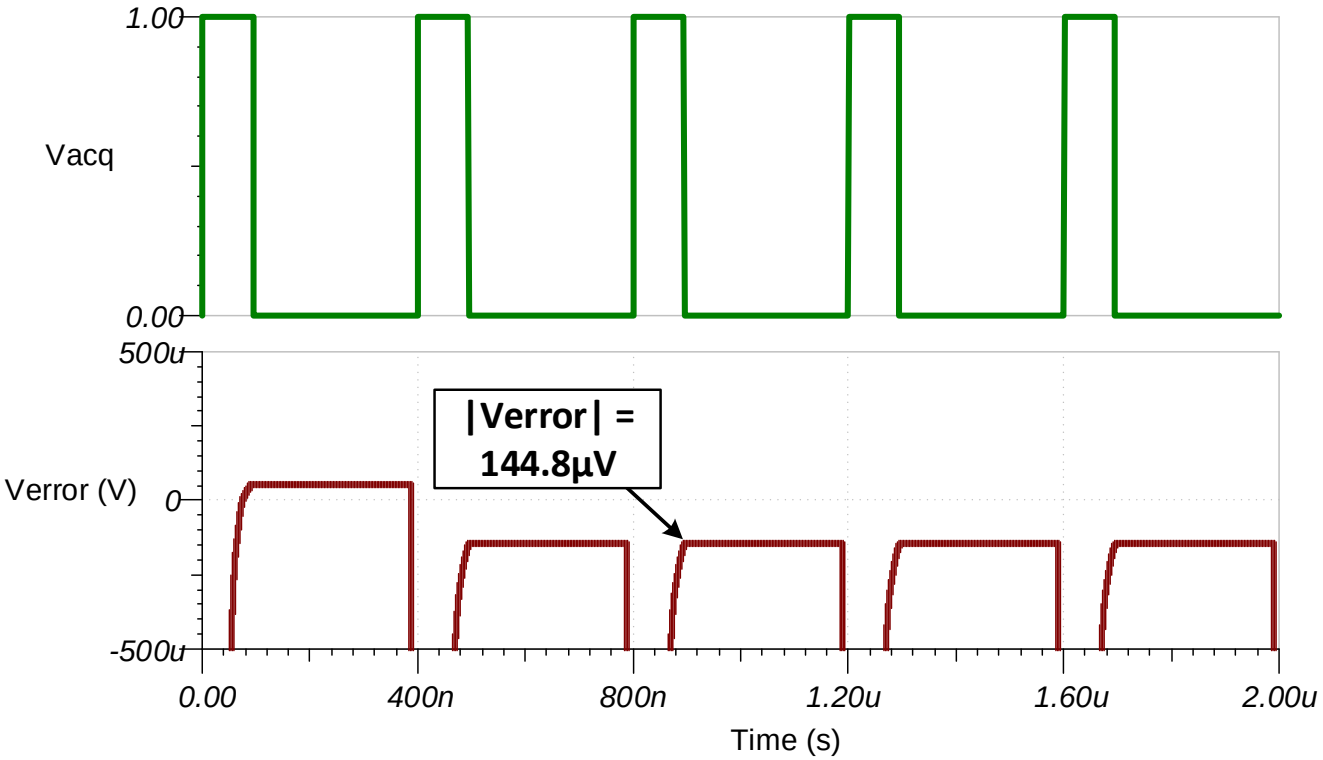
AC Transfer Characteristics

The bandwidth of the analog front end is simulated to be 4.12MHz at the gain of 0dB which is a linear gain of 1. This bandwidth will allow the inputs of the ADC to adequately settle for a 250-ksps input signal.



Transient ADC Input Settling Simulation

The following simulation shows the ADC sample and hold capacitor settling for a 3.3-V DC input signal. This simulation shows that the analog front end is able to drive the ADC with a large step input (from 0V to 3.3V) so it settles to within ½ of an LSB (approximately 200µV) in the allotted acquisition time (95ns). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject, and follow the link at the end of this design to download these simulation files.



Noise Simulation

This section walks through a simplified noise calculation, providing a rough estimate to compare with the simulated result. The resistor noise is included in this calculation as it is a significant portion of the overall noise of the system. Note that the resistor noise can be reduced by using smaller value resistors, but at the expense of increased power consumption through the feedback network.

$$F_C = \frac{1}{2 \times \pi \times R_{filt} \times C_{filt}} = \frac{1}{2 \times \pi \times 2\,K\Omega \times 30PF} = 2.65MHz$$

$$E_N = E_{OPA320} \times \sqrt{2 \times K_N \times F_C} = \left(7nV/\sqrt{Hz}\right) \times \sqrt{2 \times 1.57 \times 2.65MHz} = 20.2\mu V/\sqrt{Hz}$$

$$E_{n\_OPA320} = E_N \times Gain = 20.2\mu V/\sqrt{Hz} \times 2 = 40.4\mu V/\sqrt{Hz}$$

$$E_{n\_THS4551} = E_{NTHS4551} \times \sqrt{2 \times K_N \times F_C} = \left(3.8nV/\sqrt{Hz}\right) \times \sqrt{2 \times 157 \times 2.65MHz} = 9.52\mu V/\sqrt{Hz}$$

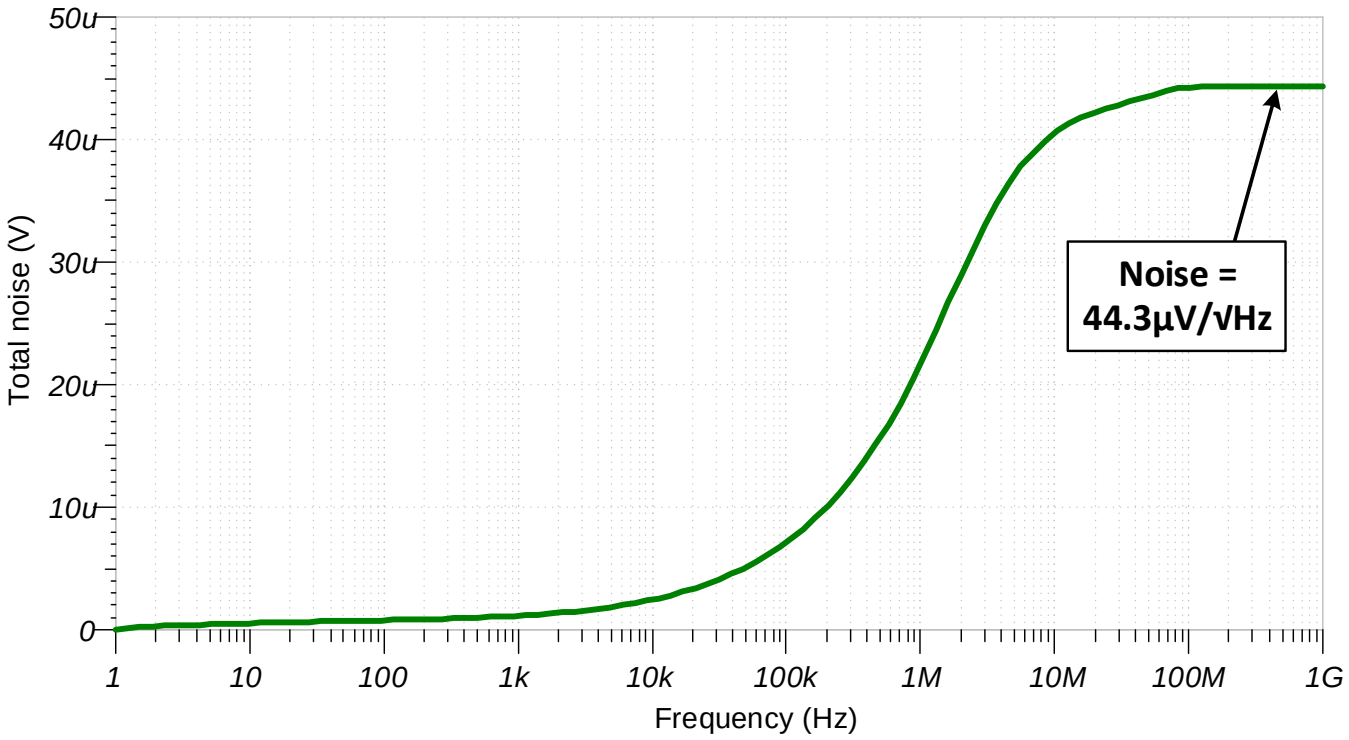
$$E_{Rg} = \frac{\sqrt{4 \times K \times T \times R_G}}{1 \times 10^{-9}} \times \frac{R_F}{R_G} \times \sqrt{2} = \frac{\sqrt{4 \times 1.38 \times 10^{-23} \times (273.15 + 25) \times 1000}}{1 \times 10^{-9}} \times \frac{2000}{1000} \times \sqrt{2} = 11.47\mu V/\sqrt{Hz}$$

$$E_{Rf} = \frac{\sqrt{4 \times K \times T \times R_F}}{1 \times 10^{-9}} \times \sqrt{2} = \frac{\sqrt{4 \times 1.38 \times 10^{-23} \times (273.15 + 25) \times 2000}}{1 \times 10^{-9}} \times \sqrt{2} = 8.11\mu V/\sqrt{Hz}$$

TOTAL NOISE AT OUTPUT EQUATION:

$$E_N = \sqrt{E_{nOPA320}^2 + E_{n\_THS4551}^2 + E_{Rg}^2 + E_{Rf}^2} = \sqrt{40.4^2 + 9.52^2 + 11.47^2 + 8.11^2} = 43.8\mu V/\sqrt{Hz}$$

Note that calculated and simulated match well. Refer to the *TI Precision Labs - ADCs* training video series for detailed theory on this subject.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS7057	*14 bit, 2.5 Msps, fully-differential input, SPI, 2.25mm^2 package*	www.ti.com/product/ADS7057	www.ti.com/adcs
THS4551	*150MHz, 3.3nV/√Hz input voltage noise, fully-differential amplifier*	www.ti.com/product/THS4551	www.ti.com/opamp
OPA320	*Precision, zero-crossover, 20MHz, 0.9pA Ib, RRIO, operational amplifier*	www.ti.com/product/OPA320	www.ti.com/opamp

NOTE: The ADS7057 uses the AVDD as the reference input. A high-PSRR LDO, such as the TPS7A47, should be used as the power supply.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key files (TINA):

Design files for this circuit – http://www.ti.com/lit/zip/sbac188.

Link to Related Cookbooks:

Single-Ended to Differential Signal Conversion for Bipolar Input

Revision History

Revision	Date	Change
A	March 2019	Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page.

Single-ended-to-differential circuit using an op amp and fully differential amplifier (FDA) for bipolar signals

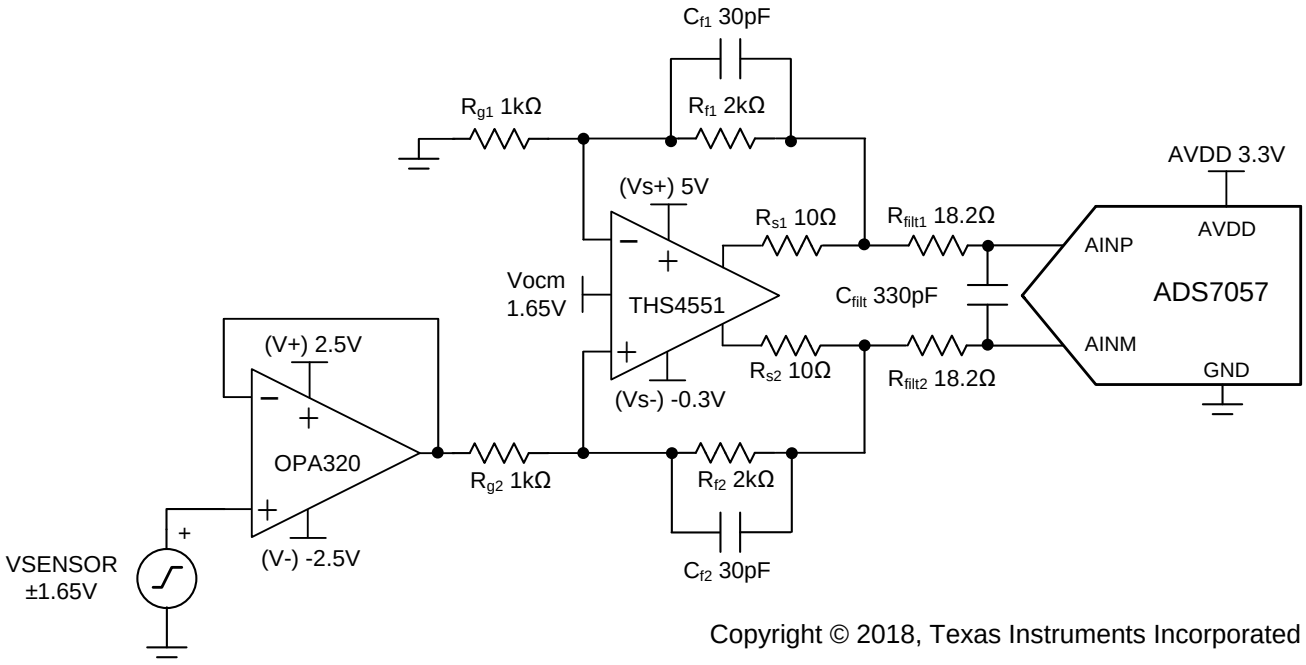
Evan Sawyer

Input	ADC Input	Digital Output ADS7057
V_{in} Min = –3.3V	AINP = 0V AINM = 3.3V	2000_H 8192_{10}
V_{in} Max = 3.3V	AINP = 3.3V AINM = 0V	$1FFF_H$ 8191_{10}

Power Supplies		
AVDD	**GND**	**DVDD**
3.3V	0V	1.8V

Design Description

This design is intended to demonstrate how to convert a bipolar, single-ended signal into a unipolar, fully-differential signal and drive a differential ADC (for more information on these and other signal types, please refer to the *TI Precision Labs* training titled *SAR ADC Input Types*). Compared to a single-ended device, a fully-differential ADC has twice the dynamic range which improves the AC performance of the converter. Many common systems, for example *Sonar Receivers*, *Flow Meters*, and *Motor Controls*, benefit from the higher performance of a differential ADC. The equations and explanation of component selection in this design can be customized based on system specifications and needs. For more information on a similar design using a unipolar input signal, see the cookbook circuit titled *Single-Ended to Differential Signal Conversion for Unipolar Inputs*.



Specifications

Specification	Calculated	Simulated
Transient ADC Input Settling (at 250ksps)	< 0.5 · LSB = 201µV	134.7µV
Conditioned Signal Range (at 250ksps)	> 99% ADC FSR = > 6.53V	6.60V
Noise	43.8µV / √Hz	44.3µV / √Hz

Design Notes

1. The ADS7057 was selected because of its throughput (2.5Msps), size (2.25mm²) and low-latency (successive approximation register, or SAR, architecture).
2. Determine the linear range of the fully-differential amplifier (ADC driver) based on common mode, output swing, and linear open-loop gain specification. This is covered in the component selection section.
3. Determine the linear range of the op amp (signal conditioning) based on common mode, output swing, and linear open-loop gain specification. This is covered in the component selection section.
4. Select COG (NPO) capacitors for C_{filt}, to minimize distortion.
5. For best performance, consider using a 0.1% 20ppm/°C film resistor, or better, to minimize distortion.
6. The *TI Precision Labs - ADCs* training video series covers methods for selecting the charge bucket circuit R_{filtx} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected. Refer to *Introduction to SAR ADC Front-end Component Selection* (a *TI Precision Labs* training video) for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

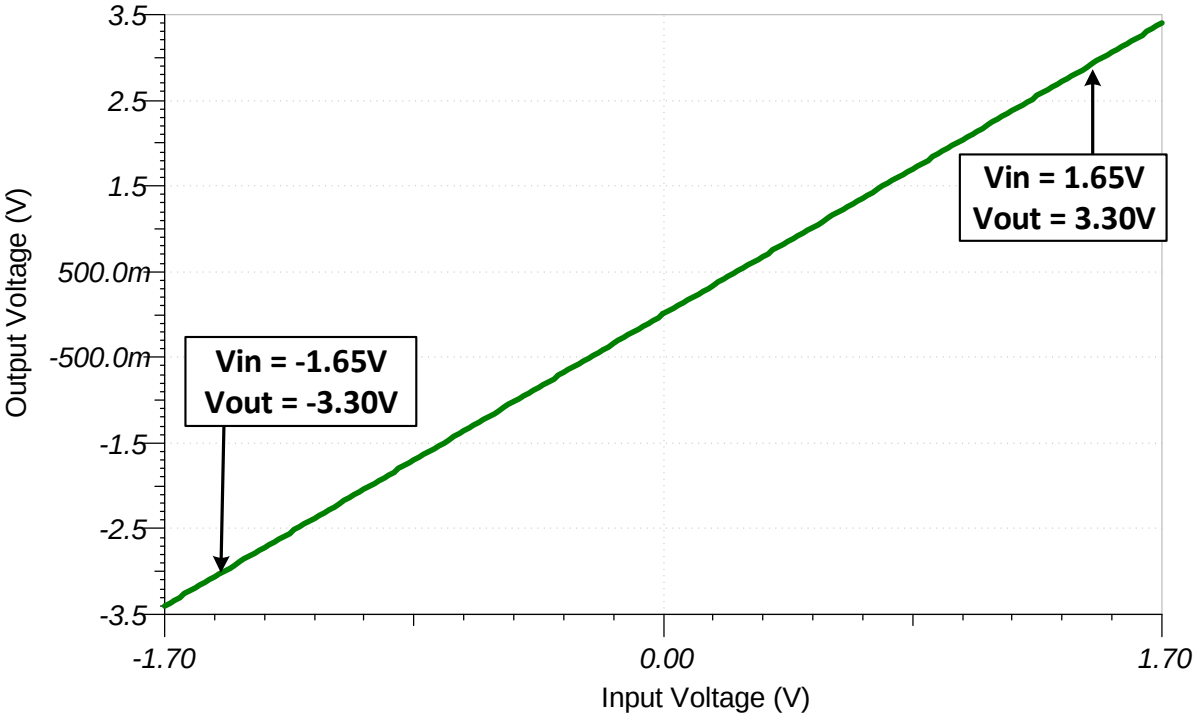
1. Select a fully-differential amplifier capable of driving the ADC:
   THS4551 – Low noise, precision, 150MHz, fully-differential amplifier
   - Wide input common-mode voltage:
     $$V_{s-} - 0.1V < V_{cm} < V_{s+} - 1.3V$$
   - Linear output (requirement: 0V to 3.3V at each output):
     $$V_{s-} + 0.22V < V_{out} < V_{s+} - 0.22V$$
2. Select a wide bandwidth operational amplifier:
   OPA320 – Precision, zero-crossover, 20MHz, RRIO, operational amplifier
   - Gain bandwidth product > 12.5MHz (> 5 times the sampling rate)
   - Input common-mode voltage (requirement: ±1.65V):
     $$V_{-} - 0.1V < V_{cm} < V_{+} + 0.1V$$
   - Linear output:
     $$V_{-} + 0.03V < V_{out} < V_{+} - 0.03V$$
     $$V_{-} + 0.2V < V_{out} < V_{+} - 0.2V$$
   - Combined worst-case linear range (calculated from supplies used with OPA320):
     $$-2.3V < V_{out} < 2.3V$$

NOTE: The operational amplifier is used to protect the sensor from any charge kickbacks that occur when the ADC connects or disconnects the sampling capacitor. This amplifier may not be needed if the sensor has a high output impedance. A negative rail is used for both the OPA320 and THS4551 based on the assumption that the sensor is operating with a negative rail. This also ensures the highest performance from the ADC by providing the full scale input range.

3. Select R_{fx} and R_{gx}
   - The combination of R_{fx} and R_{gx} sets the gain of the system. With an input range of ±1.65V and an ADC full scale of ±3.3V, a gain of 2 was selected for this system.
   - The values of R_{fx} = 2k and R_{gx} = 1k were selected to both provide the desired gain as well as limit the current through the feedback network, thus minimizing power consumption of the system.
4. Select R_{sx}
   - It is important to connect small resistors at the output of the amplifier, in this case 10Ω, to flatten the output impedance and improve stability of the system.
5. Select R_{filtx} and C_{filt} values for settling of 250-kHz input signal and sample rate of 2.5Msps:
   - *Refine the R_{filt} and C_{filt} Values* is a *TI Precision Labs* video showing the methodology for selecting R_{filtx} and C_{filt}. The final value of 18.2Ω and 330pF proved to settle to well below ½ of a least significant bit (LSB) within the acquisition window.

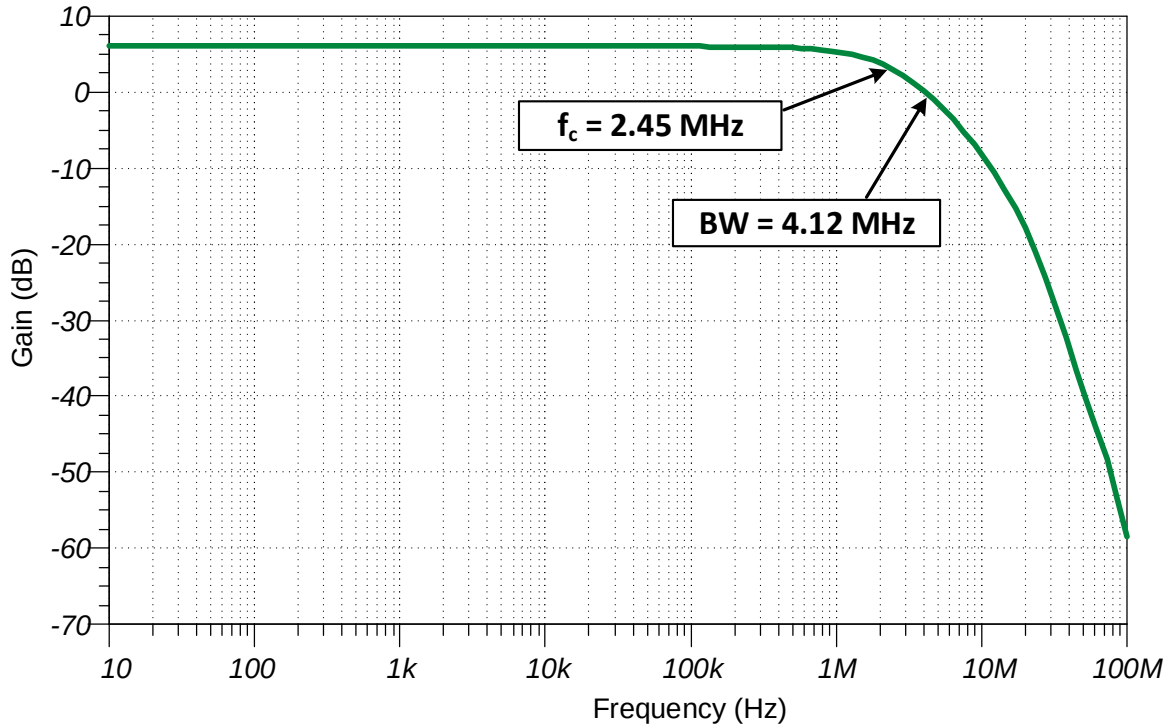
DC Transfer Characteristics

The following graph shows the simulated output for a ±1.65-V input. The analog front end has a linear output of ±3.3V which matches the full-scale range (FSR) of the ADC (with AVDD = 3.3V).



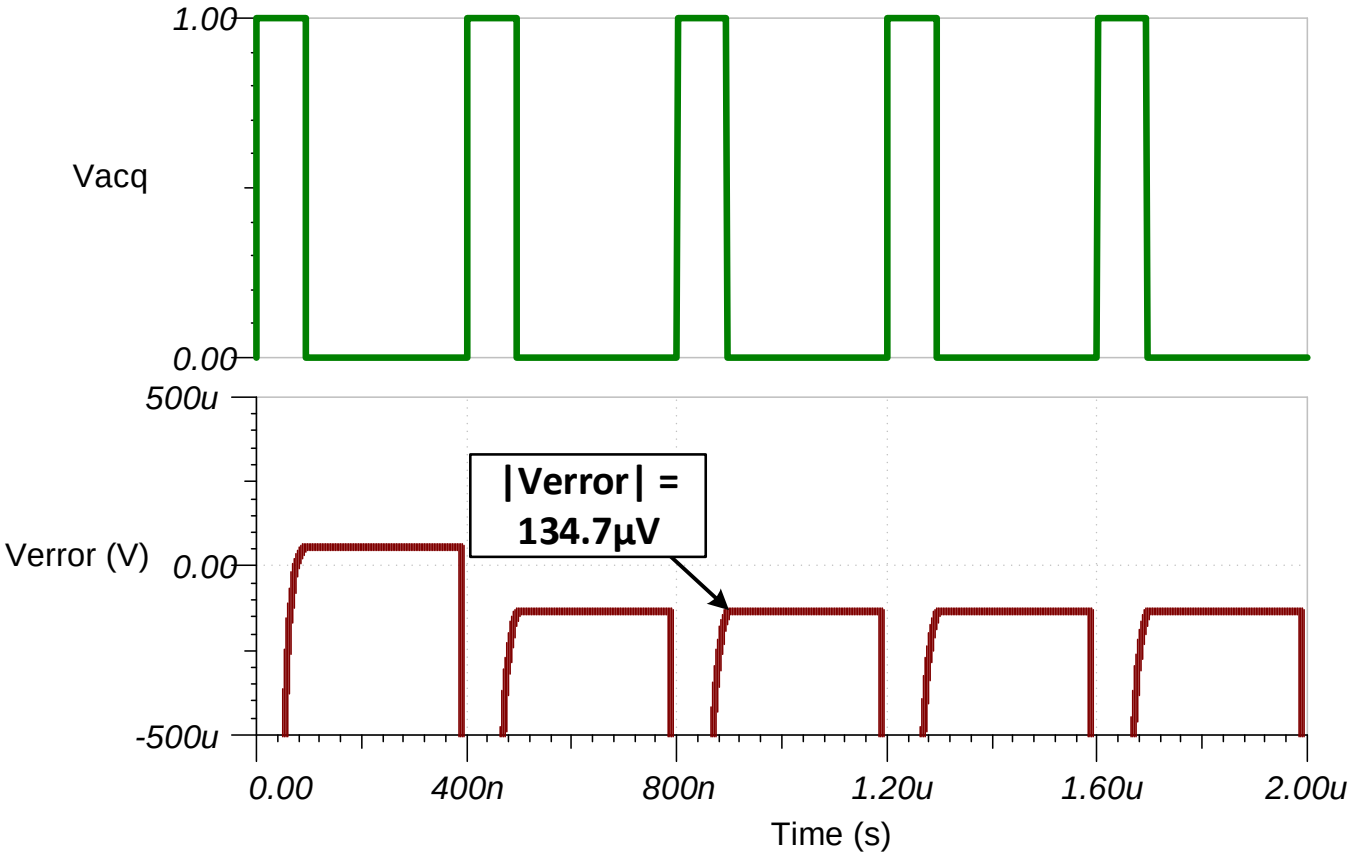
AC Transfer Characteristics

The bandwidth of the analog front end is simulated to be 4.12MHz at the gain of 0dB which is a linear gain of 1. This bandwidth will allow the inputs of the ADC to adequately settle for a 250-ksps input signal.



Transient ADC Input Settling Simulation

The following simulation shows the ADC sample and hold capacitor settling for a 3.3-V DC input signal. This simulation shows that the analog front end is able to drive the ADC with a large step input (from 0V to 3.3V) so it settles to within ½ of an LSB (approximately 200µV) in the allotted acquisition time (95ns). Refer to *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject, and follow the link at the end of this design to download these simulation files.



Noise Simulation

This section walks through a simplified noise calculation, providing a rough estimate to compare with the simulated result. The resistor noise is included in this calculation as it is a significant portion of the overall noise of the system. Note that the resistor noise can be reduced by using smaller value resistors, but at the expense of increased power consumption through the feedback network.

$$F_C = \frac{1}{2 \times \pi \times R_{filt} \times C_{filt}} = \frac{1}{2 \times \pi \times 2\,K\Omega \times 30\,PF} = 2.65\,MHz$$

$$E_N = E_{OPA320} \times \sqrt{2 \times K_N \times F_C} = \left(7\,nV/\sqrt{Hz}\right) \times \sqrt{2 \times 1.57 \times 2.65\,MHz} = 20.2\,\mu V/\sqrt{Hz}$$

$$E_{n\_OPA320} = E_N \times Gain = 20.2\,\mu V/\sqrt{Hz} \times 2 = 40.4\,\mu V/\sqrt{Hz}$$

$$E_{n\_THS4551} = E_{NTHS4551} \times \sqrt{2 \times K_N \times F_C} = \left(3.3\,nV/\sqrt{Hz}\right) \times \sqrt{2 \times 1.57 \times 2.65\,MHz} = 9.52\,\mu V/\sqrt{Hz}$$

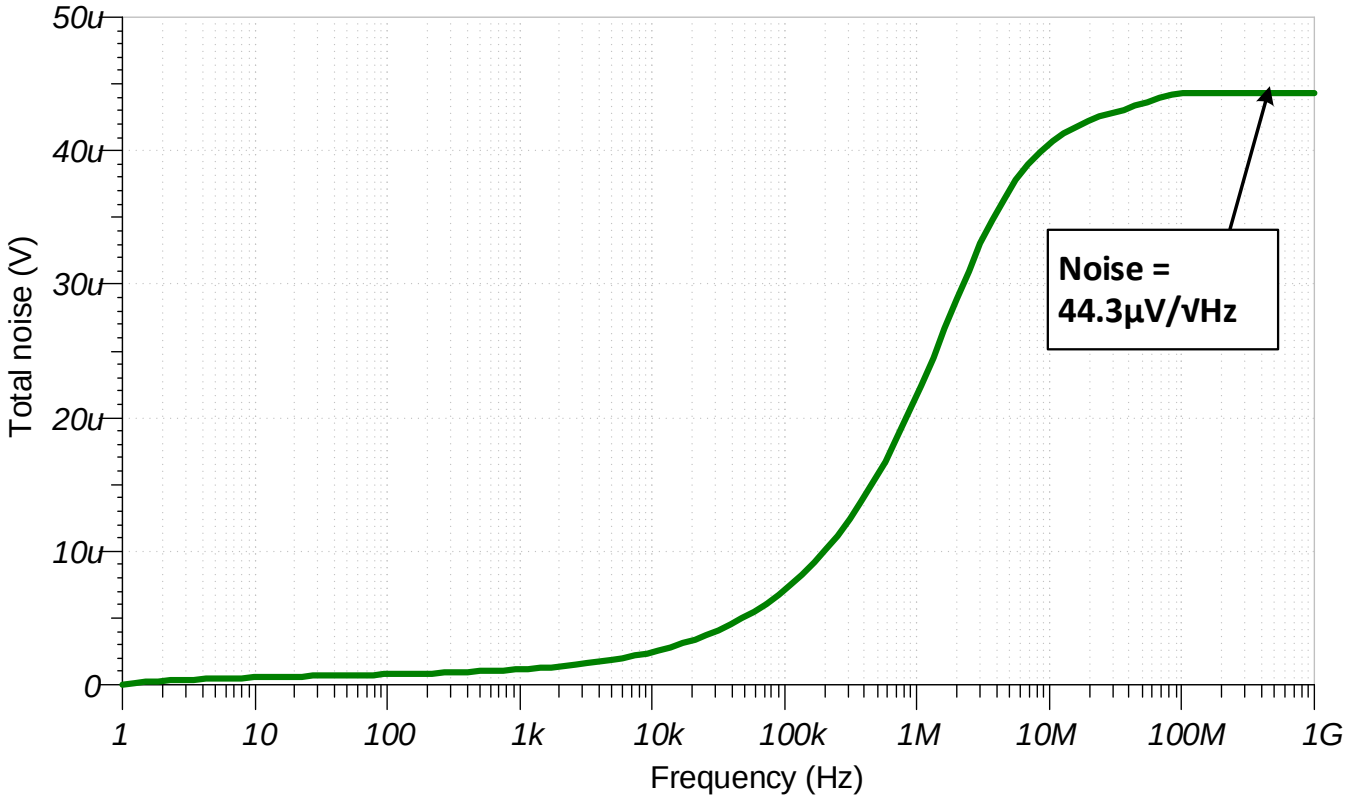
$$E_{Rg} = \frac{\sqrt{4 \times K \times T \times R_G}}{1 \times 10^{-9}} \times \frac{R_F}{R_G} \times \sqrt{2} = \frac{\sqrt{4 \times 1.38 \times 10^{-23} \times (273.15 + 25) \times 1000}}{1 \times 10^{-9}} \times \frac{2000}{1000} \times \sqrt{2} = 11.47\,\mu V/\sqrt{Hz}$$

$$E_{Rf} = \frac{\sqrt{4 \times K \times T \times R_F}}{1 \times 10^{-9}} \times \sqrt{2} = \frac{\sqrt{4 \times 1.38 \times 10^{-23} \times (273.15 + 25) \times 2000}}{1 \times 10^{-9}} \times \sqrt{2} = 8.11\,\mu V/\sqrt{Hz}$$

TOTAL NOISE AT OUTPUT EQUATION:

$$E_N = \sqrt{E_{nOPA320}^{\ 2} + E_{n\_THS4551}^{\ 2} + E_{Rg}^{\ 2} + E_{Rf}^{\ 2}} = \sqrt{40.4^2 + 9.52^2 + 11.47^2 + 8.11^2} = 43.8\,\mu V/\sqrt{Hz}$$

Note that calculated and simulated match well. Refer to the *TI Precision Labs - ADCs* training video series for detailed theory on this subject.



Design Featured Devices

Device	Key Features	Link	Similar Devices
ADS7057	*14 bit, 2.5 Msps, fully-differential input, SPI, 2.25mm^2 package*	www.ti.com/product/ADS7057	www.ti.com/adcs
THS4551	*150-MHz, 3.3-nV/√Hz input voltage noise, fully-differential amplifier*	www.ti.com/product/THS4551	www.ti.com/opamp
OPA320	*Precision, zero-crossover, 20-MHz, 0.9-pA Ib, RRIO, operational amplifier*	www.ti.com/product/OPA320	www.ti.com/opamp

NOTE: The ADS7057 uses the AVDD as the reference input. Use a high-PSRR LDO, such as the TPS7A47, as the power supply.

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to key files (TINA):

Design files for this circuit – http://www.ti.com/lit/zip/sbac181.

Link to Related Cookbooks

Single-Ended to Differential Signal Conversion for Unipolar Input

Revision History

Revision	Date	Change
A	March 2019	Downstyle the title and changed title role to 'Data Converters'. Added link to circuit cookbook landing page.

Single-ended to differential using a two op-amp circuit

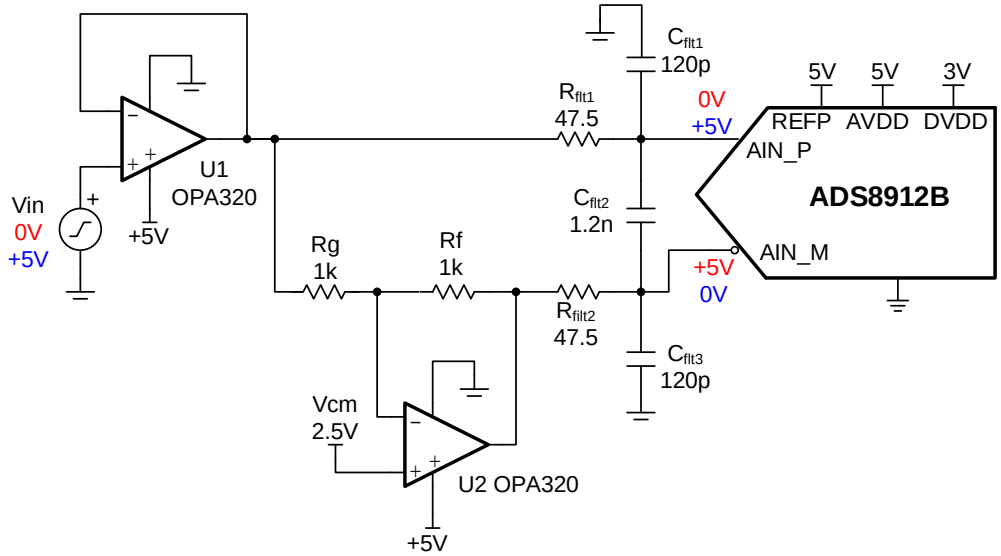
Bryan McKay, Art Kay

Input	ADC Differential Input (Vdif)	ADC Common-Mode Input (Vcm)	Digital Output ADS9110
0V	–5V	2.5V	20000_H
5V	+5V	2.5V	$1FFFF_H$

Power Supplies			
V+ (op amp)	**AVDD**	**DVDD**	**REFP**
5V	5V	3V	5V

Design Description

This circuit uses two OPA320 op amps to perform a single-ended to differential conversion for driving the ADS8912B fully-differential ADC. Another approach to solve this problem uses a fully-differential amplifier (FDA). See *Single-Ended to Differential Conversion Using an Op Amp and FDA for Unipolar Signals* for the FDA example. Since there are many thousands of different types of op amps available, finding an op amp the meets your specific requirements may be easer than finding an fully-differential amplifier. Most FDAs, for example, do not have as good swing to the rail, offset, bias current, and drift as many precision op amps have. On the other hand, the op-amp approach has an asymmetrical group delay in the inverting and non-inverting paths. Furthermore, FDA amplifiers often have better distortion and ADC drive characteristics. In general, the FDA approach will achieve best SNR and THD, and the op-amp approach will achieve best DC characteristics. Nevertheless, the specific op amp or FDA will impact the comparison of the two typologies.



Specifications

Specification	Goal	Calculated	Simulated
Transient ADC Input Settling (1MSPS)	< 0.5LSB = 19.1µV	NA	5µV
Input Output Range	NA	NA	$0.1 < V_{IN} < 4.9V$ $–4.8V < V_{OUT} < 4.8V$
Noise	NA	$30.5µV_{RMS}$	$28.4µV_{RMS}$

Design Notes

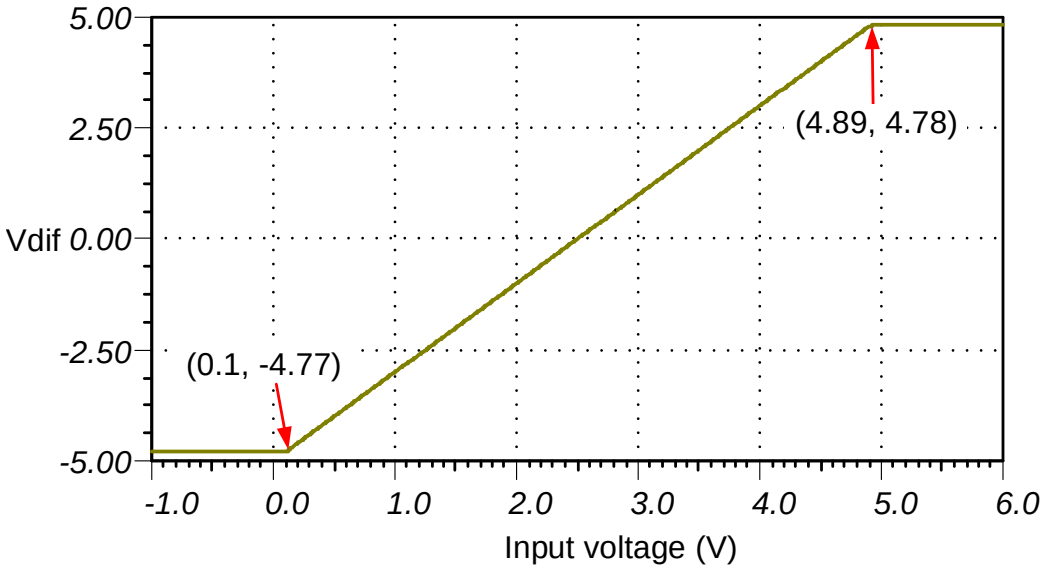
1. Use 0.1% resistors for R1 and Rg to minimize gain error and drift on U2.
2. Select COG (NPO) capacitors for C_{filt1}, C_{filt2}, and C_{filt3} to minimize distortion.
3. The *TI Precision Labs – ADCs*training video series covers methods for selecting the charge bucket circuit R_{filt} and C_{filt}. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If you modify this design you will need to select a different RC filter. See the *Introduction to SAR ADC Front-End Component Selection* training video for an explanation of how to select the RC filter for best settling and AC performance.

Component Selection

1. Select an op amp to meet the system requirements. Key specifications to consider follow:
   - Swing to rail - For 5-V supply rails it is common to use a rail-to-rail zero crossover distortion device (for example, OPA320, OPA325, and OPA365).
   - Offset voltage and Drift - One of the advantages of this circuit over the FDA approach is that some op-amps can have very good DC performance.
   - Bandwidth and quiescent current - Another advantage of this circuit over the FDA approach is that a wide range of op-amp bandwidth and related quiescent currents are available. For lower sampling rate a low bandwidth low current op amp may be a good choice.
2. Choose Rg and Rf to minimize noise. The gain of this circuit is always 1, so Rg = Rf. The main consideration here is to minimize noise while keeping the load resistance reasonable. Set the resistor noise to be roughly ⅓ of the amplifier noise. In this example Rf = Rg = 1kΩ gives a noise of 2.8nV/$\sqrt{\text{Hz}}$ which is approximately ⅓ of the 7nV/$\sqrt{\text{Hz}}$ op-amp noise. Also, the maximum load current is 2.5mA (5V / 2kΩ = 2.5mA) which is low compared to the op-amp short-circuit limit (65mA).
3. Find R_{filt} and C_{filt} to allow for settling at 1kSPS. See *Refine the Rfilt and Cfilt Values* for the algorithm to select R_{filt} and C_{filt}. The final value of 200kΩ and 510pF proved to settle to well below ½ of a least significant bit (LSB).

DC Transfer Characteristics

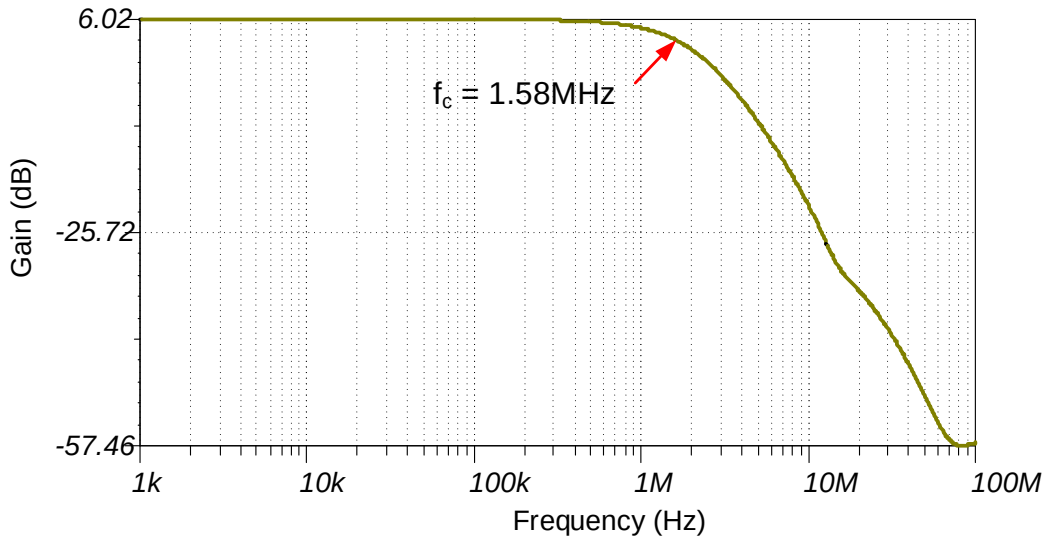
The following graph shows the DC transfer characteristics for this circuit (0-V to 5-V single-ended input, –5-V to +5-V fully-differential output). Note that the linear range is limited to about 0.1V from both supply rails (Vin linear range approximately 0.1V to 4.9V). The limitation is from the amplifier output swing limit. For improved linear swing the negative and positive supply on the amplifiers would need to be adjusted. See *Low-Power Sensor Measurements: 3.3-V, 1-ksps, 12-bit, Single-Ended, Dual-Supply Circuit* for an example on how to do this.



AC Transfer Characteristics

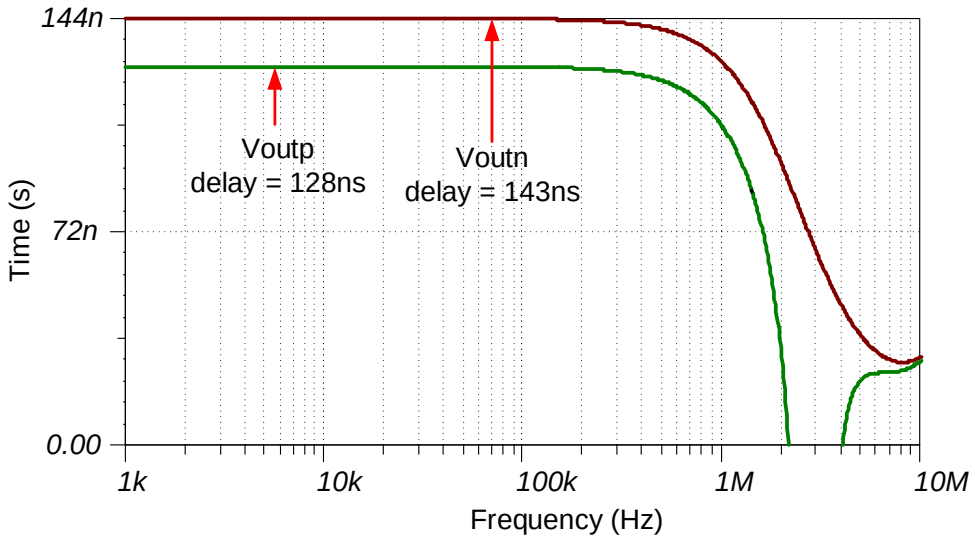
In this case the bandwidth limitation is primary set by the R_{filt}, C_{filt} values. The amplifier closed loop bandwidth can also impact the overall bandwidth. Note the bandwidth of U2 is half the bandwidth of U1 as its noise gain is two (BW_{U2} = GBW/G_n = 20MHz/2 = 10MHz).

$$f_c = \frac{1}{2\pi R \cdot C} = \frac{1}{2\pi(2 \cdot 47.5\Omega) \cdot 1.2nF} = 1.4MHz$$



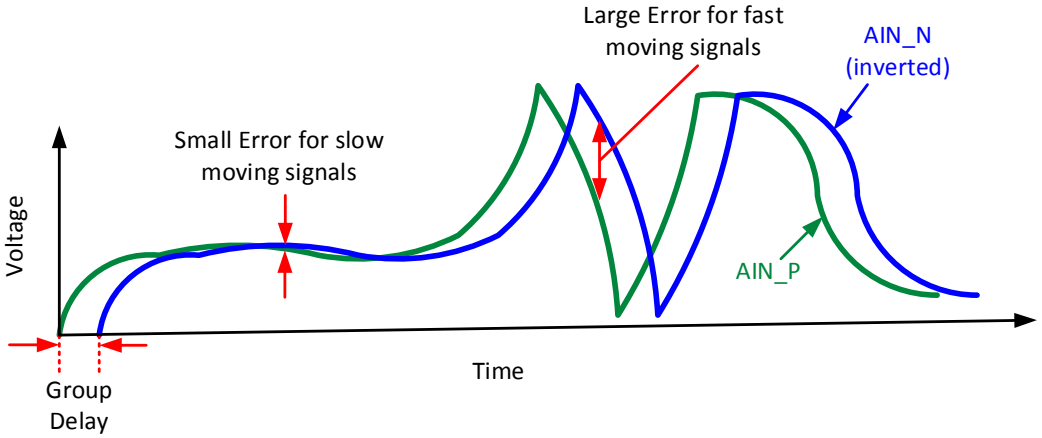
Group Delay (Frequency Domain)

Group delay is the time delay between the applied input signal and the output signal. All amplifiers and filters will have a group delay. Group delay is highlighted for this circuit because the inverting and non-inverting path both have different group delays. This can create distortion for higher frequency signals. See the group delay in time domain plot for additional detail.



Group Delay (Time Domain)

The following graph shows qualitatively how group delay can effect time domain signals. The errors in this plot are exaggerated to emphasize the effect of group delay. The green signal represents the output on AIN_P and the blue signal represents the inverted output on AIN_N. Ideally, the two signals should track, but the group delay shifts the blue signal to the right. Notice that when signals are moving slowly the error is relatively small and when they are moving rapidly the error is larger. Thus, low frequency signals will have good distortion, and higher frequency signals will have degraded distortion. SPICE does not simulate THD, so for quantitative values measurement is required. However, if the input signal period more than 1,000 times larger than the group delay between the channels than this effect can generally be neglected.



Noise Simulation

The following noise calculation considers the amplifier and resistor noise. Note that the noise from U1 is inverted by U2 and added at the differential output. Since this noise is directly correlated, it adds directly as opposed to root sum square addition usually used for noise sources. Also note that the output filter is approximated as first order but it is a more complex filter. The calculated noise compares well to the simulated noise (calculated = 30.5µV_{RMS}, simulated = 28.4µV_{RMS}).

$$e_{nU1} = e_{n320} + e_{n320} = 7\,nV/\sqrt{Hz} + 7\,nV/\sqrt{Hz} = 14\,nV/\sqrt{Hz}$$ Note these two sources are correlated

$$R_{eq} = \frac{R_f \cdot R_g}{R_f + R_g} = \frac{1k\Omega \cdot 1k\Omega}{1k\Omega + 1k\Omega} = 500\Omega$$

$$e_{nReq} = \sqrt{4K_n \cdot T_K \cdot R_{eq}} = \sqrt{4(1.38 \cdot 10^{-23}\,J/K) \cdot (298.15) \cdot (500\Omega)} = 2.87\,nV/\sqrt{Hz}$$

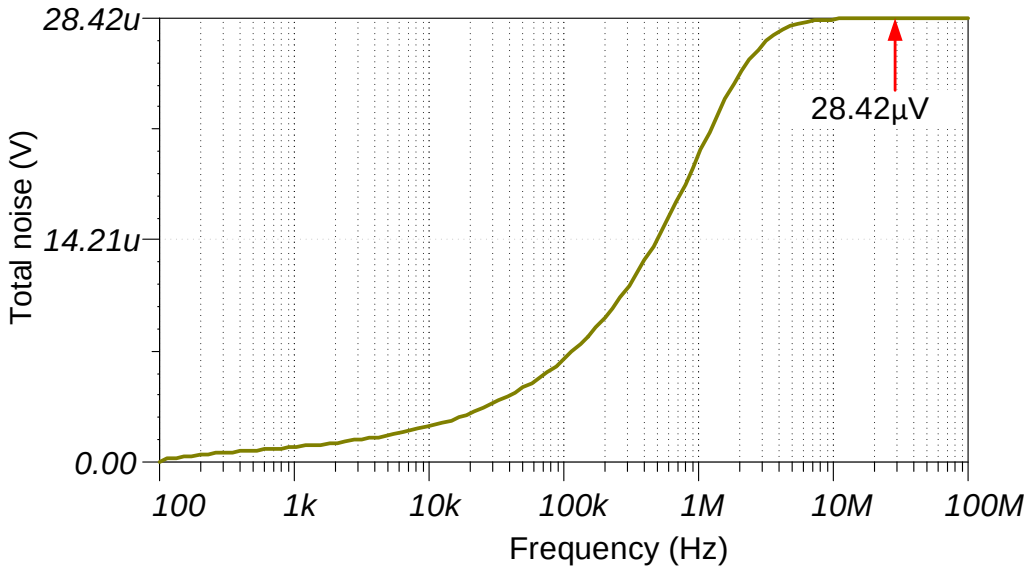
$$e_{nU2} = \sqrt{\left(e_{nReq} \cdot G_n\right)^2 + \left(e_{n320} \cdot G_n\right)^2} = \sqrt{\left(2.87\,nV/\sqrt{Hz} \cdot 2\right)^2 + \left(7\,nV/\sqrt{Hz} \cdot 2\right)^2} = 15.1nV/\sqrt{Hz}$$

$$e_{nT} = \sqrt{\left(e_{nU1}\right)^2 + \left(e_{nU2}\right)^2} = \sqrt{\left(14\,nV/\sqrt{Hz}\right)^2 + \left(15.1nV/\sqrt{Hz}\right)^2} = 20.6\,nV/\sqrt{Hz}$$

$$f_c = \frac{1}{2\pi R \cdot C} = \frac{1}{2\pi (2 \cdot 47.5\Omega) \cdot 1.2nF} = 1.4MHz$$

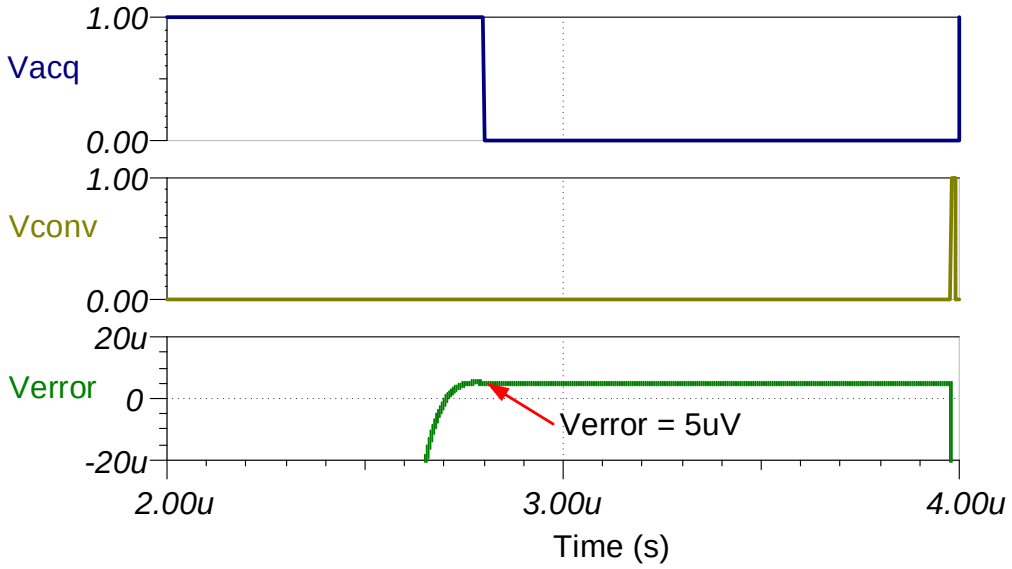
$$E_{nT} = e_{nT} \cdot \sqrt{1.57 \cdot f_c} = 20.6\,nV/\sqrt{Hz} \cdot \sqrt{1.57 \cdot 1.4MHz} = 30.5\mu V_{RMS}$$

The calculated noise compares well to the simulated noise (calculated = 30.5µV_{RMS}, simulated = 28.4µV_{RMS}). See *Calculating the Total Noise for ADC Systems* for detailed theory on this subject.



Transient ADC Input Settling Simulation

The following simulation shows settling to a full scale DC input signal at 500kSPS. This type of simulation shows that the sample and hold kickback circuit is properly selected. See *Introduction to SAR ADC Front-End Component Selection* for detailed theory on this subject.



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS8912	18-bit resolution, 500-kSPS sample rate, integrated reference buffer, fully-differential input, Vref input range 2.5V to 5V.	http://www.ti.com/product/ADS8912B	http://www.ti.com/adcs
OPA320	20-MHz bandwidth, Rail-to-Rail with zero crossover distortion, VosMax = 150 μV, VosDriftMax = 5μV/C, en = 7 nV/√Hz	http://www.ti.com/product/OPA320	http://www.ti.com/opamps

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

Source files for this circuit - http://www.ti.com/lit/zip/SBAC193.

True differential, 4 × 2 MUX, analog front end, simultaneous-sampling ADC circuit

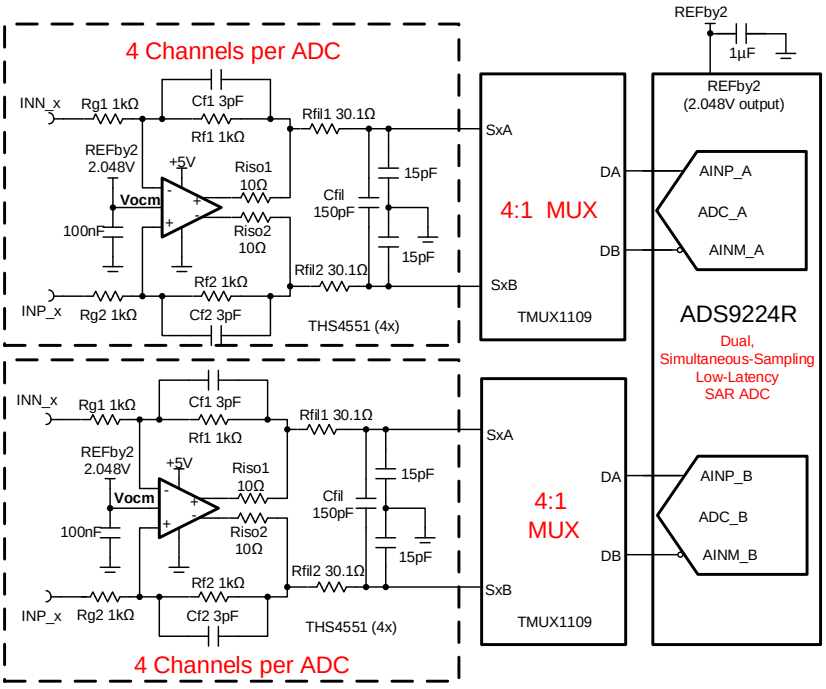
Luis Chioye

Input (THS4551 Inputs)	ADC Input (THS4551 Output)	Digital Output ADS7042
VinP = +0.23V, VinN =+3.866V, VinMin(Dif) = -3.636V	VoutP = +0.23V, VoutN = 3.866V, Vout(Dif) = -3.636V	$8E60_H$ -29088_{10}
VinP = +3.866V, VinN =0.23V, VinMax(Dif) = +3.636V	VoutP = 3.866V, VoutN = +0.23V, Vout(Dif) = +3.636V	$71A0_H$ $+29088_{10}$

Power Supplies			
Vcc	**Vee**	**Vref**	**Vocm**
5	0V	4.096V	2.048V

Design Description

This dual simultaneous-sampling SAR ADC and 4 × 2 channel multiplexed analog front end data acquisition solution can measure differential voltage signals in the range of ±3.866V supporting ADC sampling rates up to 3-MSPS (or effective sampling rate of 750-kSPS per channel) with 16-B resolution. The circuit consists of a dual simultaneous sampling SAR ADC, with each SAR ADC connected to two 4:1 (2x) multiplexers, providing 4 differential input channels per ADC. Eight *Fully Differential Amplifiers* (FDAs) drive the multiplexed SAR ADC inputs. This circuit is applicable in the accurate measurement of dual simultaneous signals in applications such as Optical Modules and Analog Input Modules. It also can be used in motor drive applications such as Servo Drive Control Module, Servo Drive Position Feedback, and Servo Drive Position Sensor.



Specifications

Specification	Goal	Calculated	Simulated
Dual ADC Sampling Speed	3-MSPS	3-MSPS	3-MSPS
Sampling Rate per Channel (dual, simultaneous)	750-kSPS (3-MSPS / 4)	750-kSPS (3-MSPS / 4)	750-kSPS (3-MSPS / 4)
Transient ADC Input Settling	<< 1 LSB << 125 µV	NA	20 µV
Noise (at ADC Input)	$50\mu V_{rms}$	$55.9\mu V_{rms}$	$51.1\mu V_{rms}$

Design Notes

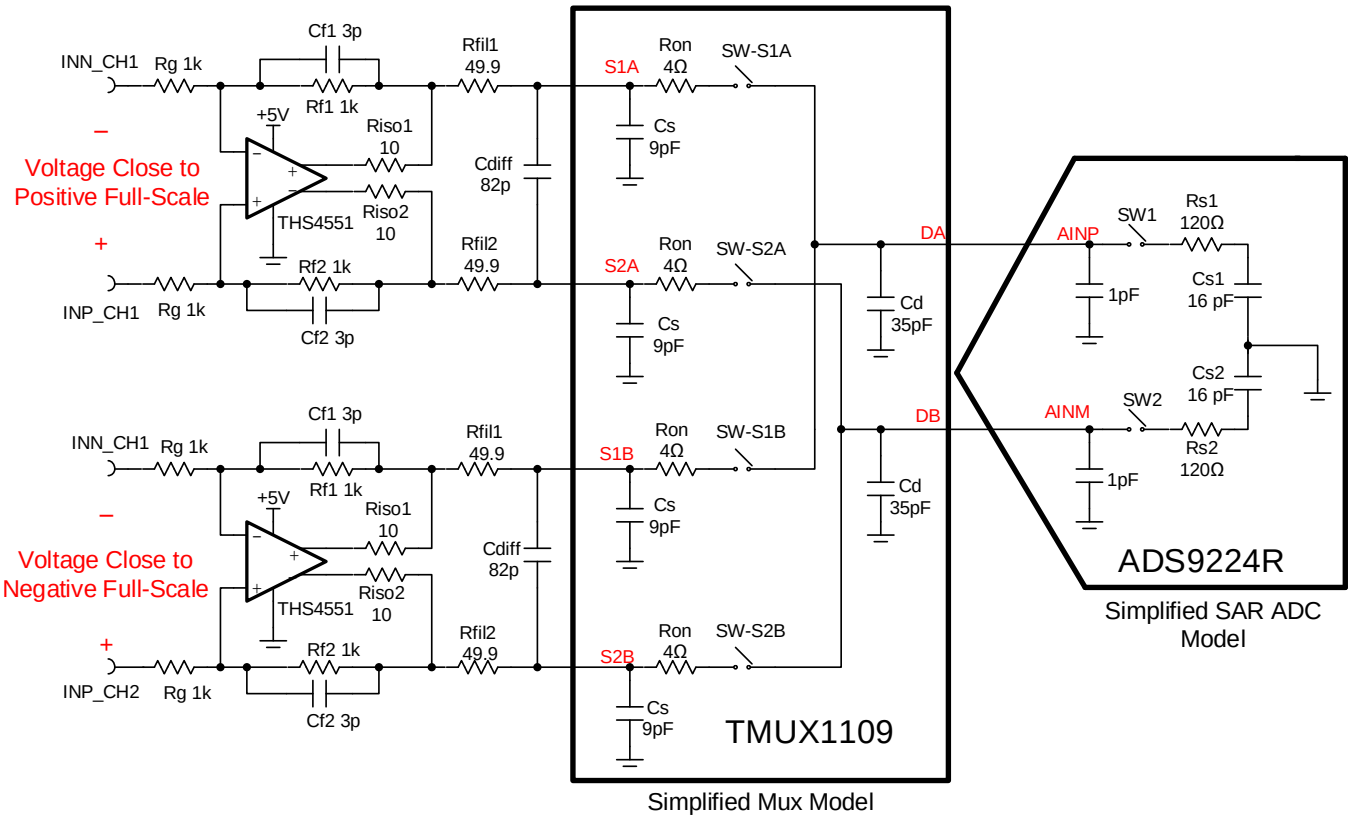
1. The ADS9224R was selected because of the dual simultaneous sampling and high throughput (3-MSPS) requirements.
2. The TMUX1109 4:1 (2x) multiplexer was selected to support 4-channel differential inputs for each ADC.
3. Find ADC full-scale range, resolution and common-mode range specifications. This is covered in the component selection.
4. Determine the linear range of the FDA (THS4551) based on common-mode and output swing specification. This is covered in the component selection section.
5. Select COG capacitors for all filter capacitors at the ADC input to minimize distortion.
6. Select the FDA gain resistors RF1,2 , RG1,2. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift and to minimize distortion.
7. *Introduction to SAR ADC Front-End Component Selection* covers the methods for selecting the charge bucket circuit Rfil1, Rfil1 and Cfil. These component values are dependent on the amplifier bandwidth, data converter sampling rare, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected.
8. The THS4551 is commonly used in high-speed precision fully differential SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling, and multiplexer charge injection and provides the common-mode level shifting to the voltage range of the SAR ADC.

Component Selection

1. Find ADC full-scale input range. In this circuit, ADS9224 internal V_REF= 2.5V
   $ADC_{Full-Scale\ Range} = (\pm 1.6384 V/V) \cdot V_{REF} = \pm 4.096 V$ from ADS9224R datasheet
2. Find required ADC common-mode voltage 2.
   $V_{CM} = \frac{+ADC_{Full-Scale\ Range}}{2} = +2.048 V$ from ADS9224R datasheet
   Use REFby2 Output pin of ADS9224R to connect to FDA (THS4551) VCOM = 2.048V
3. Find FDA absolute output voltage range for linear operation:
   $0.23V < V_{out} < 4.77V$ from THS4551 output low/high specification for linear operation
4. Find FDA differential output voltage range for linear operation. The general output voltage equations for this circuit:
   $V_{outMin} = \frac{V_{outDifMin}}{2} + V_{cm}$
   $V_{outMax} = \frac{V_{outDifMax}}{2} + V_{cm}$
   Rearrange the equations and solve for $V_{outDifMin}$ and $V_{outDifMax}$. Find maximum differential output voltage range based on worst case:
   $V_{outDifMax} = 2 \cdot V_{outMax} - 2 \cdot V_{cm} = 2 \cdot (4.096V) - 2 \cdot (2.048V) = 4.096V$
   $V_{outDifMin} = 2 \cdot V_{outMin} - 2 \cdot V_{cm} = 2 \cdot (0.23V) - 2 \cdot (2.048V) = -3.636V$
   Based on combined worst case, choose $V_{outDifMin}$ = -3.636V and $V_{outDifMax}$ = +3.636V
5. Set FDA gain to 1 V/V
   $Gain_{FDA} = \frac{R_f}{R_g} = \frac{1.00 k\Omega}{1.00 k\Omega} = 1 V/V$
6. Select the minimum charge kickback capacitor filter to optimize circuit for fastest settling.
   $C_{sh} = 16pF$ internal sample-and-hold capacitor from ADS9224R datasheet
   Select a capacitor $10\times$ larger than $C_{fil} = 150pF$
7. Optimize RC charge kickback filter resistors R_{fil1}, R_{fil2} and feedback capacitors C_{f1}, C_{f2} for both settling and stability using TINA simulations. This is covered in the transient settling optimization and stability simulation sections.

Transient Settling Optimization

TINA simulation is used to optimize the RC kickback filter for stability and transient settling. The transient simulation incorporates two adjacent channels of the multiplexer (TMUX1109). To simulate worst case transient settling during the multiplexer scanning sequence, the two adjacent channels are set to a voltage close to positive full-scale and negative full-scale respectively. The multiplexer drain capacitance and series resistance are modeled in the multiplexer simulation circuit. The sample and hold capacitor of the SAR ADC must settle within the 16-Bit resolution of the SAR ADC during the acquisition period. A simplified schematic of the simulation circuit follows:

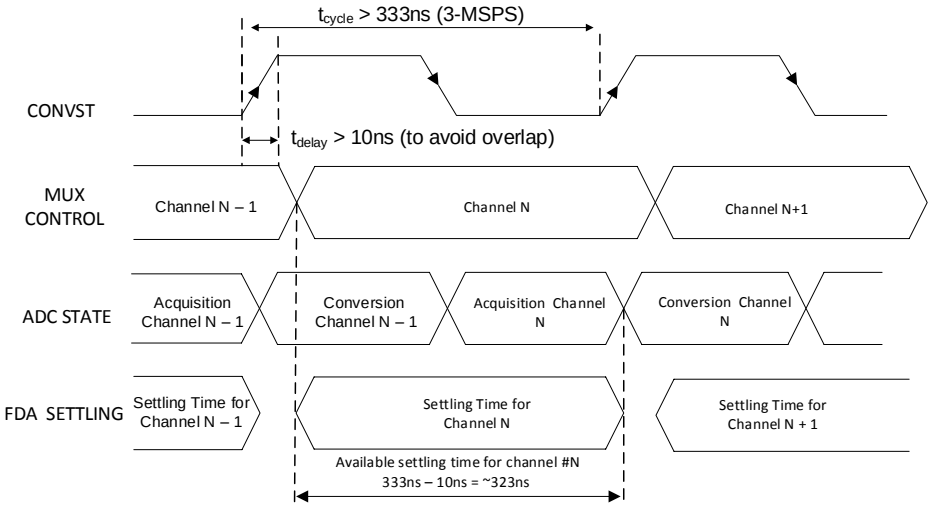


Simplified SAR ADC Model

Simplified Mux Model

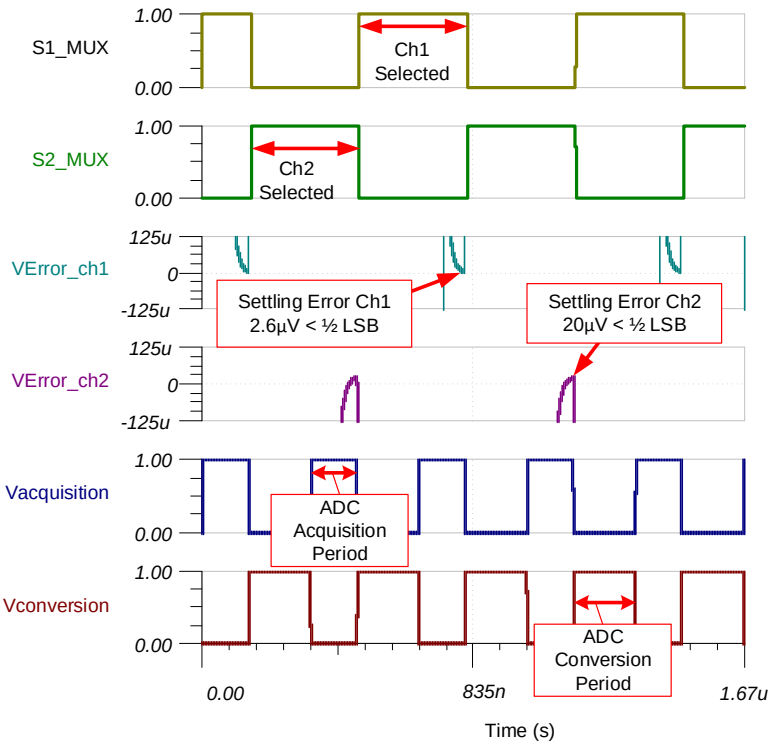
Multiplexer and ADC Control Timing

The following plot shows the ADC conversion control (CONVST) and multiplexer channel control timing. The ADS9224R supports a maximum sampling rate of 3-MSPS or a minimum cycle time of 333ns. To avoid switching channels prior to the rising edge of the CONVST signal, a small delay is implemented in the MUX channel control timing after the CONVST rising edge. Refer to TI design *16-Bit, 400-kSPS, Four-Channel MUX Data Acquisition System for High-Voltage Inputs Reference Design* for detailed theory in the subject.



Transient Settling Results

The following TINA transient simulation shows settling of the FDA, multiplexer, and SAR ADC sample and hold after a full-scale step change between adjacent MUX channels. This type of simulation shows that the sample and hold kickback circuit, and AFE amplifier circuit is properly selected. See *Introduction to SAR ADC Front-end Component Selection* for an explanation of how to select the RC filter for best settling and AC performance.

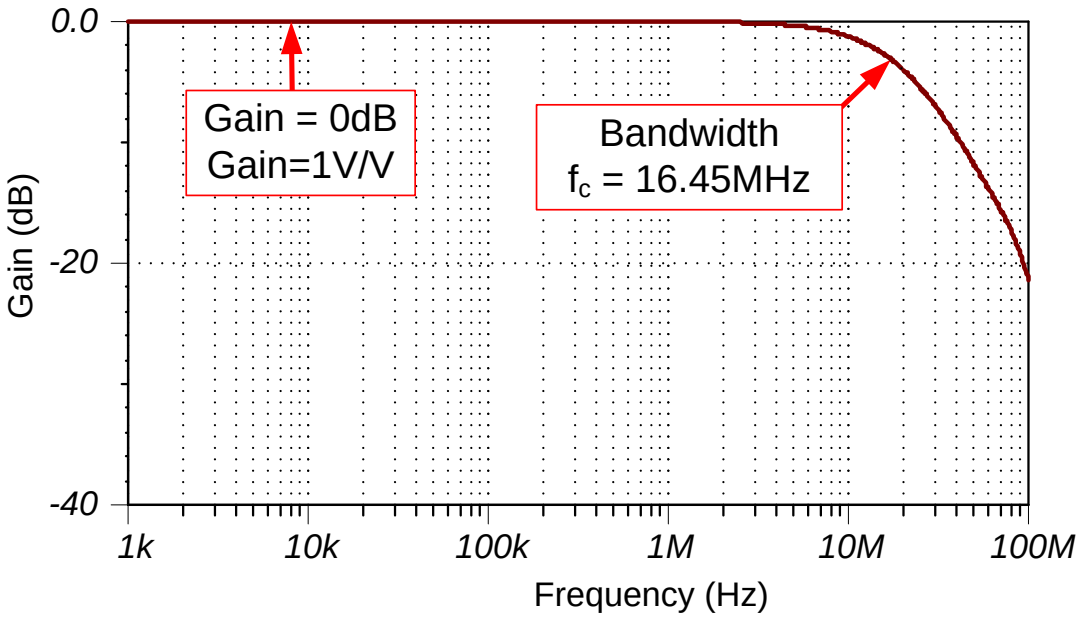


AC Transfer Characteristics

The circuit has a gain of 0-dB (1-V/V) and a simulated frequency bandwidth of 16.45-MHz. Notice that the calculated and simulated bandwidth compare well (calculated = 17.62MHz, simulated = 16.45MHz). See Op Amp Bandwidth for a general overview of bandwidth calculations and simulations.

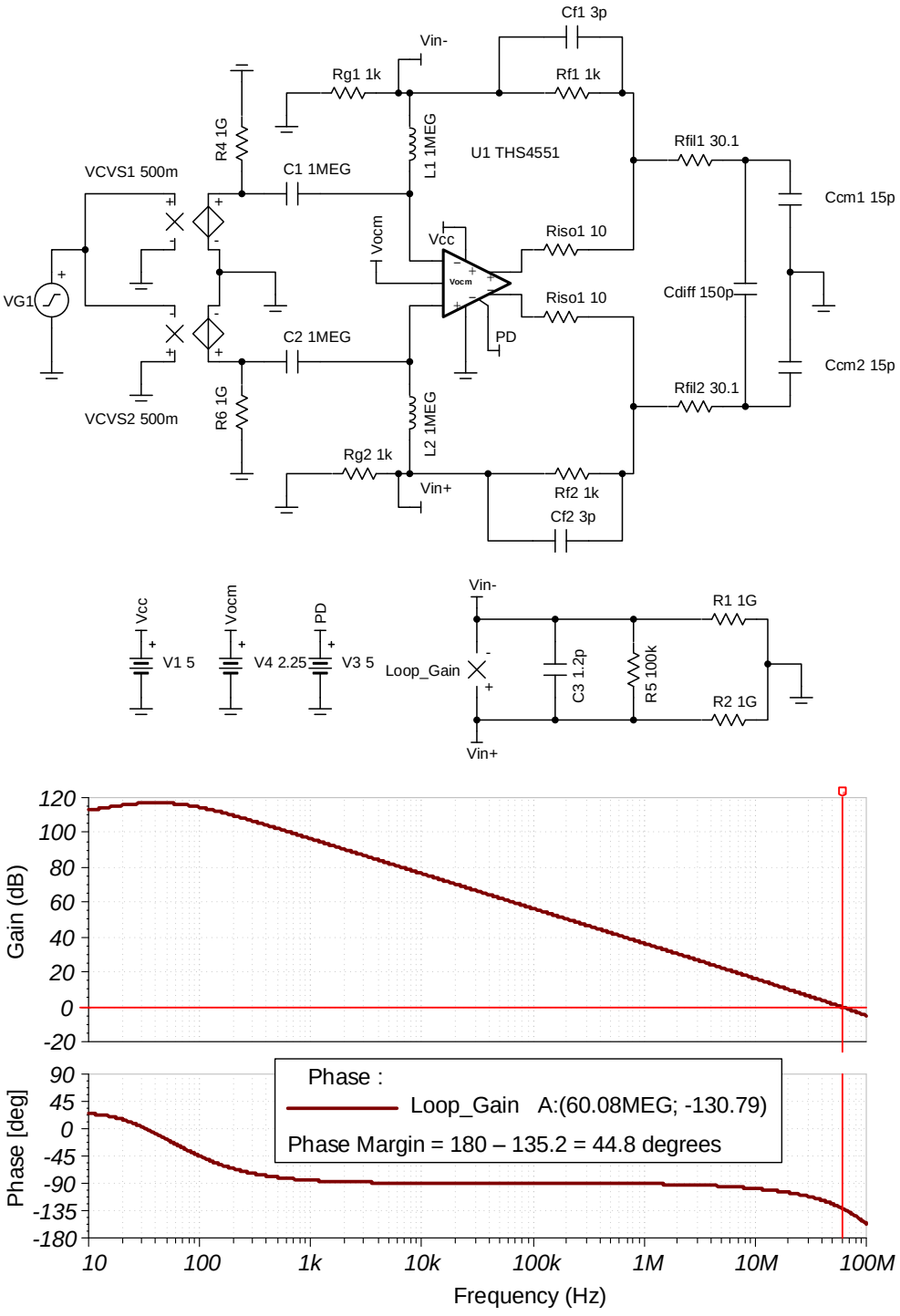
The system bandwidth is set by the output filter:

$$f_c = \frac{1}{2\pi (R_{fil1} + R_{fil2}) C_{diff}} = \frac{1}{2\pi \left(30.1\Omega \boxplus 30.1\Omega\right)\left(150pF\right)} = 17.62MHz$$



Stability Simulation Graph

The following circuit is used in TINA to measure loop gain and verify phase margin using AC analysis in TINA. Resistors RISO = 10Ω are used inside the feedback loop to increase phase margin. The circuit has good stability (approximately 45 degrees of phase margin). See Op Amp Stability for detailed theory on this subject.



Noise Simulation

Simplified noise calculation estimate:

The dominant pole in this data acquisition circuit is in the RC kickback filter:

$$f_c = \frac{1}{2\pi (R_{fil1} + R_{fil2}) C_{diff}} = \frac{1}{2\pi \left(30.1\Omega \boxplus 30.1\Omega\right)\left(150pF\right)} = 17.62MHz$$

Noise of THS4551 FDA referred to ADC input

Noise Gain: $NG = 1 + R_f / R_g = 1 + \frac{1k\Omega}{1k\Omega} = 2V/V$

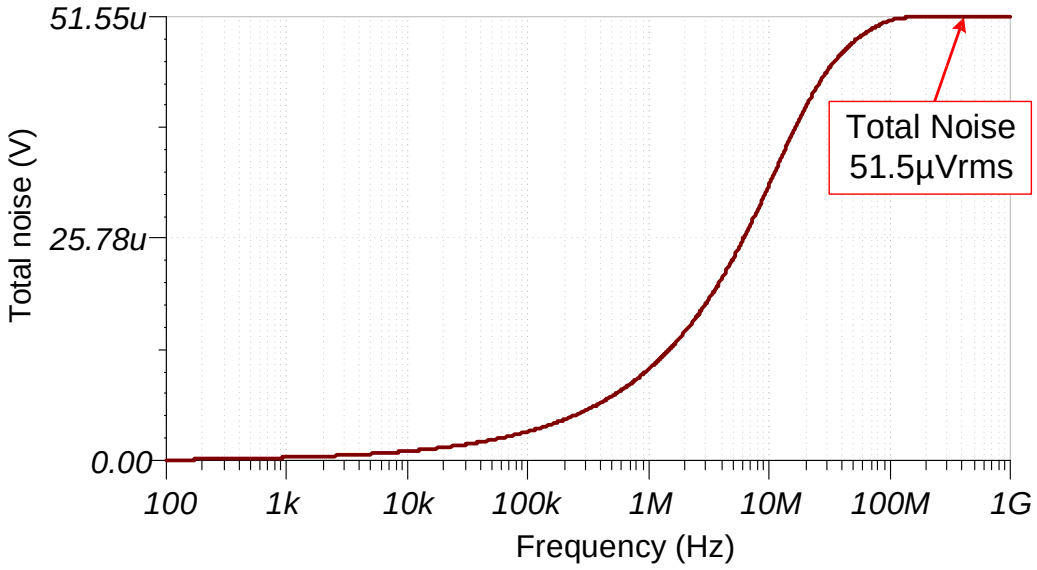
$$e_{noFDA} = \sqrt{\left(e_{nFDA} \cdot NG\right)^2 + 2\left(i_{nFDA} \cdot R_f\right)^2 + 2\left(4kTR_f \cdot NG\right)}$$

$$e_{noFDA} = \sqrt{\left(3.4nV/\sqrt{Hz} \cdot 2.00V/V\right)^2 + 2\left(0.5pA/\sqrt{Hz} \cdot 1k\Omega\right)^2 + 2\left(16.56 \cdot 10^{-18} \cdot 2.00V/V\right)}$$

$$e_{noFDA} = 10.629nV/\sqrt{Hz}$$

$$E_{nFDA} = e_{noFDA} \cdot \sqrt{K_n \cdot f_c} = \left(10.629nV/\sqrt{Hz}\right)\sqrt{1.57 \cdot 17.62MHz} = 55.90\mu Vrms$$

The following figure shows the TINA simulated total noise for the FDA circuit. See *Calculating the Total Noise for ADC systems* for detailed theory on this subject. Note that the calculated and simulated noise compare well (calculated = 55.9µV$_{rms}$, simulated = 51.5µV$_{rms}$).



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS9224R	16-bit resolution, SPI, 3-MSPS sample rate, fully-differential input, integrated 2.5-V reference, dual, simultaneous sampling, low-latency	http://www.ti.com/product/ADS9224R	http://www.ti.com/adcs
THS4551	150-MHz, 3.3-nV / $\sqrt{Hz}$ input voltage noise, fully-differential amplifier	http://www.ti.com/product/THS4551	http://www.ti.com/opamps

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Link to Key Files

See the Tina files for low-power sensor measurements - http://www.ti.com/lit/zip/SBAC219.

Revision History

Revision	Date	Change
A	November 2018	Downscale title. Updated the schematic in the *Transient Settling Optimization* section.