LOW-POWER LOW-VOLTAGE SIGMA-DELTA MODULATORS: 90 nm AN ADVANTAGE?

Libin Yao, Michiel Steyaert and Willy Sansen
Katholieke Universiteit Leuven, ESAT-MICAS
Kasteelpark Arenberg 10, B-3001 Leuven (Heverlee), Belgium
Email: libin.yao@esat.kuleuven.ac.be

Abstract

Moving into ultra-deep-submicron CMOS technologies, the design of Σ-Δ ADCs faces more challenges. Among them important ones are the restriction from the decreased supply voltage, the higher distortion and degraded device characteristics. The reduced supply voltage decreases the signal swing and lower noise floor is required to maintain the same signal-to-noise ratio. On the other hand, some advantages are gained. Important ones are the reduced threshold voltage of the transistor and lower power consumption of the digital circuits. In this paper, low-power low-voltage Σ-Δ ADC design strategies are introduced and design techniques in ultra-deep-submicron CMOS technologies are presented. As an example, a 1 V, 20 kHz, 88 dB, 140 μW Σ-Δ modulator design in a 90 nm CMOS technology is presented.

1. Introduction

Driving by the speed demand of digital circuits, in recent years the deep-submicron CMOS technology is pacing into 100 nm range, i.e. ultra-deep-submicron. As a consequence, the power supply voltage drops below one Volt earlier than expected. On the other hand, portable electronics with low-voltage operations find their big market. As a major building block, the analog to digital converter (ADC) is widely used in mixed-signal designs. As an interface between the analog world and the digital world, ADCs are implemented with the same technology as the digital circuit hence the power supply voltage reduction is inevitable. The decrease of the supply voltage obviously results in analog circuits performance degradations.

Among different ADCs, the Σ-Δ ADC is most suitable for high-resolution applications due to its high-linearity feature. The high linearity is gained by using the intrinsic linear 1-bit quantizer and the oversampling technique. However, the non-idealities in the building blocks strongly affect the ADC performances. To

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Table 1: The SIA roadmap 2003 edition

Year	2003	2004	2005	2006	2007	2008	2009
Feature size(nm)	100	90	80	70	65	57	50
Supply Voltage(V)	1.2	1.2	1.1	1.1	1.1	0.9	0.9

design a Σ-Δ ADC, main efforts are put on fighting with the non-idealities of building blocks. The reduced supply voltage makes the situation even worse.

In this paper, design difficulties of moving into ultra-deep-submicron technologies are addressed first. Then several low-power low-voltage Σ-Δ ADC design strategies and special designed circuits in ultra-deep-submicron technologies are introduced. As an example, a low-power low-voltage Σ-Δ modulator in a 90 nm CMOS technology is presented. Finally several conclusions on the design of low-power low-voltage Σ-Δ modulators in ultra-deep-submicron CMOS technologies are drawn.

2. Moving into Ultra-Deep-Submicron CMOS

Table 1 shows the International Technology Roadmap for Semiconductors 2003 edition from the Semiconductor Industry Association(SIA) [1]. From 2004, the sub-100 nm CMOS technologies will be in the mass production stage. The development is driven by the speed demand of the digital circuit. However, for the analog design, the movement into ultra-deep-submicron technologies brings some design difficulties. The impacts of moving into ultra-deep-submicron technologies on the Σ-Δ ADC design are analyzed as follows.

2.1. Decreased Signal Swing

The signal swing defines the dynamic range for a system with a certain noise floor. In order to increase the dynamic range of a system, the signal swing should be maximized and the noise floor should be minimized. Unfortunately, the movement to ultra-deep-submicron technologies brings the restriction of the supply voltage, which leads to a small signal swing of the system. For a thermal-noise-limited Σ-Δ ADC, the dynamic range can be expressed as:

$$DR = 10\,log\frac{P_s}{P_n} = 10\,log\frac{{V_{inmax}}^2}{2P_n} \tag{1}$$

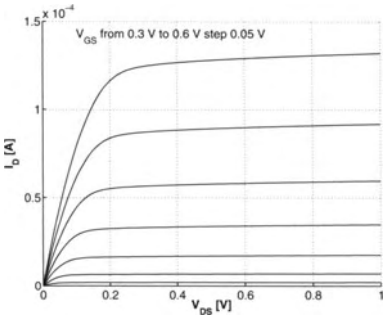
And the maximum input signal amplitude, V_{inmax}, can be expressed as:

$$V_{inmax} = V_{ref} \cdot OL \tag{2}$$

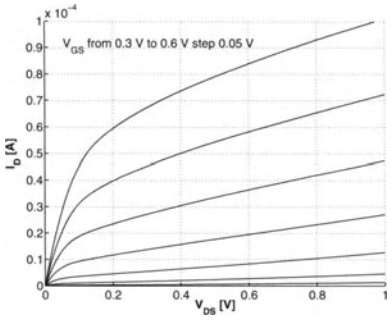
Where P_n is the input referred noise power, V_{ref} and OL are the reference voltage and the overload level, respectively. The overload level is the normalized input amplitude while the signal-to-noise ratio (SNR) decreases from the peak SNR by 3 dB. For a certain Σ-Δ ADC topology, the overload level is fixed. One can only increase the reference voltage to increase the maximum input signal amplitude. But in the real circuit the reference voltage is limited by the output swing of the integrators, which is limited by the output swing of the operational transconductance amplifier(OTA), and finally limited by the supply voltage.

2.2. Degraded Transistor Characteristics

Due to the channel length modulation, the drain-source resistance, R_{DS}, of a MOS transistor, decreases along with the reduction of the channel length. Fig. 1 gives the transistor $I_D - V_{DS}$ characteristics of transistors with different channel lengths from the same ultra-deep-submicron CMOS technology. The intrinsic gain, de-



(a) Transistor $I_D - V_{DS}$ characteristics with W/L=8 μm/0.8 μm.



(b) Transistor $I_D - V_{DS}$ characteristics with W/L=0.8 μm/0.08 μm.

Figure 1: Transistor characteristics with different channel length in an ultra-deep-submicron CMOS technology.

fined in (3), is the amplification ability of a single transistor.

$$A_{intrinsic} = \frac{g_m}{g_{DS}} = \frac{2 \cdot I_D}{V_{GS} - V_T} \cdot \frac{1}{I_D \cdot \lambda} = \frac{2}{(V_{GS} - V_T)\lambda} \tag{3}$$

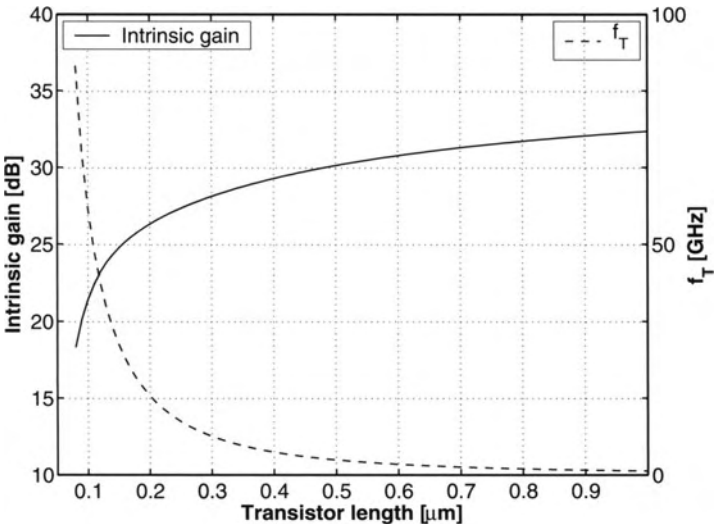


Figure 2: The transistor intrinsic gain and f_T vs. channel length curves with $V_{GS} - V_T = 0.2\ V$ and $V_{DS} = 0.3\ V$ in an ultra-deep-submicron CMOS technology.

The intrinsic gain of a transistor decreases along with the transistor channel length reduction. Fig. 2 shows the transistor intrinsic gain and f_T curves vs. the transistor channel length. It can be seen that if the transistor channel length is increased, then the f_T decreases rapidly. The gain-speed trade-off must be made here.

Another problem with ultra-deep-submicron technologies is that the transistor channel noise increases while the channel length is shrunken [2]. Further more, the $1/f$ noise corner frequency is higher in ultra-deep-submicron technologies, making the design of high dynamic range Σ-Δ modulators more difficult.

2.3. Distortion

The main source of the distortion on the Σ-Δ modulator is the OTA inside the loop. In the low-voltage environment, transistors are forced to work at the relatively larger signal condition, especially for output devices inside the OTA. From Fig. 1 it is seen for ultra-deep-submicron technologies, the drain-source resistance, R_{DS} of a transistor, has strong dependence on the source-drain voltage. The drastically changed source-drain voltage results in a big variation on the output conductance of the transistor, and generates more distortion.

Another source of the distortion is the input voltage dependent on-resistance of the switch. The main effort to solve this problem is making a constant on-resistance of the switch, which means constant overdrive voltage for switch transistors. In the low-voltage environment, normally clock boosting circuits are needed to do so [3].

3. Low-Voltage Low-Power Σ-Δ Modulator Design

The Σ-Δ modulator is always combined with digital circuits to form a system. As a result, the Σ-Δ modulator and digital circuits are fabricated on the same chip and work under the same low supply voltage. Different from the classic Σ-Δ modulator design, the design is in the low-voltage environment and some design strategies should be employed here. At the same time, the low-power consumption is normally addressed.

3.1. Low-Voltage Strategy

For a low-voltage Σ-Δ modulator, the signal swing is vital. The rail-to-rail output ability is essential for building blocks. The main building block in a Σ-Δ modulator is the OTA. OTA topologies that can offer rail-to-rail output swings are preferred. This demand is not only required by the signal swing consideration, but also by the distortion consideration. Shown in Fig. 3, the common-source output stage is often chosen for its rail-to-rail output ability. However, the insufficient gain of the single common-source stage forces designers turning into multi-stage OTA topologies. For a switched-capacitor Σ-Δ modulator, the DC gain of the OTA defines the accuracy while the slew-rate and settling time define the speed of the modulator. In the low-voltage environment, these requirements are more difficult to reach at the same time. Trade-offs are usually made to obtain some important parameters.

The common-mode input and output voltage may be different in the low-voltage environment. To obtain the highest output swing, the output common-mode voltage is set to the middle of the supply voltage. However, if the input common-mode voltage is also set to the middle of the supply voltage, then the rail-to-rail input capability, which can't be offered by the normal differential input stage, is required for the OTA. If the input common-mode voltage is set near either one supply rail, then the normal OTA can be used without the rail-to-rail input requirement and simplifies the circuits.

For the modulator topology, the single loop topology is usually selected in low-voltage designs for its relaxed requirements for building blocks. And the single-bit

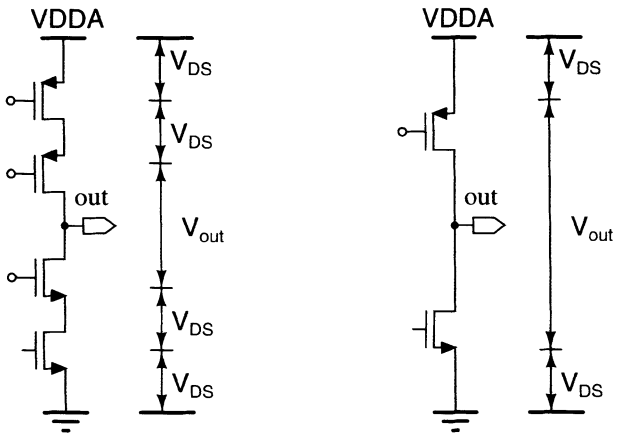


Figure 3: Output swing comparison of cascode and common-source stage.

quantizer is preferred in low-voltage Σ-Δ modulators, as it is easy to implement and the requirements, such as the offset and hysteresis, are quite relaxed too. The low-voltage multi-bit quantizer requires the rail-to-rail input ability for comparators and the offset requirement is more stringent than the single-bit one's [4].

The best strategy for low-voltage Σ-Δ modulator is to combine the circuit and system-level design techniques together. An example is the low-distortion Σ-Δ modulator topology [5]. In this topology the signal swing inside the loop can be made much smaller than that of the classic topology, which is most preferred in low-voltage Σ-Δ designs. This unique feature makes this topology a good candidate for low-voltage low-power Σ-Δ modulator designs.

3.2. Low-Power Strategy

The first and best low-power strategy is on the system level. To choose a better system topology that consumes less power is the most effective way to reduce the power consumption. For a Σ-Δ modulator with given specifications, the modulator topology, sampling frequency and oversampling ratio are essential for the system power consumption.

As described before, the reduction of the power supply voltage limits the signal swing. For the same dynamic range, the noise floor, or the mismatch error of a system, should be reduced as well. The noise floor, often restricted by the KT/C noise in the switched-capacitor circuit, can only be suppressed by increasing the

capacitance value. From (1), the dynamic range of a Σ-Δ ADC can be expressed as:

$$DR = 10\,log\frac{P_s}{P_n} = 10\,log\frac{{V_{inmax}}^2}{2P_n} = 10\,log\frac{{V_{inmax}}^2 \cdot OSR \cdot C_s}{2kT} \quad (4)$$

Where OSR and C_s is the oversampling ratio and sampling capacitance in the first integrator, respectively. From (4) it is clear that for a certain dynamic range, while signal swing is reduced, the oversampling ratio or the first sampling capacitance must be increased. On the other hand, the mismatch error, which is reversely proportional to the square root of the area of the device, can only be suppressed by increasing the size of the device. Increasing both sizes will need higher current to maintain the same speed, which means higher power consumption. In the system point of view, the larger signal swing leads to the lower power consumption. So the higher signal swing is also an important low-power strategy.

The building block topology is also important for low-power design. In Σ-Δ modulators, the OTA consumes the most power, especially the one in the first integrator. Among all OTA topologies, the single-stage topology is the most power-efficient one as it is load-compensated and no power is wasted in the compensation. Since in low-voltage Σ-Δ modulators, OTAs work in relatively large signal condition and large capacitive loads are always present, so the load-compensated, class AB OTA is preferred in terms of low-power consumption [6].

One of the most interesting property of Σ-Δ modulators is the noise suppression inside the loop. Utilizing this feature can result a large amount of power saving. For a single-loop Sigma-Delta modulator, the noise suppression in the node k can be calculated by

$$F_{sup,k} = \frac{OSR^{2k}}{\pi^{2k}}(2k+1)(\prod_{i=0}^{k} a_i)^2 \quad (5)$$

Where F is the noise suppression factor, OSR is the oversampling ratio and a_i denotes the loop coefficient of the i-th stage. This property allows the sampling capacitances of following stages being scaled down proportionally to corresponding ratios. The only restriction is from the matching requirements. Reducing the sampling capacitance results the reduction of the load capacitance of the OTA and hence reduce the power consumption.

For a single transistor, the ratio between the transconductance and the drain current, g_m/I_D, describes the power efficiency of this single device. Fig. 4 shows the g_m/I_D and f_T as a function of the transistor overdrive voltage of a transistor in an ultra-deep submicron CMOS technology. In the sub-threshold region the transistor achieves the highest power efficiency. This region is called the weak inversion region. However, the transistor biased in this region is slow, as a large

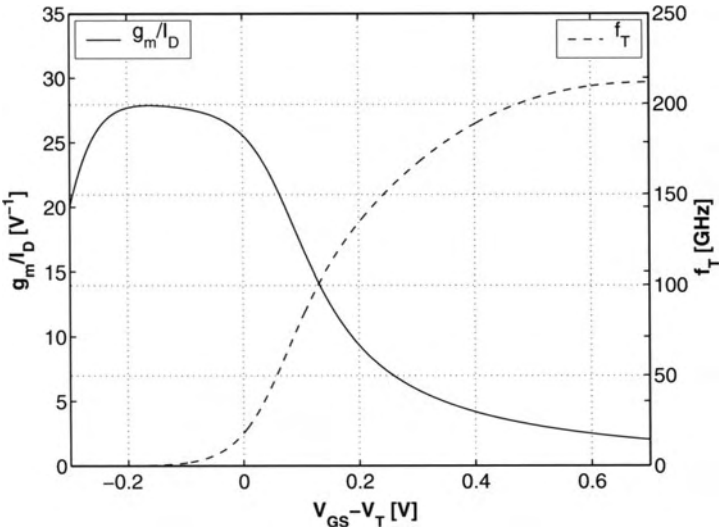


Figure 4: The transistor g_m/I_D ratio and f_T vs. $V_{GS} - V_T$ curves in an ultra-deep-submicron CMOS technology.

W/L is required. A compromise between the power efficiency and speed is made here. For ordinary applications, the weak to moderation inversion region ($V_{GS} - V_T \approx 0.1 \sim 0.2\ V$) is preferred, where both good power efficiency and speed performance can be achieved.

4. Design of a Single-Loop Third-Order Σ-Δ Modulator in 90 nm CMOS

To explore the possibility of designing high-performance Σ-Δ ADCs in ultra-deep-submicron CMOS technologies and verify the design strategies described before, a single-loop third-order Σ-Δ modulator was designed in a 90 nm pure digital CMOS technology. The technology features 9 copper layers of interconnect and low-K insulation. But no metal-insulator-metal (MIM) capacitor is available in this technology. The goal is to design a high-resolution, audio bandwidth Σ-Δ modulator with minimum power consumption in this latest technology.

4.1. Topology Selection

As mentioned before, under 1 V power supply, the non-idealities of the building block is much severe. So single-loop Σ-Δ topology, which is not sensitive to these

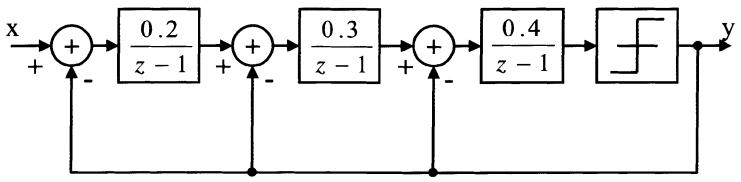
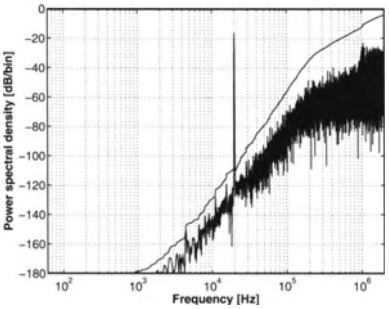


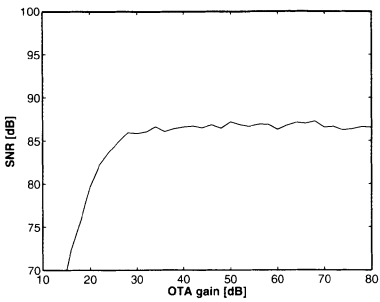
Figure 5: Single-loop third-order Σ-Δ modulator topology.

non-idealities, is chosen to implement this design. In this pure digital technology, no MIM capacitor is available. All capacitances should be implemented by means of the metal-metal capacitance or fringe capacitance. The matching properties of these kinds of capacitances are worse than that of the MIM capacitance. So the loop-coefficients are chosen not so aggressive comparing to [7] to tolerate matching errors. Fig. 6(a) shows a behavioral simulation result of the output spectrum of the modulator. More than 85 dB of the signal to noise ratio (SNR) has achieved by using the proposed topology. Fig. 6(b) shows the SNR of the converter vs. the OTA DC gain. The minimum DC gain requirement of the OTA is 30 dB to achieve a 85 dB SNR for the converter.

Fig. 7 shows the output swing of each integrators normalized to the reference voltage while the input amplitude is 70% of the reference voltage. The main consideration in the reference voltage is the distortion. The higher reference voltage means the higher dynamic range and higher output swings of OTAs. However, the high output swing drives the output transistors in the OTA out of the saturation region. As a result, the transistor's output impedance and the voltage gain are decreased drastically. This non-linear operation generates distortion. The lower reference voltage is, the less distortion is generated. As a compromise between the dynamic range and distortion, the reference voltage was selected to be 0.6 V, which can ensure all the output transistors work in the saturation region with some safe margins.



(a) Output spectrum of the proposed topology with a 20 kHz input signal.



(b) SNR vs. OTA DC gain for the proposed 3rd-order single-loop Sigma-Delta modulator.

Figure 6: Performance of the proposed topology.

From (4) the required first sampling capacitance value can be calculated. The first sampling capacitor is set to 6 pF. The second and third sampling capacitor can be scaled down. According to (5), for the proposed topology, the noise suppression of the first, seconded and third stage is 28 dB, 55 dB and 82 dB, respectively. Considering the matching property of the capacitors, both the second and third sampling capacitor are set to 0.4 pF. Accordingly the OTAs can also be scaled-down to save the power.

4.2. Building Block Design

As described previously, the rail-to-rail output swing is highly preferred for the OTA, and load-compensated OTA is preferred due to its high power-efficiency. The current mirror OTA is a good candidate for this task. However, the gain of the current mirror OTA is only a gain of a single stage amplifier. In ultra-deep-submicron technologies, the single stage gain is in the order of 20-30 dB ranges, which is not enough for the proposed topology. A gain enhancement technique is used in this design [8], and the DC gain has been enhanced to around 50 dB to fulfill the requirement with some safe margin. This OTA is load-compensated and with a class AB output stage, which both are good to lower the power consumption.

Shown in Fig. 8, the OTA is a simple current mirror OTA with two shunting

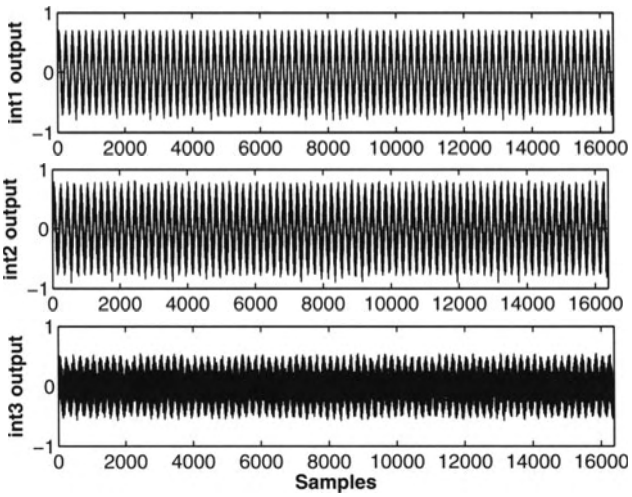


Figure 7: Normalized output of each integrators of the proposed topology.

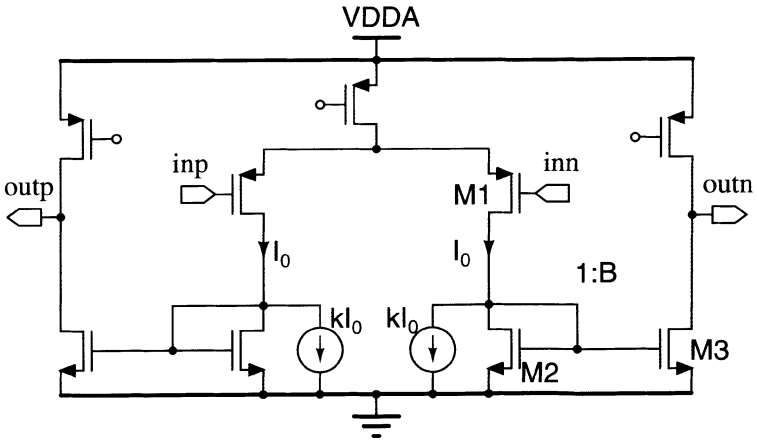


Figure 8: The current mirror OTA with gain enhancement.

current sources. The DC gain of a current mirror OTA can be described as:

$$A_0 = gm_1 \cdot B \cdot r_{o3} = \frac{2 \cdot I_{D1}}{V_{GS1} - V_T} \cdot \frac{B}{I_{D3} \cdot \lambda_3} = \frac{2}{(V_{GS_1} - V_T)\lambda_3} \tag{6}$$

Where λ_3 is the channel length modulation coefficient of the transistor M3 and $I_{D3} = B \cdot I_{D1}$. From (6) it can be seen that the gain of the current mirror OTA is still in the order of an intrinsic gain of a single transistor. For ultra-deep-submicron technologies, the gain is merely around 30 dB. With the current source shunting part of the current from the diode-connected transistor M2, the enhanced gain now is:

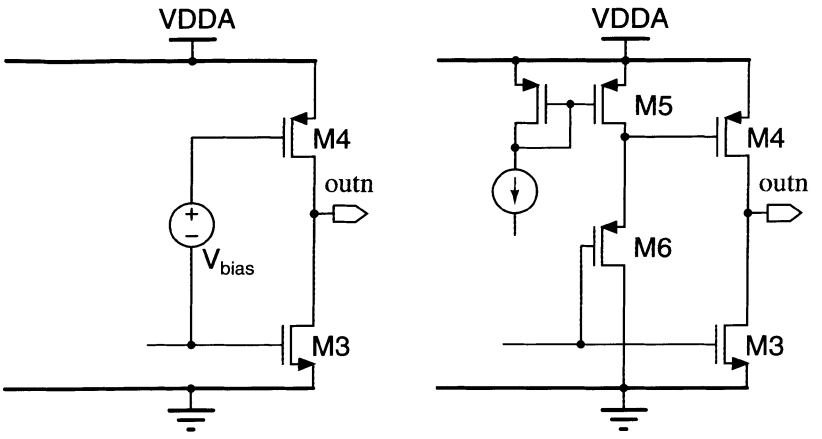
$$A_{en} = gm_1 \cdot B \cdot r_{o3} = \frac{2 \cdot I_{D1}}{V_{GS1} - V_T} \cdot \frac{B}{I_{D3} \cdot \lambda_3} \tag{7}$$

Where now $I_{D3} = (1 - k) \cdot B \cdot I_{D1}$, so:

$$A_{en} = \frac{1}{1 - k} \cdot \frac{2}{(V_{GS1} - V_T)\lambda_3} = \frac{A_0}{1 - k} \tag{8}$$

From (8), it can be seen that the OTA gain is enhanced $\frac{1}{1-k}$ times. The gain enhancement can be adjusted by changing the k factor. In practice, the gain enhancement is restricted by several factors. The first is the restriction of the OTA frequency response. Doing that actually decreases the non-dominant pole frequency and the phase margin. The criterion is to keep a safe phase margin. As the dominant pole is created by the load capacitance, so the higher load capacitance the OTA drives, the higher k factor can be chosen. Secondly, in practice the matching of current sources determines the total gain enhancement. To ensure good matching between the tail current source and the shunting current source, both of them are mirrored from the same reference current source. Due to the matching error, the k factor can not be set too high. Practically the k factor can be set to 0.8-0.9, which can enhance the OTA gain by 10-20 dB. The overall OTA DC gain can reach 40-50 dB by using this technique and the requirement of the Σ-Δ modulator can be fulfilled.

Another low-power consideration is the class AB operation of the OTA output stage. Shown in Fig. 9(a), the class AB operation is made by driving the PMOS transistor M4 by a floating voltage source V_{bias}. This is a very crude class AB output scheme that the class AB characteristics are not perfect. But here in switched-capacitor circuits, the high slew rate is more important than the good class AB output characteristics. As long as the output settles to the required final value within one clock period, the settling procedure is not important here. Actually this class AB stage increases the current sourcing ability of the output stage, and then effectively increases the slew rate of the OTA. The floating voltage



(a) Class AB biasing of the output PMOS transistor.

(b) Implementation of the class AB biasing.

Figure 9: The class AB operation of the output stage.

source V_{bias} is implemented by a level-shifter, shown in Fig. 9(b). The transistor M5 and M6 is identical and have the same drain current. As a result, their gate-source voltages are identical too. By properly biasing the M5, a certain V_{bias} can be obtained.

By using the techniques described above, a current mirror OTA with gain enhancement was designed. Fig. 10 shows the simulated frequency response of the OTA using the 90 nm CMOS technology. The simulation was done under a 1 V supply voltage and 6 pF load capacitance. The k factor was set to 0.9. The DC gain of the OTA reaches 50 dB and the phase margin is 60 degrees with a GBW of 15 MHz. The total power consumption of the OTA is 80 μW.

The common-mode feedback (CMFB) circuits are implemented with a switched-capacitor (SC) circuit [9]. The advantage of the SC CMFB circuits is the lower power consumption and it is easy to make the common-mode bandwidth of the OTA higher than the differential-mode bandwidth.

Another practical low-power consideration is the feedback scheme of the integrator. Fig. 11 shows two different feedback schemes. The left one directly connects the feedback signal to one terminal of the sampling capacitor during the clock period C2, i.e. integration phase of the integrator. The right one uses two sampling capacitors to sample the input signal and feedback signal, respectively,

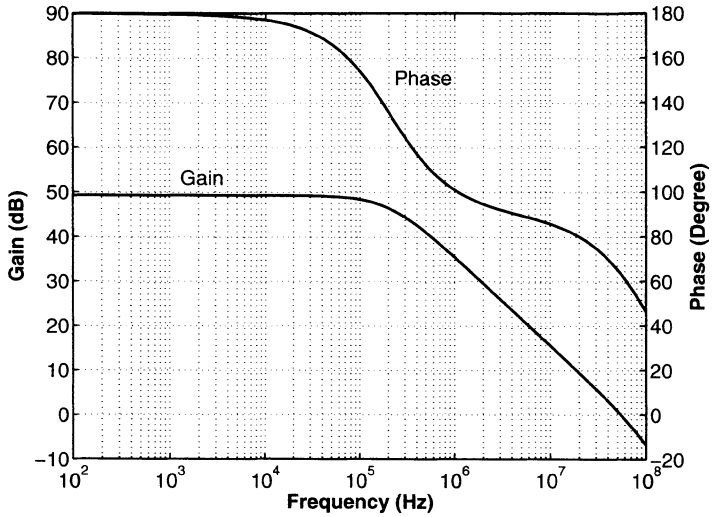


Figure 10: Simulated frequency response of the proposed current mirror OTA with gain enhancement.

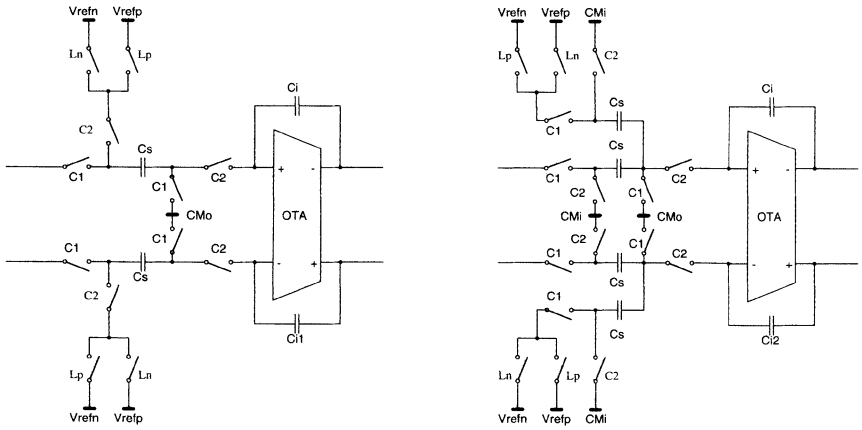


Figure 11: Different feedback schemes of the Σ-Δ modulator.

and then summarize these two signals during the integration phase of the integrator. Both of these two schemes accomplish the same function, while the right scheme uses more capacitors and switches. On the left circuit, the sampling capacitor is discharged to either Vrefp or Vrefn during the integration phase, and during the sampling phase the sampling capacitor is charged to the input voltage. During the charge and discharge cycle, the voltage change on the sampling capacitor is from either Vrefp or Vrefn to Vin, which is quite large. Most importantly, the charge current is provided by the preceding OTA. These large signal charges require a high slew-rate of the OTA and consume more power. However, on the right circuit, the large charge current is provided by the reference voltage. The OTA only charges the sampling capacitor from 0 to the input voltage, which is smaller. So the right circuit relaxes the requirement for the preceding OTA and consumes less power. Thus it is chosen in this design.

Thanking for the relatively low threshold voltage of this technology, all switches can be directly driven without any clock boosting stage. Local drivers are employed to drive switches. Minimum transistor lengths are used in these drivers and switches to lower the power consumption.

The quantizer used in this design is a regenerative comparator followed by a static latch [10]. The requirements, e.g. the offset and hysteresis, for the quantizer are quite loose due to the single-loop topology. Moreover, the dynamic operation helps to lower the power consumption as well.

4.3. Capacitance Implementation

All capacitances in this design are implemented by metal wall structure, shown in Fig. 12 [11]. This structure uses the lateral capacitance instead of the vertical capacitance. In ultra-deep-submicron technologies, the horizontal spaces between metal lines are smaller than that of vertical space, resulting high unit capacitance. Further more, the horizontal geometric sizes are well controlled in these technologies. Totally 8 metal layers are used to build the capacitance in this design. Calculation shows the unit capacitance is around 1.7 $fF/\mu m^2$, which is higher than that of the normal MIM capacitance in mixed-signal technologies. However, the matching property is worse than that of MIM capacitance. As the loop coefficients are defined by the capacitance ratios, robust loop coefficients are chosen to be more tolerant to the inferred-matched capacitance. Besides, this kind of capacitances is widely used in this design as decoupling capacitors around the chip.

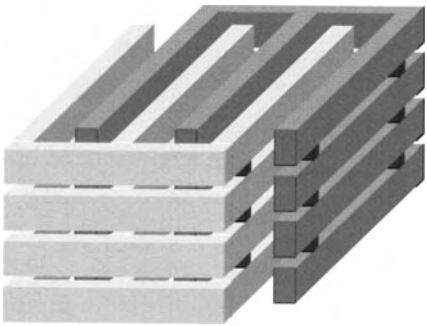


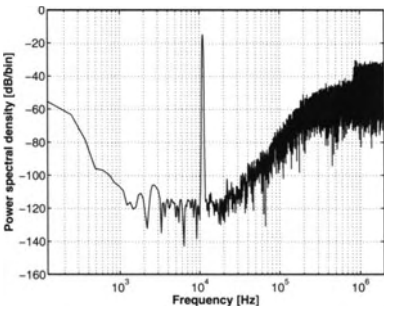
Figure 12: Proposed metal wall capacitance structure.

4.4. Measurement Results

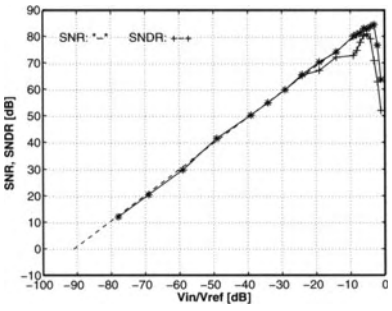
The design was implemented in a standard 90 nm pure digital CMOS technology. No additional technology features, e.g. low-V_T transistors, are used in this design. Both the analog and digital power supply voltage are 1 V. The chip core size is $0.42\ mm \times 0.42\ mm$ only. The chip was bonded on a ceramic substrate and then mounted in a copper-beryllium box to shield the chip from the external interferences. The measurement was done by feeding high quality sinusoid signals into the modulator and capturing the output data by a logic analyzer. Finally the collected data was processed in the Matlab. Fig. 13(a) shows the output spectrum of an 11 kHz input signal. It can be seen that the peak SNR reaches 85 dB and the peak signal to noise plus distortion ratio (SNDR) reaches 81 dB. Fig. 13(b) shows the plot of the SNR and SNDR vs. the input amplitude. A dynamic range (DR) of 88 dB has reached. The total power consumption is 140 μW excluding the power consumption of the output buffer. Table 2 summarizes the measured performances.

5. Conclusions

A low-power low-voltage Σ-Δ modulator was designed and implemented in a 90 nm CMOS technology. Measurement results show that it is possible to design high-performance Σ-Δ modulators in ultra-deep-submicron CMOS technologies. Table 3 shows the performance comparison of recently published low-voltage low-



(a) Measured output spectrum of an 11 kHz sinusoidal input.



(b) Measured SNR and SNDR vs. input amplitude.

Figure 13: Measured output spectrum and SNR, SNDR vs. input amplitude.

Table 2: Measured performance summary

Sampling frequency	4	MHz
Signal bandwidth	20	kHz
Over sampling ratio	100	
Supply voltage	1	V
Analog power consumption	130	μW
Digital power consumption	10	μW
Peak SNR	85	dB
Peak SNDR	81	dB
DR	88	dB
Reference voltage	0.6	V
Active die area	0.018	mm^2

Table 3: Performance comparison

Names and year	Vdd [V]	DR [dB]	BW [kHz]	Power [μW]	FOM
Keskin,2002 [12]	1.0	80	20	5600	5.9e-6
Sauerbrey,2002 [13]	0.7	75	8	80	52e-6
Dessouky,2001 [14]	1.0	88	25	950	275e-6
Peluso,1998 [15]	0.9	77	16	40	330e-6
This work	1.0	88	20	140	1493e-6

power Σ-Δ modulators whose supply voltage is not higher than 1.0 V. The figure-of-merit (FOM) is defined as:

$$FOM = \frac{4kT \cdot f_B \cdot DR}{P} \tag{9}$$

Where k is the Boltzmann's constant, T is the absolute temperature, f_B and P are the signal bandwidth and power consumption of the Σ-Δ ADC, respectively. The FOM is a measure of the power efficiency of a Σ-Δ ADC, taking the signal bandwidth and dynamic range into consideration. However, the supply voltage is not taken into consideration here. To make a fair comparison, all the converters should be working at approximately the same supply voltage. From the table it is seen that this work achieves the highest FOM among these Σ-Δ ADCs.

Following the low-voltage and low-power design strategies described in section 3., the power consumption of the proposed Σ-Δ ADC has been effectively decreased. For digital parts, the smaller transistor feature size helps to decrease the power consumption. Clocked at 4 MHz, the total digital part of this modulator consumes 10 μW only. Comparing to other CMOS technologies, ultra-deep-submicron CMOS technologies, e.g. 90 nm technology, have some advantages to implement the low-power low-voltage Σ-Δ modulators.

- The rated supply voltage is low in ultra-deep-submicron CMOS technologies. As a result, the threshold voltage of the transistor is low too, which is advantageous to implement low-voltage applications. No special designed low-voltage circuits are needed, which simplified the circuits and lower the power consumption.
- Due to the low threshold voltage in ultra-deep-submicron CMOS technologies, for SC circuits, the switch can be driven directly without the clock boosting circuits, resulting a lower power consumption.

- For digital part in the converter, the shorter the transistor length is, the less power is consumed. That is the driving force of the technology scaling-down.
- More metal layers can be used in ultra-deep-submicron CMOS technologies. For mixed-signal design, these metal layers can be used to build lateral capacitances with the high unit-capacitance.
- Better matching properties are found in ultra-deep-submicron CMOS technologies, which is always helpful for analog designs.

There are also disadvantages associated with ultra-deep-submicron CMOS technologies.

- In ultra-deep-submicron CMOS technologies the transistor characteristics degrade significantly. The intrinsic gain of the transistor is insufficient for most applications and the linearity is bad. And in the low-voltage environment, these drawbacks are getting even worse. Another problem associated with ultra-deep-submicron technologies is the transistor thermal noise level and the $1/f$ noise corner frequency is higher than that of deep-submicron technologies. The impacts of the increased thermal noise and higher $1/f$ noise corner frequency should be seriously considered in many mixed-signal and RF designs.
- The supply voltage is limited in ultra-deep-submicron CMOS technologies. No node inside the circuits can be allowed to be exposed to voltages higher than the rated supply voltage, which limits the usage of some special circuits, e.g. clock boosting and voltage doublers etc. And normally the low supply voltage leads a low over-drive voltage of the transistor, which forces the transistor works in the weak to moderate inversion region and partially compensates the high operation speed of the technology.

In a word, for low-voltage Σ-Δ ADC designs, moving into the 90 nm technology is beneficial in the term of power-consumption. The disadvantage is the linearity problem, which can be solved by employing some novel system topologies. By using special design techniques, high-performance Σ-Δ modulators can be implemented using the 90 nm technology. The proposed design and measurement have proved it.

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